



Intel® Open Source HD Graphics

Programmer's Reference Manual

For the 2016 Intel Atom™ Processors, Celeron™ Processors, and
Pentium™ Processors based on the "Apollo Lake" Platform
(Broxton Graphics)

Volume 1: Preface

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Release Notes

This Programmer's Reference Manual (PRM) contains content that applies to Broxton only. See the *Intel® Open Source HD Graphics, Intel Iris™ Graphics, and Intel Iris™ Pro Graphics Programmer's Reference Manual for the 2015 -2016 Intel Core™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Skylake" Platform* for content that applies to both Skylake and Broxton.

The following Registers and Structures, located in the Skylake Open Source PRM, have been superseded in Broxton.

Registers	Structures
ASL Storage ATS Capability ATS Control ATS Extended Capability Header Base Data of Stolen Memory Base of GTT Stolen Memory BLC_PWM_CTL BLC_PWM_DATA Built In Self Test Cache Line Size Capabilities A Capabilities B Capabilities Control Capabilities Pointer Capability Identifier Class Code Device 2 Control Device Enable Device Identification DPLL_CFGCR1 DPLL_CFGCR2 DPLL_CTRL1 DPLL_CTRL2 DPLL_STATUS GMBUS0 GMBUS1 GMBUS2 GMBUS3 GMBUS4 GMBUS5 GMCH Graphics Control GPIO_CTL Graphics Memory Range Address Graphics System Event Graphics Translation Table Memory Mapped Range Address GTC_CTL GTC_DDA_M GTC_DDA_N GTC_PORT_CTL GTC_PORT_TX_CURR	Clock Gating Disable Format



Registers	Structures
Hardware Scratch Read Write Header Type Interrupt Line Interrupt Pin I/O Base Address LCPLL1_CTL LCPLL2_CTL Master Latency Timer Maximum Latency Message Address Message Control Message Data Message Signaled Interrupts Capability ID Minimum Grant Mirror of Base Data of Stolen Memory Mirror of Capabilities A Mirror of Capabilities B Mirror of Device Enable Mirror of GMCH Graphics Control Multi Size Aperture Control Outstanding Page Request Allocation Outstanding Page Request Capacity Page Request Control Page Request Extended Capability Header Page Request Status PASID Capability PASID Control PASID Extended Capability Header PCI Command PCI Express Capability PCI Express Capability Header PCI Express Device Capabilities PCI Express Device Control PCI Express Device Status PCI Status PORT_CLK_SEL PP_CONTROL PP_DIVISOR PP_OFF_DELAYS PP_ON_DELAYS PP_STATUS RAWCLK_FREQ SBLC_PWM_CTL1 SBLC_PWM_CTL2 SFUSE_STRAP SHOTPLUG_CTL SHOTPLUG_CTL2 SHPD_FILTER_CNT SHPD_PULSE_CNT SINTERRUPT Software SCI Software SMI	



Registers	Structures
South Display Engine Interrupt Bit Definition Subsystem Identification Subsystem Vendor Identification Vendor Identification Video BIOS ROM Base Address VTd Status WRPLL_CTL	

About This Programmer's Reference Manual

This Preface serves as an Introduction to the Programmer's Reference Manual (PRM) for the Graphics Processing Unit (GPU) included on the Apollo Lake (Broxton Graphics) series of chips.

A Public View of the PRM

For each major chip series, Intel publicly releases a version of the PRM for the Open Source development community and developers at large. For those releases, we release the PRM in Portable Document Format (PDF).

Without Cross-book Links

Cross-book hyperlinks could not reasonably be included for the PDF. Instead, those links have been disabled and colored dark red and display in a serif font for easy recognition. This is an example:

RING_BUFFER_TAIL – Ring Buffer Tail

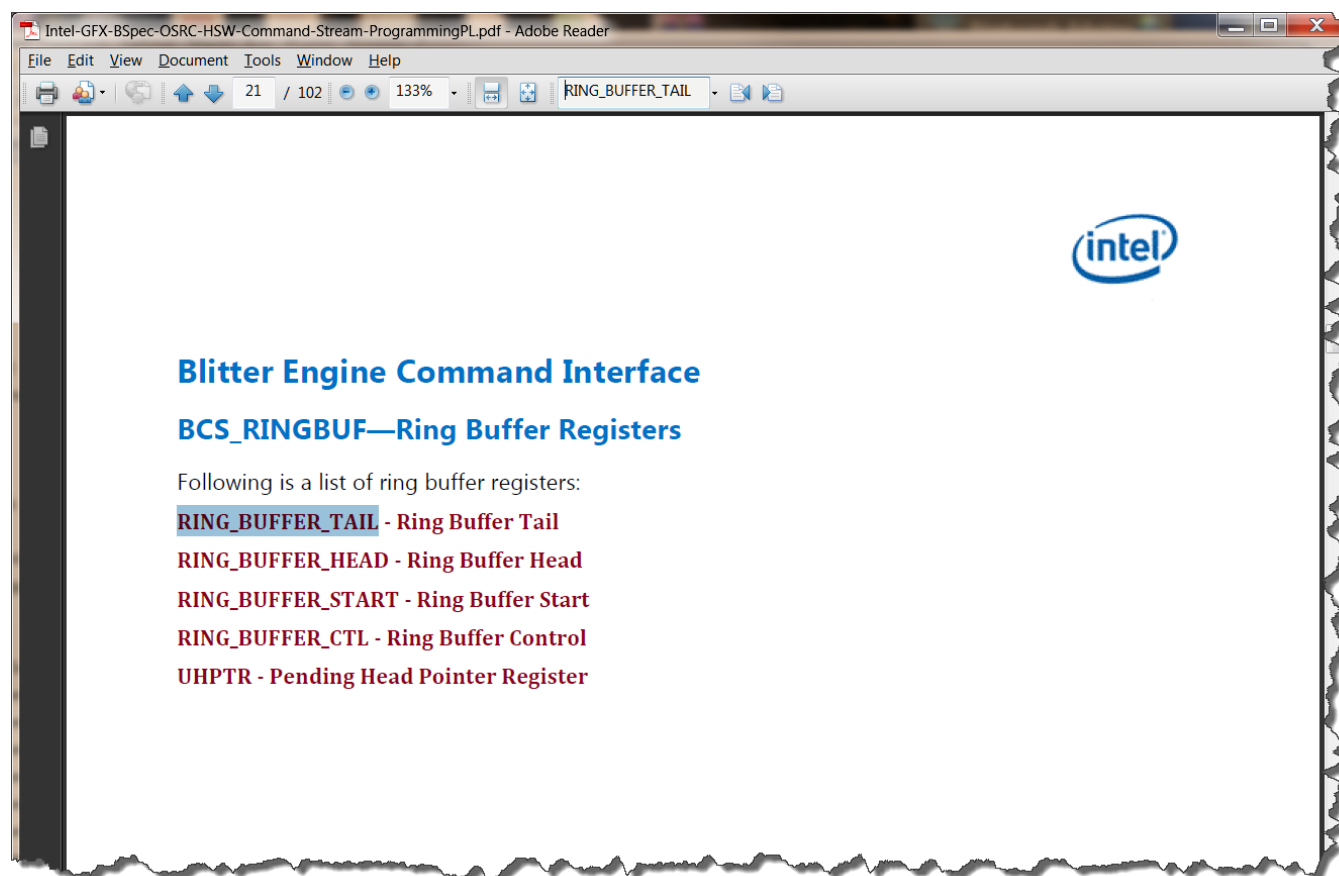
RING_BUFFER_HEAD – Ring Buffer Head

Searching Across Multiple PDF Files

You can quickly access the detailed explanation for each named memory address, command, structure or enumerator utilizing the Advanced Search capabilities in Acrobat Reader.

To maximize the efficiency of the search, make sure to place all PRM PDFs in a single folder, or at least the four Command Reference PDFs in a single folder.

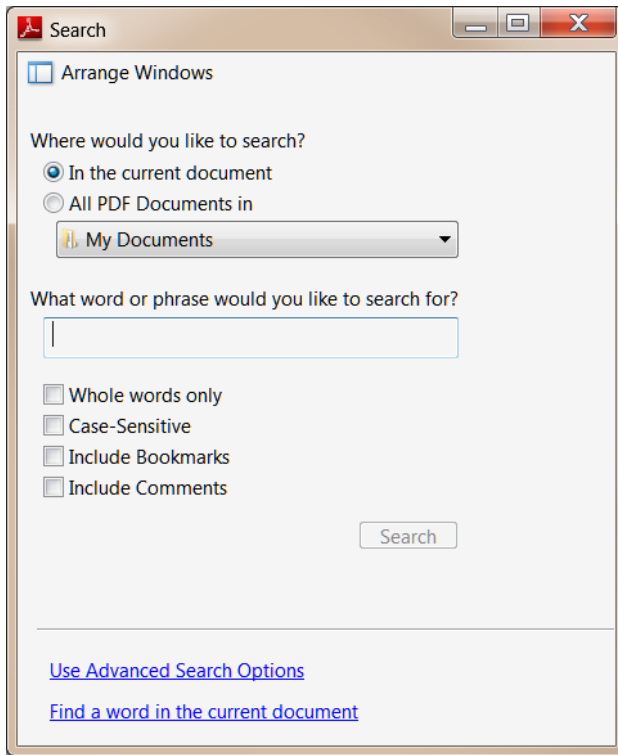
Let's walk through an example PDF search ... you might be reading the Command Stream Programming module PDF file and encounter the page illustrated below.



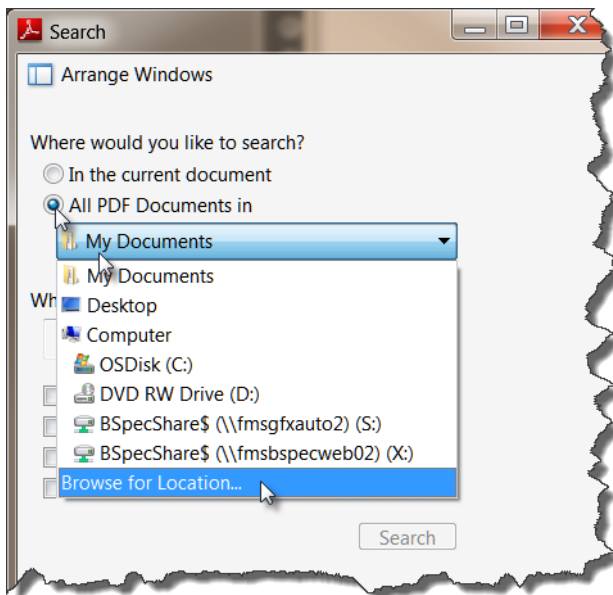
To view the detailed explanation of one of the listed registers ... for this example, we will use **RING_BUFFER_TAIL** ...

1. Simply select **Search** or **Advanced Search** from the **Edit** menu, depending on the version of Acrobat you might be using. (If you are using some other PDF Reader, it probably will also have advanced search capabilities.)

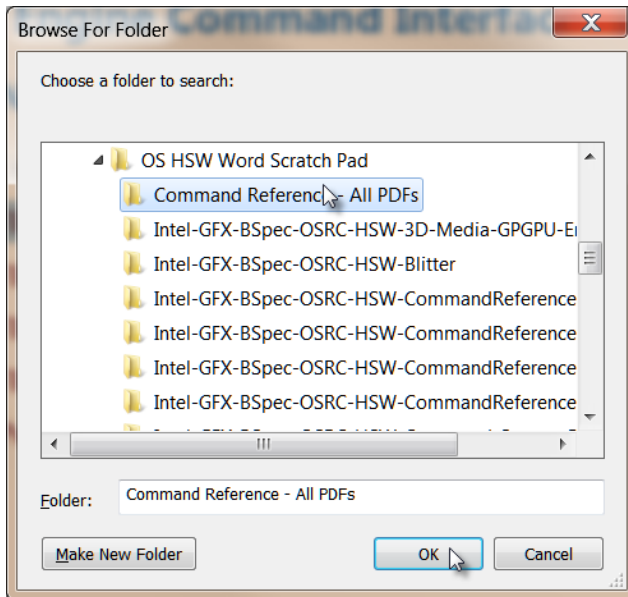
A search dialog box then displays.



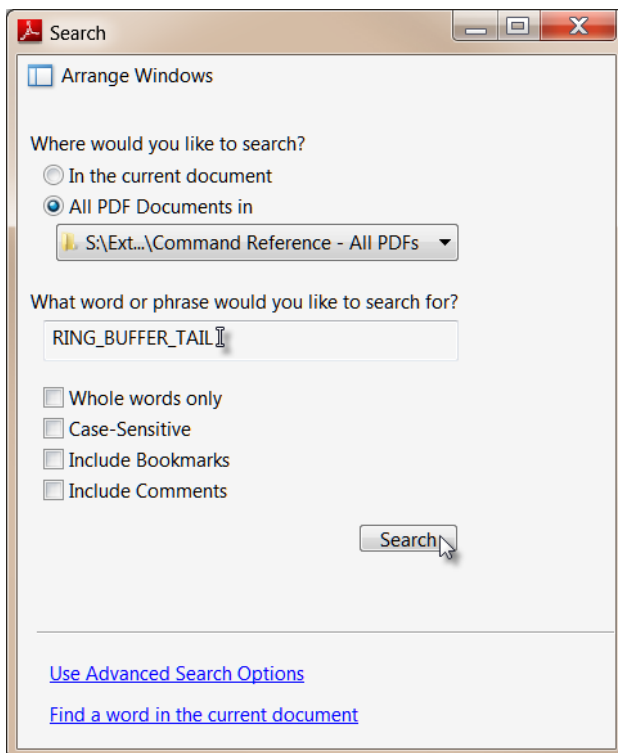
2. Select the **All PDF Documents in** radio button, click the pull-down list box, then select **Browse for Location...**



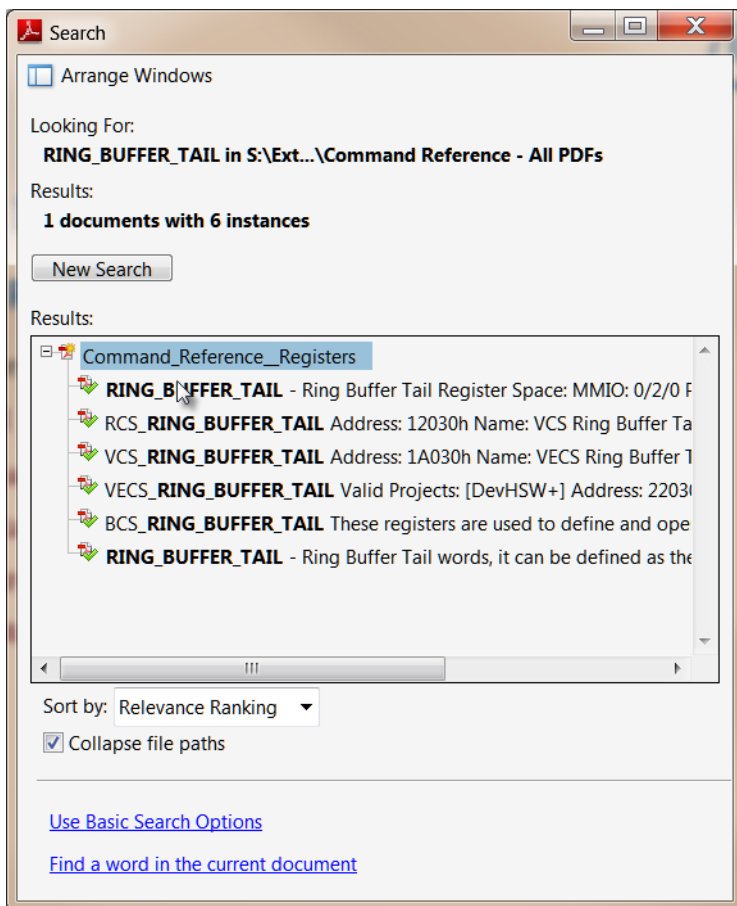
3. Browse to and select the folder containing the pertinent PDF files and click **OK**.



4. The Browse for Folder dialog closes and the focus shifts back to the original Search dialog. Enter the word or phrase from the red, serif text in the **What word or phrase would you like to search for?** text box and click **Search**.



As matches are found, they will be listed. When the search is complete, the dialog will appear similar to the following:





Click the most relevant result and the PDF file containing that result will open at the correct page.

The screenshot shows a PDF document titled "Intel-GFX-BSpec-OSRC-HSW-CommandReference-Registers.pdf" open in Adobe Reader. The document is at page 28 of 1153, with a zoom level of 111%. The main content area displays the Intel logo and the section title "Ring Buffer Tail". Below this, a table lists register details for "RING_BUFFER_TAIL - Ring Buffer Tail".

RING_BUFFER_TAIL - Ring Buffer Tail	
Register Space:	MMIO: 0/2/0
Project:	HSW
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	02030h
Name:	RCS Ring Buffer Tail
ShortName:	RCS_RING_BUFFER_TAIL
Address:	12030h
Name:	VCS Ring Buffer Tail
ShortName:	VCS_RING_BUFFER_TAIL
Address:	1A030h
Name:	VECS Ring Buffer Tail
ShortName:	VECS_RING_BUFFER_TAIL
Valid Projects:	[DevHSW+]
Address:	22030h
Name:	BCS Ring Buffer Tail
ShortName:	BCS_RING_BUFFER_TAIL

These registers are used to define and operate the "ring buffer" mechanism which can be used to pass instructions to the command interface. The buffer itself is located in a linear memory region. The ring buffer is defined by a 4 Dword register set that includes starting address, length, head offset, tail offset, and control information.

Refer to the Programming Interface chapter for a detailed description of the parameters specified in this ring buffer register set, restrictions on the placement of ring buffer memory, arbitration rules, and in how the ring buffer can be used to pass instructions.

Ring Buffer Tail Offsets must be properly programmed before ring is enabled. A Ring Buffer can be enabled



Organization of the PRM

The Intel® Graphics PRM is organized into the following content areas:

Command Reference provides a tabular graphical interface tool for searching for and displaying command opcodes, registers, structures, and instructions.

GPU Overview introduces the GPU and its subsystems. This includes high level descriptions of its hardware pipelines, command formats, register maps, and supported memory/surface formats.

Configurations tracks the evolution of the graphics architecture and provides generational information for many basic architectural attributes.

Memory Views covers the Graphics Memory Interface, including memory interface functions, tiling, the physical graphics memory, page faults and error handling, memory types, common video and non-video surface formats, and other information related to the memory interface.

Command Stream Programming describes the programming interfaces for Command Streamer, which manages the use of the 3D and Media pipelines. It performs switching between pipelines and forwarding command streams to the currently active pipeline. It also manages the allocation of the Unified Return Buffer (URB) and helps support the Constant URB Entry (CURBE) function. It includes the following topics:

Topic
Command Formats
Blitter Engine Command Interface
Render Engine Command Interface
Video Codec Engine Command Interface
Video Enhancement Engine Command Interface
Preemption
Command Streamer (CS) ALU Programming
Resource Streamer

3D/Media/GPGPU Engine includes the following topics:

- Command stream backend processing
- The Graphics L3 large-storage cache, which also acts as a GFX Unified Return Buffer (URB)
- Shared Local Memory (SLM)
- Messaging
- Shared functions for the 3D pipeline
- 3D fixed functions
- Media/GPGPU Pipeline processing via both fixed functions and programmable GPU cores
- Execution units

Display describes display engine registers, including display HD audio configuration and programming. It includes VGA and extended VGA registers, CPU display registers, North display engine registers, and



South display engine registers. The Display section explains audio codec verbs, display audio configuration registers, and the display audio controller registers.

Workarounds provide software workarounds for known issues with the GPU.



Device Tags and Definitions

The following table lists device "tags" (abbreviations, projects) used in various parts of this document as aliases for the device names. PRM content without any device tagging applies to all devices in the current spec.

Program Name	Graphics Architecture	Description
Broxton (marketed as Apollo Lake)	Gen9LP	A low-power variation of Skylake, using a 14nm process.



Reserved Bits and Software Compatibility

In many register, instruction, and memory layout descriptions, certain bits are marked as "Reserved." When bits are marked as reserved, it is essential for compatibility with future devices that the software treat these bits as having a future, though unknown, effect. The behavior of reserved bits should be regarded as undefined *and unpredictable*. Software should follow the guidelines listed below in dealing with reserved bits:

1. Do not depend on the states of any reserved bits when testing values of registers that contain such bits.
2. Mask out the reserved bits before testing.
3. Do not depend on the states of any reserved bits when storing to an instruction or to a register.
4. When loading a register or formatting an instruction, always load the reserved bits with the values indicated in the documentation (if any), or reload them with the values previously read from the register.



Terminology

Term	Abbr.	Definition
3D Pipeline	--	One of the two pipelines supported in the GPE. The 3D Pipeline is a set of fixed-function units arranged in a pipelined fashion, which process 3D-related commands by spawning EU threads. Typically this processing includes rendering primitives. See <i>3D Pipeline</i> .
Adjacency	--	One can consider a single line object as existing in a strip of connected lines. The neighboring line objects are called "adjacent objects", with the non-shared endpoints called the "adjacent vertices." The same concept can be applied to a single triangle object, considering it as existing in a mesh of connected triangles. Each triangle shares edges with three other adjacent triangles, each defined by a non-shared adjacent vertex. Knowledge of these adjacent objects/vertices is required by some object processing algorithms (e.g., silhouette edge detection). See <i>3D Pipeline</i> .
Application IP	AIP	Application Instruction Pointer. This is part of the control registers for exception handling for a thread. Upon an exception, hardware moves the current IP into this register and then jumps to System Instruction Pointer (SIP).
Architectural Register File	ARF	A collection of architecturally visible registers for a thread such as address registers, accumulator, flags, notification registers, IP, null, etc.
Binding Table	--	Memory-resident list of pointers to surface state blocks (also in memory).
Binding Table Pointer	BTP	Pointer to a binding table, specified as an offset from the Surface State Base Address register.
Blitter	BLT	Block Image Transferrer
Bypass Mode	--	Mode where a given fixed function (FF) unit is disabled and forwards data down the pipeline unchanged. Not supported by all FF units.
Byte	B	A numerical data type of 8 bits, B represents a signed byte integer.
Child Thread	--	A branch-node or a leaf-node thread that is created by another thread. It is a kind of thread associated with the media fixed function pipeline. A child thread is originated from a thread (the parent) executing on an EU and forwarded to the Thread Dispatcher by the TS unit. A child thread may or may not have child threads depending on whether it is a branch-node or a leaf-node thread. All pre-allocated resources such as URB and scratch memory for a child thread are managed by its parent thread. See also <i>Parent Thread</i> .
Clip Space	--	A 4-dimensional coordinate system within which a clipping frustum is defined. Object positions are projected from Clip Space to NDC space via "perspective divide" by the W coordinate, and then viewport mapped into Screen Space.
Clipper	--	3D fixed function unit that removes invisible portions of the drawing sequence by discarding (culling) primitives or by "replacing" primitives with one or more primitives that replicate only the visible portion of the original primitive.
Color Calculator	CC	Part of the Data Port shared function, the color calculator performs fixed-function pixel operations (e.g., blending) before writing a result pixel into the render cache.



Term	Abbr.	Definition
Command	--	Directive fetched from a ring buffer in memory by the Command Streamer and routed down a pipeline. Should not be confused with instructions which are fetched by the instruction cache subsystem and executed on an EU.
Command Streamer	CS or CSI	Functional unit of the Graphics Processing Engine that fetches commands, parses them, and routes them to the appropriate pipeline.
Constant URB Entry	CURBE	A UE that contains "constant" data for use by various stages of the pipeline.
Control Register	CR	The read-write registers are used for thread mode control and exception handling for a thread.
Core	--	Alternative name for an EU in the multi-processor system. See <i>EU</i> .
Data Port	DP	Shared function unit that performs a majority of the memory access types on behalf of SNB+ programs. The Data Port contains the render cache and the constant cache and performs all memory accesses requested by SNB+ programs except those performed by the Sampler. See <i>DataPort</i> .
Degenerate Object	--	Object that is invisible due to coincident vertices or because it does not intersect any sample points (usually due to being tiny or a very thin sliver).
Destination	--	Describes an output or write operand.
Destination Size	--	The number of data elements in the destination of a SIMD instruction.
Destination Width	--	The size of each of (possibly) many elements of the destination of a SIMD instruction.
Double Quad word (DQword)	DQ	A fundamental data type, DQ represents 16 bytes.
Double word (DWord)	D or DW	A fundamental data type, D or DW represents 4 bytes.
Drawing Rectangle	--	A screen-space rectangle within which 3D primitives are rendered. An object's screen-space positions are relative to the Drawing Rectangle origin. See <i>Strips and Fans</i> .
End of Block	EOB	A 1-bit flag in the non-zero DCT coefficient data structure indicating the end of an 8x8 block in a DCT coefficient data buffer.
End Of Thread	EOT	A message sideband signal on the Output message bus signifying that the message requester thread is terminated. A thread must have at least one SEND instruction with the EOT bit in the message descriptor field set to properly terminate.
Exception	--	Type of (normally rare) interruption to EU execution of a thread's instructions. An exception occurrence causes the EU thread to begin executing the System Routine, which is designed to handle exceptions.
Execution Channel	--	Single lane of a SIMD operand.
Execution Size	ExecSize	Execution Size indicates the number of data elements processed by an SIMD instruction. It is one of the instruction fields and can be changed per instruction.
Execution Unit	EU	An EU is a multi-threaded processor within the multi-processor system. Each EU is a fully-capable processor containing instruction fetch and decode, register files, source operand swizzle and SIMD ALU, etc. An EU is also referred to as a core.



Term	Abbr.	Definition
Execution Unit Identifier	EUID	The 4-bit field within a thread state register (SR0) that identifies the row and column location of the EU where a thread is located. A thread can be uniquely identified by the EUID and TID.
Execution Width	ExecWidth	The width of each of several data elements that may be processed by a single SIMD instruction.
Extended Math Unit	EM	A Shared Function that performs more complex math operations on behalf of several EUs.
Fixed Function	FF	Function of the pipeline that is performed by dedicated (vs. programmable) hardware.
Fixed Function ID	FFID	Unique identifier for a fixed function unit.
Gateway	GW	See <i>Message Gateway</i> .
General Register File	GRF	Large read/write register file shared by all the EUs for operand sources and destinations. This is the most commonly used read-write register space organized as an array of 256-bit registers for a thread.
General State Base Address	--	The Graphics Address of a block of memory-resident "state data", which includes state blocks, scratch space, constant buffers, and kernel programs. The contents of this memory block are referenced via offsets from the contents of the General State Base Address register. See <i>Graphics Processing Engine</i> .
Geometry Shader	GS	Fixed-function unit between the vertex shader and the clipper that (if enabled) dispatches "geometry shader" threads on its input primitives. Application-supplied geometry shaders normally expand each input primitive into several output primitives to perform 3D modeling algorithms such as fur/fins.
Graphics Address	--	The GPE virtual address of some memory-resident object. This virtual address gets mapped by a GTT or PGTT to a physical memory address. Note that many memory-resident objects are referenced not with Graphics Addresses, but instead with offsets from a "base address register".
Graphics Processing Engine	GPE	Collective name for the Subsystem, the 3D and Media pipelines, and the Command Streamer.
Guardband	GB	Region that may be clipped against to make sure objects do not exceed the limitations of the renderer's coordinate space.
Horizontal Stride	HorzStride	The distance in element-sized units between adjacent elements of a region-based GRF access.
Immediate floating point vector	VF	A numerical data type of 32 bits, an immediate floating point vector of type VF contains 4 floating point elements with 8 bits each. The 8-bit floating point element contains a sign field, a 3-bit exponent field and a 4-bit mantissa field. It may be used to specify the type of an immediate operand in an instruction.
Immediate integer vector	V	A numerical data type of 32 bits, an immediate integer vector of type V contains 8 signed integer elements with 4 bits each. The 4-bit integer element is in 2's complement form. It may be used to specify the type of an immediate operand in an instruction.
Index Buffer	IB	Buffer in memory containing vertex indices.



Term	Abbr.	Definition
Intel Architecture	IA	
Instance	--	In the context of the VF unit, an instance is one of a sequence of sets of similar primitive data. Each set has identical vertex data but may have unique instance data that differentiates it from other sets in the sequence.
Instruction	--	Data in memory directing an EU operation. Instructions are fetched from memory, stored in a cache, and executed on one or more cores. Not to be confused with commands which are fetched and parsed by the command streamer and dispatched down the 3D or Media pipeline.
Instruction Pointer	IP	The address (really an offset) of the instruction currently being fetched by an EU. Each EU has its own IP.
Instruction Set Architecture	ISA	The ISA describes the instructions supported by an EU.
Instruction State Cache	ISC	On-chip memory that holds recently-used instructions and state variable values.
Interface Descriptor	--	Media analog of a State Descriptor.
Intermediate Z	IZ	Completion of the Z (depth) test at the front end of the Windower/Masker unit when certain conditions are met (no alpha, no pixel-shader computed Z values, etc.).
Inverse Discrete Cosine Transform	IDCT	The stage in the video decoding pipe between IQ and MC.
Inverse Quantization	IQ	A stage in the video decoding pipe between IS and IDCT.
JIT	--	Just-in-time compiler, aka "jitter".
Kernel	--	A sequence of instructions that is logically part of the driver or generated by the jitter. Differentiated from a Shader which is an application supplied program that is translated by the jitter to instructions.
Logical Ring Context Area	LRCA	Memory area used to store contents of registers and state information required for initiating and resuming communication between software application and hardware graphics pipeline via Ring Buffers.
Least Significant Bit	LSB	The bit with the lowest bit position within a group of bits, which could be a bit group, DWord, field, instruction, memory range, register, or structure. For example, bit 0 of a DWord.
MathBox	--	<i>See Extended Math Unit</i>
Media	--	Term for operations such as video decode and encode that are normally performed by the Media pipeline.
Media Pipeline	--	Fixed function stages dedicated to media and "generic" processing, sometimes referred to as the generic pipeline.
Memory-mapped Input/Output	MMIO	A method for performing input/output between the CPU/GPU and peripheral devices.
Message	--	Messages are data packages transmitted from a thread to another thread, another shared function, or another fixed function. Message passing is the primary communication mechanism of the architecture.



Term	Abbr.	Definition
Message Gateway	--	Shared function that enables thread-to-thread message communication/synchronization, used solely by the Media pipeline.
Most Significant Bit	MSB	The bit with the highest bit position within a group of bits, which could be a bit group, DWord, field, instruction, memory range, register, or structure. For example, bit 31 of a DWord.
Motion Compensation	MC	Part of the video decoding pipe.
Motion Picture Expert Group	MPEG	MPEG is the international standard body JTC1/SC29/WG11 under ISO/IEC that has defined audio and video compression standards such as MPEG-1, MPEG-2, and MPEG-4.
Motion Vector Field Selection	MVFS	A four-bit field selecting reference fields for the motion vectors of the current macroblock.
Multiple Render Targets	MRT	Multiple independent surfaces that may be the target of a sequence of 3D or Media commands that use the same surface state.
Normalized Device Coordinates	NDC	Clip Space Coordinates that have been divided by the Clip Space "W" component.
Object	--	A single triangle, line, or point.
OpenGL	OGL	Open Graphics Library . A graphics API specification associated with Linux.
Parent Thread	--	A thread corresponding to a root-node or a branch-node in thread generation hierarchy. A parent thread may be a root thread or a child thread depending on its position in the thread generation hierarchy.
Pipeline Stage	--	An abstracted element of the 3D Pipeline, providing functions performed by a combination of the corresponding hardware FF unit and the threads spawned by that FF unit.
Pipelined State Pointers	PSP	Pointers to state blocks in memory that are passed down the pipeline.
Pixel Shader	PS	Shader that is supplied by the application, translated by the jitter and is dispatched to the EU by the Windower (conceptually) once per pixel.
Point	--	A drawing object characterized only by position coordinates and width.
Primitive	--	Synonym for object: triangle, rectangle, line, or point.
Primitive Topology	--	A composite primitive such as a triangle strip or a line list. Also includes the objects triangle, line, and point as degenerate cases.
Provoking Vertex	--	The vertex of a primitive topology from which vertex attributes that are constant across the primitive are taken.
Quad Quad word (QQword)	QQ	A fundamental data type, QQ represents 32 bytes.
Quad Word (QWord)	QW	A fundamental data type, QW represents 8 bytes.
Rasterization	--	Conversion of an object represented by vertices into the set of pixels that make up the object.



Term	Abbr.	Definition
Region-based addressing	--	Collective term for the register addressing modes available in the EU instruction set that permit discontinuous register data to be fetched and used as a single operand.
Render Cache	RC	Cache in which pixel color and depth information is written before being written to memory, and where prior pixel destination attributes are read in preparation for blending and Z test.
Render Target	RT	A destination surface in memory where render results are written.
Render Target Array Index	--	Selector of which of several render targets the current operation is targeting.
Resource Streamer	RS	Functional unit of the Graphics Processing Engine that examines the commands in the ring buffer in an attempt to pre-process certain long latency items for the remainder of the graphics processing.
Root Thread	--	A root-node thread. A thread corresponds to a root-node in a thread generation hierarchy. It is a kind of thread associated with the media fixed function pipeline. A root thread is originated from the VFE unit and forwarded to the Thread Dispatcher by the TS unit. A root thread may or may not have child threads. A root thread may have scratch memory managed by TS. A root thread with children has its URB resource managed by the VFE.
Sampler	--	Shared function that samples textures and reads data from buffers on behalf of EU programs.
Scratch Space	--	Memory allocated to the subsystem that is used by EU threads for data storage that exceeds their register allocation, persistent storage, storage of mask stack entries beyond the first 16, etc.
Shader	--	A program supplied by the application in a high level shader language, and translated to instructions by the jitter.
Shared Function	SF	Function unit that is shared by EUs. EUs send messages to shared functions, that consume the data and may return results. The Sampler, Data Port, and Extended Math unit are all shared functions.
Shared Function ID	SFID	Unique identifier used by kernels and shaders to target shared functions and to identify their returned messages.
Single Instruction Multiple Data	SIMD	A parallel processing architecture that exploits data parallelism at the instruction level. It can also be used to describe the instructions in such an architecture or to describe the amount of data parallelism in a particular instruction (SIMD8 for example).
Source	--	Describes an input or read operand.
Spawn	--	To initiate a thread for execution on an EU. Done by the thread spawner as well as most FF units in the 3D Pipeline.
Sprite Point	--	Point object using full range texture coordinates. Points that are not sprite points use the texture coordinates of the point's center across the entire point object.
State Descriptor	--	Blocks in memory that describe the state associated with a particular FF, including its associated kernel pointer, kernel resource allowances, and a pointer to its surface state.

Term	Abbr.	Definition
State Register	SR	The read-only registers containing the state information of the current thread, including the EUID/TID, Dispatcher Mask, and System IP.
State Variable	SV	An individual state element that can be varied to change the way given primitives are rendered or media objects processed. On state variables persist only in memory and are cached as needed by rendering/processing operations except for a small amount of non-pipelined state.
Stream Output	--	A term for writing the output of a FF unit directly to a memory buffer instead of, or in addition to, the output passing to the next FF unit in the pipeline. Currently only supported for the Geometry Shader (GS) FF unit.
Strips and Fans	SF	Fixed function unit whose main function is to decompose primitive topologies such as strips and fans into primitives or objects.
Sub-Register	--	Subfield of a SIMD register. A SIMD register is an aligned fixed size register for a register file or a register type. For example, a GRF register, <i>r2</i> , is a 256-bits wide, 256-bit aligned register. A sub-register, <i>r2.3:d</i> , is the fourth dword of GRF register <i>r2</i> .
Subsystem	--	The name given to the resources shared by the FF units, including shared functions and EUs.
Surface	--	A rendering operand or destination, including textures, buffers, and render targets.
Surface State Base Pointer	--	Base address used when referencing binding table and surface state data.
Synchronized Root Thread	--	A root thread that is dispatched by TS upon a 'dispatch root thread' message.
System IP	SIP	There is one global System IP register for all the threads. From a thread's point of view, this is a virtual read only register. Upon an exception, hardware performs some bookkeeping and then jumps to SIP.
System Routine	--	Sequence of instructions that handles exceptions. SIP is programmed to point to this routine, and all threads encountering an exception will call it.
Thread	--	An instance of a kernel program executed on an EU. The life cycle for a thread starts from the executing the first instruction after being dispatched from Thread Dispatcher to an EU to the execution of the last instruction – a <i>send</i> instruction with EOT that signals the thread termination. Threads in the system may be independent from each other or communicate with each other through Message Gateway share function.
Thread Dispatcher	TD	Functional unit that arbitrates thread initiation requests from Fixed Functions units and instantiates the threads on EUs.
Thread Identifier	TID	The field within a thread state register (SR0) that identifies which thread slots on an EU a thread occupies. A thread can be uniquely identified by the EUID and TID.
Thread Payload	--	Before a thread starting execution, some amount of data is pre-loaded into the thread's GRF (starting at <i>r0</i>). This data is typically a combination of control information provided by the spawning entity (FF Unit) and data read from the URB.



Term	Abbr.	Definition
Thread Spawner	TS	The second and the last fixed function stage of the media pipeline that initiates new threads on behalf of generic/media processing.
Topology	--	See <i>Primitive Topology</i> .
Unified Return Buffer	URB	The on-chip memory managed/shared by Fixed Functions in order for a thread to return data that will be consumed either by a Fixed Function or other threads.
Unsigned Byte integer	UB	A numerical data type of 8 bits.
Unsigned Double Word integer	UD	A numerical data type of 32 bits. It may be used to specify the type of an operand in an instruction.
Unsigned Word integer	UW	A numerical data type of 16 bits. It may be used to specify the type of an operand in an instruction.
Unsynchronized Root Thread	--	A root thread that is automatically dispatched by TS.
URB Dereference	--	
URB Entry	UE	URB Entry: A logical entity stored in the URB (such as a vertex), referenced via a URB Handle.
URB Entry Allocation Size	--	Number of URB entries allocated to a Fixed Function unit.
URB Fence	Fence	Virtual, movable boundaries between the URB regions owned by each FF unit.
URB Handle	--	A unique identifier for an URB entry that is passed down a pipeline.
URB Reference	--	
Variable Length Decode	VLD	The first stage of the video decoding pipe that consists mainly of bit-wide operations.
Vertex Buffer	VB	Buffer in memory containing vertex attributes.
Vertex Cache	VC	Cache of Vertex URB Entry (VUE) handles tagged with vertex indices. See the VS chapter for details on this cache.
Vertex Fetcher	VF	The first FF unit in the 3D Pipeline responsible for fetching vertex data from memory. Sometimes referred to as the Vertex Formatter.
Vertex Header	--	Vertex data required for every vertex appearing at the beginning of a Vertex URB Entry.
Vertex ID	--	Unique ID for each vertex that can optionally be included in vertex attribute data sent down the pipeline and used by kernel/shader threads.
Vertex Shader	VS	An API-supplied program that calculates vertex attributes. Also refers to the FF unit that dispatches threads to "shade" (calculate attributes for) vertices.
Vertex URB Entry	VUE	An URB entry that contains data for a specific vertex.
Vertical Stride	VertStride	The distance in element-sized units between 2 vertically-adjacent elements of a region-based GRF access.
Video Front End	VFE	The first fixed function in the generic pipeline; performs fixed-function media operations.



Term	Abbr.	Definition
Viewport	VP	
Windower IZ	WIZ	Term for Windower/Masker that encapsulates its early ("intermediate") depth test function.
Windower/Masker	WM	Fixed function triangle/line rasterizer.
Word	W	A numerical data type of 16 bits, W represents a signed word integer.



Intel® Open Source HD Graphics

Programmer's Reference Manual

For the 2016 Intel Atom™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Apollo Lake" Platform (Broxton Graphics)

Volume 2a: Command Reference: Instructions (Command Opcodes)

May 2017, Revision 1.0



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3DSTATE_DS

3DSTATE_DS		
Source: RenderCS		
Length Bias: 2		
The state used by DS is defined with this inline state packet		
DWord	Bit	Description
0	31:29	Command Type
		Default Value: 3h GFXPIPE
		Format: OpCode
	28:27	Command SubType
		Default Value: 3h GFXPIPE_3D
		Format: OpCode
	26:24	3D Command Opcode
		Default Value: 0h 3DSTATE_PIPELINED
		Format: OpCode
	23:16	3D Command Sub Opcode
		Default Value: 1Dh 3DSTATE_DS
		Format: OpCode
	15:8	Reserved
		Format: MBZ
	7:0	DWord Length
		Default Value: 9h Excludes DWord (0,1)
		Format: =n Total Length - 2
1..2	63:6	Kernel Start Pointer
		Format: InstructionBaseOffset[63:6]Kernel This field specifies the starting location of the kernel program run by threads spawned by this FF unit. It is specified as a 64-byte-granular offset from the Instruction Base Address. This field is ignored if DS Function Enable is DISABLED.
	5:0	Reserved
		Format: MBZ
3	31	Reserved
		Format: MBZ

**3DSTATE_DS**

3DSTATE_DS		
30	Vector Mask Enable	
	Format:	U1 Enumerated Type
	Upon subsequent DS thread dispatches, this bit is loaded into the EU's Vector Mask Enable (VME, cr0.0[3]) thread state. Refer to EU documentation for the definition and use of VME state.	
	Value	Name Description
	0h	Dmask The EU will use the Dispatch Mask (supplied by the DS stage) for instruction execution.
	1h	Vmask The EU will use the Vector Mask (derived from the Dispatch Mask) for instruction execution.
Programming Notes		
Under normal conditions SW shall specify DMask, as the DS stage will provide a Dispatch Mask appropriate to SIMD4x2 or SIMD8 thread execution (as a function of dispatch mode). E.g., for SIMD4x2 thread execution, the DS stage will generate a Dispatch Mask that is equal to what the EU would use as the Vector Mask. For SIMD8 execution there is no known usage model for use of Vector Mask (as there is for PS shaders).		
29:27	Sampler Count	
	Format:	U3
	Specifies how many samplers (in multiples of 4) the kernel uses. Used only for prefetching the associated sampler state entries.	
	This field is ignored if DS Function Enable is DISABLED.	
	Value	Name Description
	0h	No Samplers
1h	1-4 Samplers	between 1 and 4 samplers used
2h	5-8 Samplers	between 5 and 8 samplers used
3h	9-12 Samplers	between 9 and 12 samplers used
4h	13-16 Samplers	between 13 and 16 samplers used
26	Reserved	
	Format:	MBZ
25:18	Binding Table Entry Count	
	Format:	U8
	When HW Generated Binding Table is disabled: Specifies how many binding table entries the kernel uses. Used only for prefetching of the binding table entries and associated surface state. Note: For kernels using a large number of binding table entries, it may be wise to set this field to zero to avoid prefetching too many entries and thrashing the state cache. This field is ignored if DS Function Enable is DISABLED.	



3DSTATE_DS

3DSTATE_DS											
	When HW Generated Binding Table bit is enabled: This field indicates which cache lines (512bit units - 32 Binding Table Entry section) should be fetched. Each bit in this field corresponds to a cache line. Only the 1st 4 non-zero Binding Table entries of each 32 Binding Table entry section prefetched will have its surface state prefetched. <table><tr><th>Value</th><th colspan="2">Name</th></tr><tr><td>[0,255]</td><td colspan="2"></td></tr></table> Programming Notes When HW binding table bit is set, it is assumed that the Binding Table Entry Count field will be generated at JIT time.		Value	Name		[0,255]					
Value	Name										
[0,255]											
17	Thread Dispatch Priority Format:U1 Enumerated Type Specifies the priority of the thread for dispatch: This field is ignored if DS Function Enable is DISABLED. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Normal</td><td>Normal Priority</td></tr><tr><td>1h</td><td>High</td><td>High Priority</td></tr></table>		Value	Name	Description	0h	Normal	Normal Priority	1h	High	High Priority
Value	Name	Description									
0h	Normal	Normal Priority									
1h	High	High Priority									
16	Floating Point Mode Format:U1 Enumerated Type Specifies the initial floating point mode used by the dispatched thread. This field is ignored if DS Function Enable is DISABLED. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>IEEE-754</td><td>Use IEEE-754 Rules</td></tr><tr><td>1h</td><td>Alternate</td><td>Use alternate rules</td></tr></table>		Value	Name	Description	0h	IEEE-754	Use IEEE-754 Rules	1h	Alternate	Use alternate rules
Value	Name	Description									
0h	IEEE-754	Use IEEE-754 Rules									
1h	Alternate	Use alternate rules									
15	Reserved Format:MBZ										
14	Accesses UAV Format:Enable This bit gets loaded into EU CR0.1[12] (note the bit # difference). See Exceptions and ISA Execution Environment. Programming Notes This field must not be set when DS Function Enable is disabled.										
13	Illegal Opcode Exception Enable Format:Enable This bit gets loaded into EU CR0.1[12] (note the bit # difference). See Exceptions and ISA Execution Environment. This field is ignored if DS Function Enable is DISABLED.										



3DSTATE_DS											
	12:8	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ							
	Format:	MBZ									
	7	Software Exception Enable <table><tr><td>Format:</td><td>Enable</td></tr></table> This bit gets loaded into EU CR0.1[13] (note the bit # difference). See Exceptions and ISA Execution Environment. This field is ignored if DS Function Enable is DISABLED.	Format:	Enable							
Format:	Enable										
6:0	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ								
Format:	MBZ										
4..5	63:10	Scratch Space Base Pointer <table><tr><td>Format:</td><td>GeneralStateOffset[63:10]ScratchSpace</td></tr></table> Specifies the starting location of the scratch space area allocated to this FF unit as a 1K-byte aligned offset from the General State Base Address. If required, each thread spawned by this FF unit will be allocated some portion of this space, as specified by Per-Thread Scratch Space. The computed offset of the thread-specific portion will be passed in the thread payload as Scratch Space Offset. The thread is expected to utilize "stateless" DataPort read/write requests to access scratch space, where the DataPort will cause the General State Base Address to be added to the offset passed in the request header. This field is ignored if DS Function Enable is DISABLED.	Format:	GeneralStateOffset[63:10]ScratchSpace							
	Format:	GeneralStateOffset[63:10]ScratchSpace									
	9:4	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ							
Format:	MBZ										
3:0	Per-Thread Scratch Space <table><tr><td>Format:</td><td>U4 power of 2 Bytes over 1K Bytes</td></tr></table> Specifies the amount of scratch space to be allocated to each thread spawned by this FF unit. The driver must allocate enough contiguous scratch space, starting at the Scratch Space Base Pointer, to ensure that the Maximum Number of Threads can each get Per-Thread Scratch Space size without exceeding the driver-allocated scratch space. This field is ignored if DS Function Enable is DISABLED. <table><tr><th>Value</th><th>Name</th></tr><tr><td>[0,11]</td><td>indicating [1K Bytes, 2M Bytes]</td></tr></table> <table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">This amount is available to the kernel for information only. It will be passed verbatim (if not altered by the kernel) to the Data Port in any scratch space access messages, but the Data Port will ignore it.</td></tr></table>	Format:	U4 power of 2 Bytes over 1K Bytes	Value	Name	[0,11]	indicating [1K Bytes, 2M Bytes]	Programming Notes		This amount is available to the kernel for information only. It will be passed verbatim (if not altered by the kernel) to the Data Port in any scratch space access messages, but the Data Port will ignore it.	
Format:	U4 power of 2 Bytes over 1K Bytes										
Value	Name										
[0,11]	indicating [1K Bytes, 2M Bytes]										
Programming Notes											
This amount is available to the kernel for information only. It will be passed verbatim (if not altered by the kernel) to the Data Port in any scratch space access messages, but the Data Port will ignore it.											
6	31:25	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ							
Format:	MBZ										



3DSTATE_DS

	24:20	Dispatch GRF Start Register For URB Data	
		Format:	GRFRegister[4:0]
		Specifies the starting GRF register number for the URB portion (Constant + Vertices) of the thread payload. This field is ignored if DS Function Enable is DISABLED. When SIMD8_SINGLE_OR_DUAL_PATCH dispatch mode is selected, HW shall increment the GRF start register by 1 when a dual patch simd8 thread is dispatched.	
		Value	Name
		[0,31]	indicating GRF [R0, R31]
		Programming Notes When SIMD8_SINGLE_OR_DUAL_PATCH dispatch mode is selected, SW shall program this field to a value of 6 or greater to accommodate either the DUAL_PATCH or SIMD8_SINGLE_PATCH payloads.	
	19:18	Reserved	
		Format:	MBZ
	17:11	Patch URB Entry Read Length	
		Format:	U7
		Specifies how much data (in 256-bit units) is to be read from the Patch URB entry and passed in the DS thread payload. This field is ignored if DS Function Enable is DISABLED.	
		Value	Name
	10	Reserved	
		Format:	MBZ
	9:4	Patch URB Entry Read Offset	
		Format:	U6
		Specifies the offset (in 256-bit units) at which Patch URB data is to be read from the URB before being included in the thread payload. This field is ignored if DS Function Enable is DISABLED.	
		Value	Name
7	3:0	Reserved	
		Format:	MBZ
	31	Reserved	
		Format:	MBZ
	30	Reserved	
		Format:	MBZ

**3DSTATE_DS**

3DSTATE_DS											
29:21	Maximum Number of Threads										
	Format:	U9-1 Thread Count									
	Specifies the maximum number of simultaneous DS threads allowed to be active. Used to avoid using up the scratch space. Programming the value of the max threads over the number of threads based off number of threads supported in the execution units may improve performance since the architecture allows threads to be buffered between the check for max threads and the actual dispatch into the EU. Programming the max values to a number less than the number of threads supported in the execution units may reduce performance.										
	This field is ignored if DS Function Enable is DISABLED.										
<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[0,111]</td><td></td><td>indicating thread count of [1,112]</td></tr></table>				Value	Name	Description	[0,111]		indicating thread count of [1,112]		
Value	Name	Description									
[0,111]		indicating thread count of [1,112]									
20:11	Reserved										
	Format:	MBZ									
10	Statistics Enable										
	Format:	Enable									
If ENABLED, this FF unit will engage in statistics gathering. Refer to the Statistics Gathering section.											
If DISABLED, statistics information associated with this FF stage will be left unchanged.											
This field is ignored if DS Function Enable is DISABLED.											
9:5	Reserved										
	Format:	MBZ									
4:3	Dispatch Mode										
	Format:	U2									
This field specifies how the DS stage generates DS thread requests, and correspondingly impacts the DS thread payload. The setting of this field must agree with how the DS kernel was compiled.											
This field is ignored if DS Function Enable is DISABLED.											
<table><tr><th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr><tr><td>0h</td><td>SIMD4X2</td><td>DS threads are passed one patch, up to 2 domain point inputs, and up to two output vertex handles. The DS kernel (at KSP) is expected to run in SIMD4x2 execution mode. The DUAL_PATCH KSP is ignored. The Single Domain Point Dispatch field can be used to force single domain point dispatches.</td><td></td></tr></table>				Value	Name	Description	Programming Notes	0h	SIMD4X2	DS threads are passed one patch, up to 2 domain point inputs, and up to two output vertex handles. The DS kernel (at KSP) is expected to run in SIMD4x2 execution mode. The DUAL_PATCH KSP is ignored. The Single Domain Point Dispatch field can be used to force single domain point dispatches.	
Value	Name	Description	Programming Notes								
0h	SIMD4X2	DS threads are passed one patch, up to 2 domain point inputs, and up to two output vertex handles. The DS kernel (at KSP) is expected to run in SIMD4x2 execution mode. The DUAL_PATCH KSP is ignored. The Single Domain Point Dispatch field can be used to force single domain point dispatches.									



3DSTATE_DS

3DSTATE_DS					
		1h	SIMD8_SINGLE_PATCH	DS threads are passed one patch, up to 8 domain point inputs, and up to 8 output vertex handles. All the domain points are associated with the single input patch. The DS kernel (at KSP) is expected to run in SIMD8 execution mode. The DUAL_PATCH KSP is ignored.	
		2h	SIMD8_SINGLE_OR_DUAL_PATCH	SIMD8_SINGLE_OR_DUAL_PATCH This mode enables use of both the KSP and the DUAL_PATCH KSP. The KSP kernel operates just like in SIMD8_SINGLE_PATCH mode. See DUAL_PATCH Thread Execution for a discussion of how the DUAL_PATCH KSP is used.	At least 2 HS URB handles must be allocated in order to enable this mode. SIMD8_SINGLE_OR_DUAL_PATCH must not be used if the domain shader kernel uses primitive id.
		3h	Reserved		
2	Compute W Coordinate Enable				
	Format:		Enable		
If ENABLED, the DS unit will (for each domain point) compute $W = 1 - (U + V)$ and pass the result as a floating point value in the DS thread payload. If DISABLED, 0.0 will be passed. This field must only be ENABLED for the tessellation of TRI domains, where UVW coordinates are required. This field must be DISABLED for other domains (as they only require UV coordinates) otherwise the computed W coordinate is UNDEFINED. This field is ignored if DS Function Enable is DISABLED.					
1	Cache Disable				
	Format:		Disable		
This bit controls the operation of the DS Cache. This field is ignored if DS Function Enable is DISABLED. If the DS Cache is DISABLED and the DS Function is ENABLED, the DS Cache is not used and all incoming domain points will be passed to DS threads. If the DS Cache is ENABLED and the DS Function is ENABLED, incoming domain points that do not hit in the DS Cache will be passed to DS threads. The DS Cache is invalidated whenever the DS Cache becomes DISABLED , whenever the DS Function Enable toggles, and between patches.					



3DSTATE_DS											
8	0	Function Enable <table><tr><td>Format:</td><td>Enable</td></tr></table> If ENABLED, DS threads will be spawned to process incoming domain points which miss in the DS cache. If DISABLED, the DS stage goes into pass-through mode and performs no specific processing. This field is always used. <table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">The tessellation stages (HS, TE and DS) must be enabled/disabled as a group. I.e., draw commands can only be issued if all three stages are enabled or all three stages are disabled, otherwise the behavior is UNDEFINED.</td></tr></table>	Format:	Enable	Programming Notes		The tessellation stages (HS, TE and DS) must be enabled/disabled as a group. I.e., draw commands can only be issued if all three stages are enabled or all three stages are disabled, otherwise the behavior is UNDEFINED.				
	Format:	Enable									
	Programming Notes										
	The tessellation stages (HS, TE and DS) must be enabled/disabled as a group. I.e., draw commands can only be issued if all three stages are enabled or all three stages are disabled, otherwise the behavior is UNDEFINED.										
	31:27	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ							
Format:	MBZ										
26:21	Vertex URB Entry Output Read Offset <table><tr><td>Format:</td><td>U6</td></tr></table> Specifies the offset (in 256-bit units) at which Vertex URB data is to be read from the URB by SBE. <table><tr><th>Value</th><th>Name</th></tr><tr><td>[0,63]</td><td></td></tr></table>	Format:	U6	Value	Name	[0,63]					
Format:	U6										
Value	Name										
[0,63]											
20:16	Vertex URB Entry Output Length <table><tr><td>Format:</td><td>U5</td></tr></table> Specifies the amount of URB data written for each Vertex URB entry, in 256-bit register increments. <table><tr><th>Value</th><th>Name</th></tr><tr><td>[1,16]</td><td></td></tr></table> <table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">This length does not include the vertex header.</td></tr></table>	Format:	U5	Value	Name	[1,16]		Programming Notes		This length does not include the vertex header.	
Format:	U5										
Value	Name										
[1,16]											
Programming Notes											
This length does not include the vertex header.											
15:8	User Clip Distance Clip Test Enable Bitmask <table><tr><td>Format:</td><td>U8</td></tr></table> This 8 bit mask field selects which of the 8 user clip distances against which trivial reject / trivial accept / must clip determination needs to be made. DX10 allows simultaneous use of ClipDistance and Cull Distance test of up to 8 distances.	Format:	U8								
Format:	U8										
7:0	User Clip Distance Cull Test Enable Bitmask <table><tr><td>Format:</td><td>U8</td></tr></table> This 8 bit mask field selects which of the 8 user clip distances against which trivial reject / trivial accept determination needs to be made (does not cause a must clip). DX10 allows simultaneous use of ClipDistance and Cull Distance test of up to 8 distances.	Format:	U8								
Format:	U8										



3DSTATE_DS				
9..10	63:6	DUAL_PATCH Kernel Start Pointer <table><tr><td>Format:</td><td>InstructionBaseOffset[63:6]Kernel</td></tr></table> This field specifies the starting location of the DUAL_PATCH kernel program run by threads spawned by this FF unit. It is specified as a 64-byte-granular offset from the Instruction Base Address. This field is ignored if DS Function Enable is DISABLED. See DUAL_PATCH Thread Execution for a discussion of how the DUAL_PATCH KSP is used.	Format:	InstructionBaseOffset[63:6]Kernel
	Format:	InstructionBaseOffset[63:6]Kernel		
5:0	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ	
Format:	MBZ			



3DSTATE_GS

3DSTATE_GS					
Source:		RenderCS			
Length Bias:		2			
Controls the GS stage hardware.					
DWord	Bit	Description			
0	31:29	Command Type			
		Default Value:	3h GFXPIPE		
		Format:	OpCode		
	28:27	Command SubType			
		Default Value:	3h GFXPIPE_3D		
		Format:	OpCode		
	26:24	3D Command Opcode			
		Default Value:	0h 3DSTATE_PIPELINED		
		Format:	OpCode		
	23:16	3D Command Sub Opcode			
		Default Value:	11h 3DSTATE_GS		
		Format:	OpCode		
15:8	Reserved				
	Format:	MBZ			
7:0	DWord Length				
	Format:	=n			
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>8h</td><td>Excludes DWord (0,1) [Default]</td></tr></table>	Value	Name	8h	Excludes DWord (0,1) [Default]
Value	Name				
8h	Excludes DWord (0,1) [Default]				
1..2	63:6	Kernel Start Pointer			
		Format:	InstructionBaseOffset[63:6]Kernel		
	This field specifies the starting location (1st GEN4 core instruction) of the kernel program run by threads spawned by this FF unit. It is specified as a 64-byte-granular offset from the Instruction Base Address.				
1..2	5:0	Reserved			
		Format:	MBZ		



3DSTATE_GS

3	31	Single Program Flow		
		Specifies the initial condition of the kernel program as either a single program flow (SIMDn _{xm} with m = 1) or as multiple program flows (SIMDn _{xm} with m > 1). See CR0 description in ISA Execution Environment.		
		Value	Name	Description
		0h	Disable	Single Program Flow disabled
		1h	Enable	Single Program Flow enabled
	30	Vector Mask Enable		
		Format: Enable Enumerated Type		
		Upon subsequent GS thread dispatches, this bit is loaded into the EU's Vector Mask Enable (VME, cr0.0[3]) thread state. Refer to EU documentation for the definition and use of VME state.		
		Value	Name	Description
		0h	Dmask	The EU will use the Dispatch Mask (supplied by the GS stage) for instruction execution.
		1h	Vmask	The EU will use the Vector Mask (derived from Dispatch Mask) for instruction execution.
		Programming Notes		
		Under normal conditions SW shall specify DMask, as the GS stage will provide a Dispatch Mask appropriate to SIMD4x2 or SIMD8 thread execution (as a function of dispatch mode). E.g., for SIMD4x2 execution, the GS stage will generate a Dispatch Mask that is equal to what the EU would use as the Vector Mask. For SIMD8 execution there is no known usage model for use of Vector Mask (as there is for PS shaders).		
	29:27	Sampler Count		
		Format: U3		
		Specifies how many samplers (in multiples of 4) the geometry shader kernel uses. Used only for prefetching the associated sampler state entries.		
		Value	Name	Description
		0h	No Samplers	No Samplers used
		1h	1-4 Samplers	Between 1 and 4 samplers used
		2h	5-8 Samplers	Between 5 and 8 samplers used
		3h	9-12 Samplers	Between 9 and 12 samplers used
		4h	13-16 Samplers	Between 13 and 16 samplers used
		5h-7h	Reserved	
	26	Reserved		

**3DSTATE_GS**

3DSTATE_GS		
25:18	Binding Table Entry Count	
	Format:	U8
	When HW Generated Binding Table is disabled: Specifies how many binding table entries the kernel uses. Used only for prefetching of the binding table entries and associated surface state. Note: For kernels using a large number of binding table entries, it may be wise to set this field to zero to avoid prefetching too many entries and thrashing the state cache.	
	When HW Generated Binding Table bit is enabled: This field indicates which cache lines (512bit units - 32 Binding Table Entry section) should be fetched. Each bit in this field corresponds to a cache line. Only the 1st 4 non-zero Binding Table entries of each 32 Binding Table entry section prefetched will have its surface state prefetched.	
	Programming Notes	
	When HW binding table bit is set, it is assumed that the Binding Table Entry Count field will be generated at JIT time.	
17	Thread Dispatch Priority Specifies the priority of the thread for dispatch.	
	Value	Name Description
	0h	Normal Normal thread dispatch priority
	1h	High High thread dispatch priority
16	Floating Point Mode Specifies the initial floating point mode used by the dispatched thread.	
	Value	Name Description
	0h	IEEE-754 Use IEEE-754 Rules
	1h	Alternate Use alternate rules
15:14	Reserved	
	Format:	MBZ
13	Illegal Opcode Exception Enable	
	Format:	Enable This bit gets loaded into EU CR0.1[12] (note the bit # difference). See <i>Exceptions and ISA Execution Environment</i> .
12	Accesses UAV	
	Format:	Enable This field must be set when GS has a UAV access.
	Programming Notes	
	This field must not be set when GS Function Enable is disabled.	
11	Mask Stack Exception Enable	
	Format:	Enable This bit gets loaded into EU CR0.1[11]. See <i>Exceptions and ISA Execution Environment</i> .



3DSTATE_GS									
	10:8	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ					
	Format:	MBZ							
	7	Software Exception Enable <table><tr><td>Format:</td><td>Enable</td></tr></table> This bit gets loaded into EU CR0.1[13] (note the bit # difference). See <i>Exceptions and ISA Execution Environment</i>.	Format:	Enable					
	Format:	Enable							
	6	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ					
Format:	MBZ								
5:0	Expected Vertex Count <table><tr><td>Format:</td><td>U6</td></tr></table> Specifies the number of vertices per input object expected by the GS thread. Input topologies not matching this expect value are discarded. Note that DiscardAdjacency is also considered (e.g., if the value programmed is 3 and DiscardAdjacency is set, TRILIST_ADJ and TRISTRIP_ADJ topologies are <u>not</u> discarded as they will pass 3 vertices/object to the GS threads). <table><tr><th>Value</th><th>Name</th></tr><tr><td>[1,32]</td><td></td></tr></table>	Format:	U6	Value	Name	[1,32]			
Format:	U6								
Value	Name								
[1,32]									
4..5	63:10	Scratch Space Base Pointer <table><tr><td>Format:</td><td>GeneralStateOffset[63:10]ScratchSpace</td></tr></table> Specifies the starting location of the scratch space area allocated to this FF unit as a 1K-byte aligned offset from the General State Base Address. If required, each thread spawned by this FF unit will be allocated some portion of this space, as specified by Per-Thread Scratch Space. The computed offset of the thread-specific portion will be passed in the thread payload as Scratch Space Offset. The thread is expected to utilize "stateless" DataPort read/write requests to access scratch space, where the DataPort will cause the General State Base Address to be added to the offset passed in the request header. This field is ignored if VS Function Enable is DISABLED.	Format:	GeneralStateOffset[63:10]ScratchSpace					
	Format:	GeneralStateOffset[63:10]ScratchSpace							
	9:4	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ					
Format:	MBZ								
3:0	Per-Thread Scratch Space <table><tr><td>Format:</td><td>U4 power of 2 Bytes over 1K Bytes</td></tr></table> Specifies the amount of scratch space to be allocated to each thread spawned by this FF unit. The driver must allocate enough contiguous scratch space, starting at the Scratch Space Base Pointer, to ensure that the Maximum Number of Threads can each get Per-Thread Scratch Space size without exceeding the driver-allocated scratch space. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[0,11]</td><td></td><td>indicating [1K Bytes, 2M Bytes]</td></tr></table>	Format:	U4 power of 2 Bytes over 1K Bytes	Value	Name	Description	[0,11]		indicating [1K Bytes, 2M Bytes]
Format:	U4 power of 2 Bytes over 1K Bytes								
Value	Name	Description							
[0,11]		indicating [1K Bytes, 2M Bytes]							
6	31	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ					
Format:	MBZ								



3DSTATE_GS		
30:29	Dispatch GRF Start Register For URB Data [5:4]	
	Format:	U2
Specifies bit [5:4] of the starting GRF register number for the URB portion (Constant + Vertices) of the thread payload. The Dispatch GRF Start Register For URB Data [3:0] field is used to specify bits [3:0] of the starting GRF register number.		
28:23	Output Vertex Size	
	Format:	U6
	[0,63] indicating [1,64] 16B units	
	Specifies the size of each vertex stored in the GS output entry (following any Control Header data) as a number of 128-bit units (minus one).	
	Programming Notes Programming Restrictions: The vertex size must be programmed as a multiple of 32B units with the following exception: Rendering is disabled (as per SOL stage state) and the vertex size output by the GS thread is 16B. If rendering is enabled (as per SOL state) the vertex size must be programmed as a multiple of 32B units. In other words, the only time software can program a vertex size with an odd number of 16B units is when rendering is disabled.	
22:17	Output Topology	
	Format:	3D_Prim_Topo_Type
This field specifies the topology type (3DPrimType) to be associated with GS-thread output vertices (if any).		
16:11	Vertex URB Entry Read Length	
	Specifies the amount of URB data read and passed in the thread payload for each Vertex URB entry, in 256-bit register increments.	
	Programming Notes Programming Restriction: This field must be a non-zero value if Include Vertex Handles is cleared to zero.	
10	Include Vertex Handles	
	Format:	Boolean
	If set, all the input Vertex URB handles are included in the payload. These are referred to as "pull model" URB handles, as the thread will use them to read from the URB.	
	Programming Notes Programming Restriction: This field must be set if Vertex URB Entry Read Length is cleared to zero.	



3DSTATE_GS										
7	9:4	Vertex URB Entry Read Offset <table><tr><td>Format:</td><td>U6</td></tr></table> Specifies the offset (in 256-bit units) at which Vertex URB data is to be read from the URB before being included in the thread payload. This offset applies to all Vertex URB entries passed to the thread.	Format:	U6						
	Format:	U6								
	3:0	Dispatch GRF Start Register For URB Data <table><tr><td>Format:</td><td>U4</td></tr></table> Specifies the starting GRF register number for the URB portion (Constant + Vertices) of the thread payload. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[0,15]</td><td></td><td>indicating GRF [R0, R15]</td></tr></table> Programming Notes If Include Vertex Handles is enabled (pull or hybrid handles case), then For simd4x2: For DUAL_OBJECT dispatch mode this field should be: $((2*\text{numVerticesPerObject}) + 8 - 1)/8) + 1$ For SINGLE and DUAL_INSTANCE dispatch modes this field should be: $((\text{numVerticesPerObject} + 8 - 1)/8) + 1$ If Include Primitive ID is set, then add 1 to the value obtained by using the above If Include Vertex Handles is enabled (pull or hybrid handles case), then For SKL simd8: For InstanceCount == 1: numVerticesPerObject 2 For InstanceCount > 1: $((\text{numVerticesPerObject} 8 - 1)/8) 2$ If Include Primitive ID is set, then add 1 to the value obtained by using the above When Include Vertex Handles is set for non-instanced SIMD8 dispatch of PATCHLIST_14..32 objects, pushed vertex data and/or pushed constants cannot be used as they would need to start in the payload beyond the range of this field (i.e., beyond R15). When Include PrimitiveID is also set, this issue extends to non-instanced SIMD8 dispatch of PATCHLIST_13..32 objects.	Format:	U4	Value	Name	Description	[0,15]		indicating GRF [R0, R15]
	Format:	U4								
	Value	Name	Description							
	[0,15]		indicating GRF [R0, R15]							
	31:26	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ						
	Format:	MBZ								
	25:24	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ						
	Format:	MBZ								
23:20	Control Data Header Size <table><tr><td>Format:</td><td>U4</td></tr></table> Specifies the number of 32B units of control data header located at the start of the GS URB entry. The value 0 indicates there is no control data header, and Control Data Format is ignored. Software must ensure that the Control Data Header Size is sufficient to accommodate the maximum number of vertices output by the GS thread. It is UNDEFINED for a GS thread to report	Format:	U4							
Format:	U4									



3DSTATE_GS

3DSTATE_GS

		more output vertices than can be accommodated in a non-zero-sized header. (If the header size is zero, by definition neither cut nor StreamID bits are defined).			
		Value		Name	
		[0,8]		32B Units	
19:15	Instance Control				
	Format:		U5-1 #Instances		
	Specifies the number of instances (minus one) for each input object. To avoid confusion, this document uses the term " InstanceCount " to refer to InstanceControl+1, with a range of [1,32] If InstanceCount >1, DUAL_OBJECT mode is invalid. Software will likely want to use DUAL_INSTANCE mode for higher performance, but SINGLE mode is also supported. When InstanceCount =1 (one instance per object), software can decide which dispatch mode to use. DUAL_OBJECT mode would likely be the best choice for performance, followed by SINGLE mode. DUAL_INSTANCE mode is not recommended but is supported.				
	Value	Name	Description		
	[0,31]		Indicating [1,31] instances		
14:13	Default Stream Id				
	Format:			U2	
	When the GS is enabled, unless the GS output entry contains StreamID bits in the control header, this field specifies the default StreamID associated with any GS-thread output vertices. When the GS is disabled, StreamID will be output as 0.				
12:11	Dispatch Mode				
	Format:			U2	
	This field specifies how the GS unit dispatches multiple instances and/or multiple objects.				
	Value	Name	Description	Programming Notes	
	0h	Single	Each thread shades a single instance of one object.		
	1h	Dual Instance	Each thread shades possibly two instances of one object. If the InstanceCount is odd, a trailing dispatch of only one instance will be made for each object received. Not recommended if InstanceCount = 1, assuming a kernel optimized for SINGLE or DUAL_OBJECT dispatch would outperform a kernel compiled for DUAL_INSTANCE but only passed one instance.		
	2h	Dual Object	Each thread shades one instance of possibly two objects. The GS unit attempt to pair objects together into one dispatch, but under some circumstances only one object may be dispatched (as controlled by the DispatchMask generated by the GS unit). Not valid for objects		



3DSTATE_GS

			with more than 16 vertices per object. Not valid if InstanceCount > 1 (more than one instance per object).										
	3h	SIMD8	Each thread shades up to 8 different objects or (if InstanceCount > 1) 8 instances of a single object.	The driver must send pipe control with a cs stall after a 3dstate_gs state change and the Dispatch Mode is simd8 and the number of handles allocated to gs is less than 16.									
Programming Notes The GS must be allocated at least two URB handles or behavior is UNDEFINED for Dual Instance or Dual Object mode.													
10	Statistics Enable Format: Enable This bit controls whether GS-unit-specific statistics register(s) can be incremented. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable</td><td>GS_INVOCATIONS_COUNT and GS_PRIMITIVES_COUNT cannot increment</td></tr><tr><td>1h</td><td>Enable</td><td>GS_INVOCATIONS_COUNT and GS_PRIMITIVES_COUNT can increment</td></tr></table>				Value	Name	Description	0h	Disable	GS_INVOCATIONS_COUNT and GS_PRIMITIVES_COUNT cannot increment	1h	Enable	GS_INVOCATIONS_COUNT and GS_PRIMITIVES_COUNT can increment
Value	Name	Description											
0h	Disable	GS_INVOCATIONS_COUNT and GS_PRIMITIVES_COUNT cannot increment											
1h	Enable	GS_INVOCATIONS_COUNT and GS_PRIMITIVES_COUNT can increment											
9:5	Invocations Increment Value Format: U5 Specifies how much to increment the GS_INVOCATIONS_COUNT for each instance of each object. This control is provided to allow software to process multiple instances (from an API POV) in a single kernel invocation. In SINGLE dispatch mode, the counter will increment by this value for each dispatch (as it's only one instance of one object). In DUAL_INSTANCE mode, the counter will be incremented by the value if only one instance is included in the dispatch (i.e., the last odd instance), otherwise the counter will be incremented by twice this value. In DUAL_OBJECT dispatch mode, the counter will be incremented by the value if only one object is included in the dispatch (i.e., a forced dispatch of one object), otherwise the counter will be incremented by twice this value. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[0,31]</td><td></td><td>indicating an increment of [1,32]</td></tr></table>				Value	Name	Description	[0,31]		indicating an increment of [1,32]			
Value	Name	Description											
[0,31]		indicating an increment of [1,32]											
4	Include Primitive ID Format: Boolean If set, R1 of the payload is written with Primitive ID value(s). If clear, these Primitive ID values are not included in the payload R1.												

**3DSTATE_GS**

3DSTATE_GS

3	Hint <table><tr><td>Format:</td><td>U1</td></tr></table> This state bit is simply passed in GS thread payloads for use by the GS kernel - it has no other impact on hardware operation.	Format:	U1							
Format:	U1									
2	Reorder Mode This bit controls how vertices of triangle objects resulting from TRISTRIP[_ADJ][_REV] topologies are [re]ordered when passed in the GS thread payload See Object Vertex Ordering table (below). <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>LEADING</td><td>Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the leading (first) vertices are in consecutive order starting at v0. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.</td></tr><tr><td>1h</td><td>TRAILING</td><td>Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the trailing (last) vertices are in consecutive order starting at v2. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.</td></tr></table>	Value	Name	Description	0h	LEADING	Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the leading (first) vertices are in consecutive order starting at v0. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.	1h	TRAILING	Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the trailing (last) vertices are in consecutive order starting at v2. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.
Value	Name	Description								
0h	LEADING	Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the leading (first) vertices are in consecutive order starting at v0. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.								
1h	TRAILING	Reorder the vertices of alternating triangles of a TRISTRIP[_ADJ] such that the trailing (last) vertices are in consecutive order starting at v2. A similar reordering is performed on alternating triangles in a TRISTRIP_REV.								
1	Discard Adjacency <table><tr><td>Format:</td><td>Enable</td></tr></table> When set, adjacent vertices <u>will not be passed</u> in the GS payload when objects with adjacency are processed. Instead, only the non-adjacent vertices will be passed in the same fashion as the without-adjacency form of the primitive. Software should set this bit whenever a GS kernel is used that <u>does not expect</u> adjacent vertices. This allows both with-adjacency/without-adjacency variants of the primitive to be submitted to the pipeline (via 3DPRIMITIVE) - the GS unit will silently discard any adjacent vertices and present the GS thread with only the internal object. When clear, adjacent vertices <u>will be passed</u> to the GS thread, as dictated by the incoming primitive type. Software should only clear this bit when a GS kernel is used that does expect adjacent vertices. E.g., if the GS kernel is compiled to expect a TRIANGLE_ADJ object, software must clear this bit. Software should also clear this bit if the GS kernel expects a POINT or PATCHLIST_n object (which don't have with-adjacency variants). The only hardware assistance is to allow the submission of a with-adjacency variant of a primitive when operating with a GS kernel that expects the without-adjacency variant of the object. (E.g., when the GS kernel is compiled to expect a TRIANGLE object, software should set this bit just in case a TRILIST_ADJ is submitted to the pipeline.) Note that the GS unit is otherwise not aware of the object type that is expected by the GS kernel. It is up to software to ensure that the submitted primitive type (in 3DPRIMITIVE) is otherwise compatible with the object type expected by the GS kernel. (E.g., if the GS kernel expects a LINE_ADJ object, only LINELIST_ADJ or LINESTRIP_ADJ should be submitted, otherwise the GS kernel will produce unpredictable results.) Also note that it is possible to craft a GS kernel which can accept any object type that's thrown at it by first examining the PrimType passed in the payload and then using this info to correctly interpret the number of vertices passed in the payload.	Format:	Enable							
Format:	Enable									
0	Enable <table><tr><td>Format:</td><td>Enable</td></tr></table> Specifies whether the GS stage is enabled or disabled (pass-through).	Format:	Enable							
Format:	Enable									



3DSTATE_GS													
8	31	Control Data Format <table><tr><td>Format:</td><td>U1</td></tr></table> This field specifies the format of the control data header (if any). <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>CUT</td><td>The control data header contains cut bits.</td></tr><tr><td>1h</td><td>SID</td><td>The control data header contains StreamID bits. . Output Topology must be set to POINTLIST, or behavior is UNDEFINED.</td></tr></table>	Format:	U1	Value	Name	Description	0h	CUT	The control data header contains cut bits.	1h	SID	The control data header contains StreamID bits. . Output Topology must be set to POINTLIST, or behavior is UNDEFINED.
		Format:	U1										
		Value	Name	Description									
		0h	CUT	The control data header contains cut bits.									
		1h	SID	The control data header contains StreamID bits. . Output Topology must be set to POINTLIST, or behavior is UNDEFINED.									
	30	Static Output <table><tr><td>Format:</td><td>Enable</td></tr></table> Specifies whether the GS shader outputs a static number of vertices per invocation. If this bit is clear, the number of vertices output by each GS shader invocation is stored by the GS thread at the very beginning of the output URB entry (see GS URB Entry section below).	Format:	Enable									
		Format:	Enable										
		29:27	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ								
		Format:	MBZ										
	26:16	Static Output Vertex Count <table><tr><td>Format:</td><td>U11 Count of object vertices</td></tr></table> If GSEnable is set and StaticOutput is set, this field specifies the total number of vertices output each GS shader invocation. If GSEnable is set and StaticOutput is clear (variable GS output), the total number of vertices output by a GS shader invocation is stored by the thread at the very beginning of the output URB entry. This field is then ignored. (See GS URB Entry below).	Format:	U11 Count of object vertices									
Format:		U11 Count of object vertices											
15:9	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ										
Format:	MBZ												
8:0	Maximum Number of Threads <table><tr><td>Format:</td><td>U9-1 Thread count</td></tr></table> Specifies the maximum number of simultaneous threads allowed to be active. Used to avoid using up the scratch space. Programming the value of the max threads over the number of threads based off number of threads supported in the execution units may improve performance since the architecture allows threads to be buffered between the check for max threads and the actual dispatch into the EU. Programming the max values to a number less than the number of threads supported in the execution units may reduce performance. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[7,111]</td><td></td><td>Indicating thread count of [8,112]</td></tr></table>	Format:	U9-1 Thread count	Value	Name	Description	[7,111]		Indicating thread count of [8,112]				
	Format:	U9-1 Thread count											
	Value	Name	Description										
[7,111]		Indicating thread count of [8,112]											
9	31:27	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ									
	Format:	MBZ											
26:21	Vertex URB Entry Output Read Offset <table><tr><td>Format:</td><td>U6</td></tr></table> Specifies the offset (in 256-bit units) at which Vertex URB data is to be read from the URB by SBE.	Format:	U6										
Format:	U6												



3DSTATE_GS						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>[0,63]</td><td></td></tr></table>	Value	Name	[0,63]	
Value	Name					
[0,63]						
20:16	Vertex URB Entry Output Length					
	Format:	U5				
	Specifies the amount of URB data written for each Vertex URB entry, in 256-bit register increments.					
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>[1,16]</td><td></td></tr></table>	Value	Name	[1,16]		
	Value	Name				
[1,16]						
<table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">This length does not include the vertex header.</td></tr></table>		Programming Notes		This length does not include the vertex header.		
Programming Notes						
This length does not include the vertex header.						
15:8	User Clip Distance Clip Test Enable Bitmask					
	Format:	Enable[8]				
	This 8 bit mask field selects which of the 8 user clip distances against which trivial reject / trivial accept / must clip determination needs to be made. DX10 allows simultaneous use of ClipDistance and Cull Distance test of up to 8 distances.					
7:0	User Clip Distance Cull Test Enable Bitmask					
	Format:	Enable[8]				
	This 8 bit mask field selects which of the 8 user clip distances against which trivial reject / trivial accept determination needs to be made (does not cause a must clip). DX10 allows simultaneous use of ClipDistance and Cull Distance test of up to 8 distances.					



3DSTATE_HS

3DSTATE_HS															
Source:		RenderCS													
Length Bias:		2													
Controls the HS stage hardware.															
DWord	Bit	Description													
0	31:29	Command Type													
		Default Value:	3h GFXPIPE												
		Format:	OpCode												
	28:27	Command SubType													
		Default Value:	3h GFXPIPE_3D												
		Format:	OpCode												
	26:24	3D Command Opcode													
		Default Value:	0h 3DSTATE_PIPELINED												
		Format:	OpCode												
	23:16	3D Command Sub Opcode													
		Default Value:	1Bh 3DSTATE_HS												
		Format:	OpCode												
	15:8	Reserved													
		Format:	MBZ												
	7:0	DWord Length													
		Format:	=n												
<table><tr><th>Value</th><th>Name</th></tr><tr><td>7</td><td>Excludes DWord (0,1) [Default]</td></tr></table>		Value	Name	7	Excludes DWord (0,1) [Default]										
Value	Name														
7	Excludes DWord (0,1) [Default]														
1	31:30	Reserved													
		Format:	MBZ												
	29:27	Sampler Count													
		Format:	U3												
		Specifies how many samplers (in multiples of 4) the HS kernels use. Used only for prefetching the associated sampler state entries.													
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>No Samplers</td><td>no samplers used</td></tr><tr><td>1h</td><td>1-4 Samplers</td><td>between 1 and 4 samplers used</td></tr><tr><td>2h</td><td>5-8 Samplers</td><td>between 5 and 8 samplers used</td></tr></table>	Value	Name	Description	0h	No Samplers	no samplers used	1h	1-4 Samplers	between 1 and 4 samplers used	2h	5-8 Samplers	between 5 and 8 samplers used	
		Value	Name	Description											
		0h	No Samplers	no samplers used											
		1h	1-4 Samplers	between 1 and 4 samplers used											
		2h	5-8 Samplers	between 5 and 8 samplers used											

**3DSTATE_HS**

		3h	9-12 Samplers	between 9 and 12 samplers used
		4h	13-16 Samplers	between 13 and 16 samplers used
		5h-7h	Reserved	Reserved
	26	Reserved		
		Format:		MBZ
	25:18	Binding Table Entry Count		
		Format:		U8
		When HW Generated Binding Table is disabled: Specifies how many binding table entries the kernel uses. Used only for prefetching of the binding table entries and associated surface state. Note: For kernels using a large number of binding table entries, it may be wise to set this field to zero to avoid prefetching too many entries and thrashing the state cache.		
		Programming Notes		
		When HW binding table bit is set, it is assumed that the Binding Table Entry Count field will be generated at JIT time.		
	17	Thread Dispatch Priority Specifies the priority of the thread for dispatch		
		Value	Name	Description
		0h	Normal	Normal Priority
		1h	High	High Priority
	16	Floating Point Mode Specifies the initial floating point mode used by the dispatched thread.		
		Value	Name	Description
		0h	IEEE-754	Use IEEE-754 Rules
		1h	alternate	Use alternate rules
	15:14	Reserved		
		Format:		MBZ
	13	Illegal Opcode Exception Enable		
		Format:		Enable
		This bit gets loaded into EU CR0.1[12] (note the bit # difference). See Exceptions and ISA Execution Environment.		
	12	Software Exception Enable		
		Format:		Enable
		This bit gets loaded into EU CRO1[13] (note the bit # difference). See Exceptions and ISA Execution Environment.		
	11:8	Reserved		
		Format:		MBZ
	7:0	Reserved		



3DSTATE_HS			
2		Format:	MBZ
	31	Enable	
		Format:	Enable
		Specifies whether the HS function is enabled or disabled (pass-through). If ENABLED MI_TOPOLOGY_FILTER must be used to silently discard any topologies that the HS kernel is not expecting. E.g., if the HS kernel is expecting PATCHLIST_32 topologies, MI_TOPOLOGY_FILTER must be set to PATCHLIST_32 so only those topologies can reach the enabled HS.	
		Programming Notes	
		The tessellation stages (HS, TE and DS) must be enabled/disabled as a group. I.e., draw commands can only be issued if all three stages are enabled or all three stages are disabled, otherwise the behavior is UNDEFINED.	
	30	Reserved	
		Format:	MBZ
	29	Statistics Enable	
		Format:	Enable
		This bit controls whether HS-unit-specific statistics register(s) will increment (for each patch).	
	28:27	Reserved	
		Format:	MBZ
	26:18	Reserved	
		Format:	MBZ
	17	Reserved	
		Format:	MBZ
	16:8	Maximum Number of Threads	
		Format:	U9-1
		Specifies the maximum number of simultaneous threads allowed to be active. Used to avoid using up the scratch space. Programming the value of the max threads over the number of threads based off number of threads supported in the execution units may improve performance since the architecture allows threads to be buffered between the check for max threads and the actual dispatch into the EU. Programming the max values to a number less than the number of threads supported in the execution units may reduce performance.	
		Value	Name
		[0,335]	indicating thread count of [1,336]
	7:5	Reserved	
		Format:	MBZ
	4	Reserved	
		Format:	MBZ
	3:0	Instance Count	
		Format:	U4-1



3DSTATE_HS										
		This field determines the number of threads (minus one) spawned per input patch. If the HS kernel uses a barrier function, software must restrict the Instance Count to the number of threads that can be simultaneously active within a subslice. Factors which must be considered includes scratch memory availability. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[0,15]</td><td></td><td>representing [1,16] instances</td></tr></table> Programming Notes Instance Count must be programmed to 0 (1 instance) whenever DispatchMode is programmed to DUAL_PATCH. A pipe_control with cs stall must be sent whenever the HS_STATE.InstanceCount changes from 0 (no instancing) to >0 (instancing) or when there is transition from HS_STATE.Enabled = false to (HS_STATE.Enabled = true && InstanceCount > 0).	Value	Name	Description	[0,15]		representing [1,16] instances		
Value	Name	Description								
[0,15]		representing [1,16] instances								
3..4	63:6	Kernel Start Pointer <table><tr><td>Format:</td><td>InstructionBaseOffset[63:6]Kernel</td></tr></table> This field specifies the starting location (1st GEN core instruction) of the kernel program run by threads spawned by this FF unit. It is specified as a 64-byte-granular offset from the Instruction Base Address.	Format:	InstructionBaseOffset[63:6]Kernel						
Format:	InstructionBaseOffset[63:6]Kernel									
	5:0	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ						
Format:	MBZ									
5..6	63:10	Scratch Space Base Pointer <table><tr><td>Format:</td><td>GeneralStateOffset[63:10]</td></tr></table> <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[0,31]</td><td></td><td>Specifies the location of the scratch space area allocated to this FF unit, specified as a 1KB-granular offset from the General State Base Address. If required, each thread spawned by this FF unit will be allocated some portion of this space, as specified by Per-Thread Scratch Space.</td></tr></table>	Format:	GeneralStateOffset[63:10]	Value	Name	Description	[0,31]		Specifies the location of the scratch space area allocated to this FF unit, specified as a 1KB-granular offset from the General State Base Address. If required, each thread spawned by this FF unit will be allocated some portion of this space, as specified by Per-Thread Scratch Space.
Format:	GeneralStateOffset[63:10]									
Value	Name	Description								
[0,31]		Specifies the location of the scratch space area allocated to this FF unit, specified as a 1KB-granular offset from the General State Base Address. If required, each thread spawned by this FF unit will be allocated some portion of this space, as specified by Per-Thread Scratch Space.								
	9:4	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ						
Format:	MBZ									
	3:0	Per-Thread Scratch Space <table><tr><td>Format:</td><td>U4 power of 2 Bytes over 1K Bytes</td></tr></table> Specifies the amount of scratch space to be allocated to each thread spawned by this FF unit. The driver must allocate enough contiguous scratch space, starting at the Scratch Space Base Pointer, to ensure that the Maximum Number of Threads can each get Per-Thread Scratch Space size without exceeding the driver-allocated scratch space. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[0,11]</td><td></td><td>Indicating[1K Bytes, 2M Bytes</td></tr></table>	Format:	U4 power of 2 Bytes over 1K Bytes	Value	Name	Description	[0,11]		Indicating[1K Bytes, 2M Bytes
Format:	U4 power of 2 Bytes over 1K Bytes									
Value	Name	Description								
[0,11]		Indicating[1K Bytes, 2M Bytes								
7	31:29	Reserved								



3DSTATE_HS

		Format:	MBZ
28	Dispatch GRF Start Register For URB Data [5]		
		Format:	U1
	Specifies bit [5] of the starting GRF register number for the URB portion (Constant + Vertices) of the thread payload. The Dispatch GRF Start Register For URB Data [4:0] field is used to specify bits [4:0] of the starting GRF register number.		
27	Single Program Flow		
		Format:	Enable
	Specifies the initial condition of the kernel program as either a single program flow (SIMD _n x _m with $m = 1$) or as multiple program flows (SIMD _n x _m with $m > 1$). See CR0 description in <i>ISA Execution Environment</i> .		
	Value	Name	Description
	0h	Reserved	
	1h	Enable	Single Program Flow Enabled
26	Vector Mask Enable		
		Format:	U1 Enumerated Type
	Upon subsequent HS thread dispatches, this bit is loaded into the EU's Vector Mask Enable (VME, cr0.0[3]) thread state. Refer to the EU documentation for the definition and use of VME state.		
	Value	Name	Description
	0h	Dmask	The EU will use the Dispatch Mask (supplied by the HS stage) for instruction execution.
	1h	Vmask	The EU will use the Vector Mask (derived from the Dispatch Mask) for instruction execution.
	Programming Notes		
	Under normal conditions SW shall specify DMask, as the HS stage will provide a Dispatch Mask appropriate to SIMD4x2 or SIMD8 thread execution (as a function of dispatch mode). E.g., for SIMD4x2 thread execution, the HS state will generate a Dispatch Mask that is equal to what the EU would use as a Vector Mask. For SIMD8 execution there is no known usage model for use of Vector Mask (as there is for PS shaders).		
25	Accesses UAV		
		Format:	Enable
	This field must be set when HS has a UAV access		
	Programming Notes		
	This field must not be set when HS Function Enable is disabled.		
24	Include Vertex Handles		
		Format:	Boolean
	If set, all the input Vertex URB handles are included in payloads.		



3DSTATE_HS			
		This field is ignored if HS Function Enable is DISABLED. Programming Notes Programming Restriction: This field must be set if value if Vertex URB Entry Read Length is cleared to zero.	
23:19	Dispatch GRF Start Register For URB Data		
	Format:	U5	
	Specifies the starting GRF register number for the URB portion (Constant + Vertices) of the thread payload.		
	This field is ignored if HS Function Enable is DISABLED.		
	Value	NameDescription	
	[0,31]		indicating GRF [R0, R31]
18:17	Dispatch Mode		
	Format:	U2	
	This field is unused to set the current thread dispatch mode for the HS stage.		
	Value	NameDescription	
	0h	SINGLE_PATCH	HS threads are passed inputs and an output handle associated with a single input patch.
	1h	DUAL_PATCH	HS threads are passed inputs and an output handle associated with (up to) two input patches. Patch 0 data is passed in the four lower channels while Patch 1 data (if present) is passed in the four upper channels. Restrictions: Only valid for 4 or fewer input control points (PATCHLIST_4 and below). SW is expected to use MI_TOPOLOGY_FILTER to ensure only patches with the expected # of ICPs are processed by the pipeline when HS is enabled.
2h	8_PATCH	HS threads are passed inputs and an output handle associated with (up to) 8 patches in SIMD8 fashion. See 8_PATCH Thread Payload.	
	3h	Reserved	



3DSTATE_HS			
	16:11	Vertex URB Entry Read Length Format: U6 Specifies the amount of URB data read and passed in the thread payload <u>for each Vertex URB entry</u>, in 256-bit register increments. This field is ignored if HS Function Enable is DISABLED. Value Name [0,63] Programming Notes Programming Restriction: This field must be a non-zero value if Include Vertex Handles is cleared to zero.	
	10	Reserved Format: MBZ	
	9:4	Vertex URB Entry Read Offset Format: U6 Specifies the offset (in 256-bit units) at which Vertex URB data is to be read from the URB before being included in the thread payload. This offset applies to all Vertex URB entries passed to the thread. This field is ignored if HS Function Enable is DISABLED. Value Name [0,63]	
	3:1	Reserved Format: MBZ	
	0	Include Primitive ID Format: Enable If set, R1 of the payload is written with Primitive ID value(s). If clear, these Primitive IDs are not included in the payload R1. Programming Notes This field is only used when DUAL_PATCH DispatchMode is specified. In SINGLE_PATCH, the single Primitive ID is always passed in R0.	
	8	31:0	Reserved Format: MBZ



3DSTATE_URB_DS

3DSTATE_URB_DS			
Source:		RenderCS	
Length Bias:		2	
Description			
This command may not overlap with the push constants in the URB defined by the 3DSTATE_PUSH_CONSTANT_ALLOC_VS, 3DSTATE_PUSH_CONSTANT_ALLOC_DS, 3DSTATE_PUSH_CONSTANT_ALLOC_HS, and 3DSTATE_PUSH_CONSTANT_ALLOC_GS commands. The URB Starting Address and Number of URB Entries fields shall be programmed as if there is only one slice enabled. When more than one slice is enabled, hardware will (a) recompute the actual URB Starting Address based on the number of enabled slices and (b) multiply the Number of URB Entries by the number of enabled slices. Software shall ensure that the values programmed do not exceed the URB capacity of a single slice. Refer to the L3 allocation and programming guide for valid URB configurations.			
Programming Notes			
When programming DS URB state for the RCS 3D pipe, 3DSTATE_URB_VS, 3DSTATE_URB_HS, and 3DSTATE_URB_GS must also be programmed in order for the programming of this state to be valid.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	Command SubType	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	3D Command Opcode	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	3D Command Sub Opcode	
		Default Value:	32h 3DSTATE_URB_DS
		Format:	OpCode
	15:8	Reserved	
		Format:	MBZ
	7:0	DWord Length	
		Default Value:	0h DWORD_COUNT_n
		Format:	=n



3DSTATE_URB_DS

1	31:25	DS URB Starting Address	
		Format:	U7
		Offset from the start of the URB memory where DS starts its allocation, specified in multiples of 8 KB.	
	24:16	DS URB Entry Allocation Size	
		Format:	U9-1 Count of 512-bit units
		Specifies the length of each URB entry owned by DS. This field is always used (even if DS Function Enable is DISABLED).	
	15:0	DS Number of URB Entries	
		Description	
		Specifies the number of URB entries that are used by DS, based on only 1 slice enabled. When multiple slices are enabled, HW will multiply the value programmed by the number of slices in order to determine the total number of entries. SW shall ensure that the total number of entries does not exceed the relevant ValidValue range listed below. This field is always used (even if DS Function Enable is DISABLED).	
		If Domain Shader Thread Dispatch is Enabled then the minimum number of handles that must be allocated is 34 URB entries.	



3DSTATE_URB_GS

3DSTATE_URB_GS			
Source:	RenderCS		
Length Bias:	2		
Description			
This command may not overlap with the push constants in the URB defined by the 3DSTATE_PUSH_CONSTANT_ALLOC_VS, 3DSTATE_PUSH_CONSTANT_ALLOC_DS, 3DSTATE_PUSH_CONSTANT_ALLOC_HS, and 3DSTATE_PUSH_CONSTANT_ALLOC_GS commands.			
The URB Starting Address and Number of URB Entries fields shall be programmed as if there is only one slice enabled. When more than one slice is enabled, hardware will (a) recompute the actual URB Starting Address based on the number of enabled slices and (b) multiply the Number of URB Entries by the number of enabled slices. Software shall ensure that the values programmed do not exceed the URB capacity of a single slice. Refer to the L3 allocation and programming guide for valid URB configurations			
Programming Notes			
When programming GS URB state for the RCS 3D pipe, 3DSTATE_URB_VS, 3DSTATE_URB_HS, and 3DSTATE_URB_DS must also be programmed in order for the programming of this state to be valid.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	Command SubType	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	3D Command Opcode	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	3D Command Sub Opcode	
		Default Value:	33h 3DSTATE_URB_GS
		Format:	OpCode
	15:8	Reserved	
		Format:	MBZ
	7:0	DWord Length	
		Default Value:	0h DWORD_COUNT_n
		Format:	=n



3DSTATE_URB_GS											
1	31:25	GS URB Starting Address									
		Format:U7									
		Offset from the start of the URB memory where GS starts its allocation, specified in multiples of 8 KB.									
		<table><tr><th>Value</th><th>Name</th><th>Exists If</th></tr><tr><td>[0,48]</td><td></td><td>Device[SliceCount] == 1</td></tr><tr><td>[4,48]</td><td></td><td>Device[SliceCount] GT 1</td></tr></table>	Value	Name	Exists If	[0,48]		Device[SliceCount] == 1	[4,48]		Device[SliceCount] GT 1
		Value	Name	Exists If							
	[0,48]		Device[SliceCount] == 1								
	[4,48]		Device[SliceCount] GT 1								
	24:16	GS URB Entry Allocation Size									
		Format:U9-1 512-bit units									
		Specifies the length of each URB entry owned by GS. This field is always used (even if GS Function Enable is DISABLED).									
15:0	GS Number of URB Entries										
	Specifies the number of URB entries that are used by GS, based on only 1 slice enabled. When multiple slices are enabled, HW will multiply the value programmed by the number of slices in order to determine the total number of entries. SW shall ensure that the total number of entries does not exceed the relevant ValidValue range listed below. This field is always used (even if GS Function Enable is DISABLED).										
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>[0,256]</td><td></td></tr></table>	Value	Name	[0,256]							
	Value	Name									
	[0,256]										
	Programming Notes										
	Only if GS is disabled can this field be programmed to 0. If GS is enabled this field shall be programmed to a value greater than 0. For GS Dispatch Mode "Single", this field shall be programmed to a value greater than or equal to 1. For other GS Dispatch Modes, refer to the definition of Dispatch Mode (3DSTATE_GS) for minimum values of this field.										
	GS Number of URB Entries must be divisible by 8 if the GS URB Entry Allocation Size is less than 9 512-bit URB entries. "2:0" = reserved "000"										
When 3DSTATE_GS:Enable is true, the minimum number of GS Number of URB Entries must be set to 2.											



3DSTATE_URB_HS

3DSTATE_URB_HS			
Source:	RenderCS		
Length Bias:	2		
Description			
This command may not overlap with the push constants in the URB defined by the 3DSTATE_PUSH_CONSTANT_ALLOC_VS, 3DSTATE_PUSH_CONSTANT_ALLOC_DS, 3DSTATE_PUSH_CONSTANT_ALLOC_HS, and 3DSTATE_PUSH_CONSTANT_ALLOC_GS commands. The URB Starting Address and Number of URB Entries fields shall be programmed as if there is only one slice enabled. When more than one slice is enabled, hardware will (a) recompute the actual URB Starting Address based on the number of enabled slices and (b) multiply the Number of URB Entries by the number of enabled slices. Software shall ensure that the values programmed do not exceed the URB capacity of a single slice. Refer to the L3 allocation and programming guide for valid URB configurations			
Programming Notes			
When programming HS URB state for the RCS 3D pipe, 3DSTATE_URB_VS, 3DSTATE_URB_DS, and 3DSTATE_URB_GS must also be programmed in order for the programming of this state to be valid.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	Command SubType	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	3D Command Opcode	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	3D Command Sub Opcode	
		Default Value:	31h 3DSTATE_URB_HS
		Format:	OpCode
	15:8	Reserved	
		Format:	MBZ
	7:0	DWord Length	
		Default Value:	0h DWORD_COUNT_n
		Format:	=n



3DSTATE_URB_HS					
1	31:25	HS URB Starting Address			
		Format:	U7		
		Offset from the start of the URB memory where HS starts its allocation, specified in multiples of 8 KB.			
		Value	Name	Exists If	
		[0,48]		Device[SliceCount] == 1	
			[4,48]		Device[SliceCount] GT 1
	24:16	HS URB Entry Allocation Size			
		Format:	U9-1 Count of 512-bit units		
		Specifies the length of each URB entry owned by HS. This field is always used (even if HS Function Enable is DISABLED).			
	15:0	HS Number of URB Entries			
Specifies the number of URB entries that are used by HS, based on only 1 slice enabled. When multiple slices are enabled, HW will multiply the value programmed by the number of slices in order to determine the total number of entries. SW shall ensure that the total number of entries does not exceed the relevant ValidValue range listed below.					
This field is always used (even if HS Function Enable is DISABLED).					
Programming Restriction:HS Number of URB Entries must be divisible by 8 if the HS URB Entry Allocation Size is less than 9 512-bit URB entries."2:0" = reserved "000"					
Value		Name			
[0,256]					
Programming Notes					
When 3DSTATE_HS:Enable is true and 3DSTATE_HS:Dispatch Mode is set to 8 patch, the minimum number of HS Number of URB Entries must be set to 16. When 3DSTATE_HS:Enable is true and 3DSTATE_HS:Dispatch Mode is set to dual patch, the minimum number of HS Number of URB Entries must be set to 4.					



3DSTATE_URB_VS

3DSTATE_URB_VS			
Source:	RenderCS, PositionCS		
Length Bias:	2		
Description			
VS URB Entry Allocation Size equal to 4(5 512-bit URB rows) may cause performance to decrease due to banking in the URB. Element sizes of 16 to 20 should be programmed with six 512-bit URB rows.			
This command may not overlap with the push constants in the URB defined by the 3DSTATE_PUSH_CONSTANT_ALLOC_VS, 3DSTATE_PUSH_CONSTANT_ALLOC_DS, 3DSTATE_PUSH_CONSTANT_ALLOC_HS, and 3DSTATE_PUSH_CONSTANT_ALLOC_GS commands.			
The offset and size should be programmed as if there is only one slice enabled. Hardware will grow the size based on the slice configuration. Software shall ensure that the values programmed do not exceed the URB capacity of one slice. Refer to the L3 allocation and programming guide for valid URB configurations.			
Programming Notes			
When programming VS URB state for the RCS 3D pipe, 3DSTATE_URB_HS, 3DSTATE_URB_DS, and 3DSTATE_URB_GS must also be programmed in order for the programming of this state to be valid.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	Command SubType	
		Default Value:	3h GFXPIPE_3D
		Format:	OpCode
	26:24	3D Command Opcode	
		Default Value:	0h 3DSTATE_PIPELINED
		Format:	OpCode
	23:16	3D Command Sub Opcode	
		Default Value:	30h 3DSTATE_URB_VS
		Format:	OpCode
	15:8	Reserved	
		Format:	MBZ
	7:0	DWord Length	
		Default Value:	0h DWORD_COUNT_n
		Format:	=n



3DSTATE_URB_VS											
1	31:25	VS URB Starting Address									
		Format: U7									
		Offset from the start of the URB memory where VS starts its allocation, specified in multiples of 8 KB.									
		<table><tr><th>Value</th><th>Name</th><th>Exists If</th></tr><tr><td>[0,48]</td><td></td><td>Device[SliceCount] == 1</td></tr><tr><td>[4,48]</td><td></td><td>Device[SliceCount] GT 1</td></tr></table>	Value	Name	Exists If	[0,48]		Device[SliceCount] == 1	[4,48]		Device[SliceCount] GT 1
		Value	Name	Exists If							
[0,48]		Device[SliceCount] == 1									
[4,48]		Device[SliceCount] GT 1									
24:16	VS URB Entry Allocation Size										
	Format: U9-1 count of 512-bit units										
	Specifies the length of each URB entry owned by VS. This field is always used (even if VS Function Enable is DISABLED).										
	Programming Notes										
	Programming Restriction: As the VS URB entry serves as both the per-vertex input and output of the VS shader, the VS URB Allocation Size must be sized to the maximum of the vertex input and output structures.										
	15:0	VS Number of URB Entries									
		Format: U16									
		Specifies the number of URB entries that are used by VS, based on only 1 slice enabled. When multiple slices are enabled, HW will multiply the value programmed by the number of slices in order to determine the total number of entries. SW shall ensure that the total number of entries does not exceed the relevant ValidValue range listed below. This field is always used (even if VS Function Enable is DISABLED).									
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>[34,704]</td><td></td></tr></table>	Value	Name	[34,704]						
		Value	Name								
[34,704]											
Programming Notes											
	Programming Restriction: VS Number of URB Entries must be divisible by 8 if the VS URB Entry Allocation Size is less than 9 512-bit URB entries."2:0" = reserved "000b"										



HCP_BSD_OBJECT

HCP_BSD_OBJECT			
Source:		VideoCS	
Length Bias:		2	
The HCP is selected with the Media Instruction Opcode "7h" for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16. The HCP_BSD_OBJECT command fetches the HEVC bit stream for a slice starting with the first byte in the slice. The bit stream ends with the last non-zero bit of the frame and does not include any zero-padding at the end of the bit stream. There can be multiple slices in a HEVC frame and thus this command can be issued multiple times per frame. The HCP_BSD_OBJECT command must be the last command issued in the sequence of batch commands before the HCP starts decoding. Prior to issuing this command, it is assumed that all configuration parameters in the HCP have been loaded including workload configuration registers and configuration tables. When this command is issued, the HCP is waiting for bit stream data to be presented to the shift register.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	Pipeline Type	
		Default Value:	2h
		Format:	OpCode
	26:23	Media Instruction Opcode	
		Default Value:	7h Codec/Engine Name
		Format:	OpCode
		Codec/Engine Name = HCP = 7h	
	22:16	Media Instruction Command	
		Default Value:	20h HCP_BSD_OBJECT_STATE
		Format:	OpCode
	15:12	Reserved	
		Format:	MBZ
	11:0	Dword Length	
		Format:	=n
		(Excludes Dwords 0, 1).	
		Value	Name
1h			



HCP_BSD_OBJECT						
1	31:0	Indirect BSD Data Length				
		Format: U32				
		Specifies the length in bytes of the bitstream data for the current slice. It includes the first byte of the slice and the last non-zero byte of the in the slice. Specifically, the zero-padding bytes (if present) and the next start-code are excluded.				
		<table> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>[268435456,2147483547]</td><td>Data_Length_beyond_28_bits</td><td>This is an added valid range when the bit length is extended from 28 bits to 32 bits. This is added to support 16k x 16k picture size bitstream.</td></tr> </table>	Value	Name	Description	[268435456,2147483547]
Value	Name	Description				
[268435456,2147483547]	Data_Length_beyond_28_bits	This is an added valid range when the bit length is extended from 28 bits to 32 bits. This is added to support 16k x 16k picture size bitstream.				
2	31:29	Reserved				
		Format: MBZ				
	28:0	Indirect Data Start Address Format: U29 Specifies the byte-aligned graphics memory starting address of the slice bit stream relative to the BSD Indirect Object Base Address .				



HCP_PIC_STATE

HCP_PIC_STATE			
Source:		VideoCS	
Length Bias:		2	
The HCP is selected with the Media Instruction Opcode "7h" for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16.			
This is a picture level command and is issued only once per workload for both encoding and decoding processes.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	Pipeline Type	
		Default Value:	2h
		Format:	OpCode
	26:23	Media Instruction Opcode	
		Default Value:	7h Codec/Engine Name
		Format:	OpCode
		Codec/Engine Name = HCP = 7h	
	22:16	Media Instruction Command	
		Default Value:	10h HCP_PIC_STATE
		Format:	OpCode
	15:12	Reserved	
		Format:	MBZ
	11:0	Dword Length	
		Format:	=n
		(Excludes Dwords 0, 1).	
Value		Name	
11h			
1	31:26	Reserved	
		Format:	MBZ
	25:16	FrameHeightInMinCbMinus1	
		Format:	U10
		Specifies the height of each decoded picture in units of minimum coding block size.	
		Value	Name
[0-4122]			



HCP_PIC_STATE																		
		<table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">The decoded picture height in units of luma samples equals (FrameHeightInMinCbMinus1 + 1) * (1 « (log2_min_coding_block_size_minus3 + 3)) </td></tr><tr><td colspan="2">In HEVC Encoder mode, the following restrictions apply. Note : for a frame height that is not an integer multiple of LCU : Kernel : on last LCU at frame's bottom edge, it must align to CU boundary. This applies to all size of LCU: 16x16, 32x32, 64x64. Kernel does not count/include CUs outside of the picture in PakObj/CU_record respectively. Driver : sets up a LCU aligned (both in X/Y direction) surface.</td></tr></table>	Programming Notes		The decoded picture height in units of luma samples equals (FrameHeightInMinCbMinus1 + 1) * (1 « (log2_min_coding_block_size_minus3 + 3))		In HEVC Encoder mode, the following restrictions apply. Note : for a frame height that is not an integer multiple of LCU : Kernel : on last LCU at frame's bottom edge, it must align to CU boundary. This applies to all size of LCU: 16x16, 32x32, 64x64. Kernel does not count/include CUs outside of the picture in PakObj/CU_record respectively. Driver : sets up a LCU aligned (both in X/Y direction) surface.											
	Programming Notes																	
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	15	Reserved																
	14:10	<table><tr><td>Reserved</td><td></td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>	Reserved		Format:	MBZ												
	Reserved																	
	Format:	MBZ																
	9:0	<table><tr><td>FrameWidthInMinCbMinus1</td><td></td></tr><tr><td>Format:</td><td>U10</td></tr><tr><td colspan="2">Specifies the width of each decoded picture in units of minimum coding block size.</td></tr><tr><td>Value</td><td>Name</td></tr><tr><td>[0-4122]</td><td></td></tr><tr><td colspan="2">Programming Notes</td></tr><tr><td colspan="2">The decoded picture width in units of luma samples equals (FrameWidthInMinCbMinus1 + 1) * (1 « (log2_min_coding_block_size_minus3 + 3)) </td></tr></table>	FrameWidthInMinCbMinus1		Format:	U10	Specifies the width of each decoded picture in units of minimum coding block size.		Value	Name	[0-4122]		Programming Notes		The decoded picture width in units of luma samples equals (FrameWidthInMinCbMinus1 + 1) * (1 « (log2_min_coding_block_size_minus3 + 3))			
	FrameWidthInMinCbMinus1																	
Format:	U10																	
Specifies the width of each decoded picture in units of minimum coding block size.																		
Value	Name																	
[0-4122]																		
Programming Notes																		
The decoded picture width in units of luma samples equals (FrameWidthInMinCbMinus1 + 1) * (1 « (log2_min_coding_block_size_minus3 + 3))																		
2	15	<table><tr><td>Reserved</td><td></td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>	Reserved		Format:	MBZ												
Reserved																		
Format:	MBZ																	
	31:12	<table><tr><td>Reserved</td><td></td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>	Reserved		Format:	MBZ												
Reserved																		
Format:	MBZ																	
	11:10	<table><tr><td>MaxPCMSize</td><td></td></tr><tr><td>Format:</td><td>U2</td></tr><tr><td colspan="2">Specifies the largest allowed PCM coding block size.</td></tr><tr><td>Value</td><td>Name</td></tr><tr><td>3</td><td>Reserved</td></tr><tr><td>2</td><td>32x32</td></tr><tr><td>1</td><td>16x16</td></tr><tr><td>0</td><td>8x8</td></tr></table>	MaxPCMSize		Format:	U2	Specifies the largest allowed PCM coding block size.		Value	Name	3	Reserved	2	32x32	1	16x16	0	8x8
MaxPCMSize																		
Format:	U2																	
Specifies the largest allowed PCM coding block size.																		
Value	Name																	
3	Reserved																	
2	32x32																	
1	16x16																	
0	8x8																	



HCP_PIC_STATE

HCP_PIC_STATE			
	9:8	MinPCMSize	
		Format: U2	
		Specifies the smallest allowed PCM coding block size.	
		Value	Name
		3	Reserved
		2	32x32
		1	16x16
		0	8x8
	7:6	MaxTUSize	
		Format: U2	
		Specifies the largest allowed transform block size.	
		Value	Name
		3	32x32
		2	16x16
		1	8x8
		0	4x4
	5:4	MinTUSize	
		Format: U2	
		Specifies the smallest allowed transform block size.	
		Value	Name
3		32x32	
2		16x16	
1		8x8	
0		4x4	
3:2	CtbSize (LCUSize)		
	Format: U2		
	Specifies the coding tree block size.		
	Value	Name	Programming Notes
	3	64x64	
	2	32x32	
	1	16x16	
	0	illegal/reserved	
	Programming Notes		
	LCU is restricted based on the picture size.		
1:0	MinCUSize		



HCP_PIC_STATE			
		Format: U2	
		Specifies the smallest coding block size.	
		Value	Name
		3	64x64
		2	32x32
		1	16x16
		0	8x8
3	31:3	Reserved	
		Format: MBZ	
	2	InsertTestFlag	
		Format: U1	
		Value	Name
		0h	[Default]
		1h	
		Programming Notes	
		CABAC 0 Word Insertion Test Enable (Encoder Only)This bit will modify CABAC K equation so that a positive K value can be generated easily. This is done for validation purpose only. In normal usage this bit should be set to 0. Regular equation for generating 'K' value when CABAC 0 Word Insertion Test Enable is set to 0. $K = \{ [((96 * pic\_bin\_count()) - (RawMinCUBits * PicSizeInMinCUs * 3) + 1023) / 1024] - bytes\_in\_picture \} / 3$ Modified equation when CABAC 0 Word Insertion Test Enable bit set to 1. $K = \{ [((1536 * pic\_bin\_count()) - (RawMinCUBits * PicSizeInMinCUs * 3) + 1023) / 1024] - bytes\_in\_picture \} / 3$ Encoder only feature.	
		This bit should be set to 0 in regular PAK mode.	



HCP_PIC_STATE				
	1	CurPicIsl		
		Format: U1		
		Specifies that the current picture is comprised solely of I slices and that there are no P or B slices in the picture.		
		Value	Name	
		0	Current picture has at least one P or B slice	
		Programming Notes		
	This bit should be set to "0". Note: The value of "1" setting ("Current picture is comprised solely of I slices") is REMOVED. This bit is used for hardware optimization only. There is not enough information to set this bit to "1" correctly.			
	0	ColPicIsl		
		Format: U1		
		Specifies that the collocated picture is comprised solely of I slices and that there are no P or B slices in the picture.		
Value		Name		
0		Collocated picture has at least one P or B slice		
Programming Notes				
This bit should be set to "0". Note: The value of "1" setting ("Collocated picture is comprised solely of I slices") is REMOVED. This bit is used for hardware optimization only. There is not enough information to set this bit to "1" correctly.				
4	31:28	Reserved		
		Format: MBZ		
	26	strong_intra_smoothing_enable_flag		
		Format: U1		
	25	transquant_bypass_enable_flag		
		Format: Enable		
		Value	Name	Description
		0	Disable	cu_transquant_bypass is not supported
		1	Enable	cu_transquant_bypass is supported
	24	Reserved		
Format: MBZ				



HCP_PIC_STATE

HCP_PIC_STATE					
	23	amp_enabled_flag			
		Format: Enable			
		Value	Name Description		
		0	Disable	Asymmetric motion partitions cannot be used in coding tree blocks.	
	22	transform_skip_enabled_flag	Format: Enable		
			Value	Name Description	
			0	Disable	transform_skip_flag is not supported in the residual coding
			1	Enable	transform_skip_flag is supported
	21	BottomField	Format: U1		
			Value	Name Description	
			0	Bottom Field	
			1	Top Field	
Programming Notes					
Must be zero for encoder only					
20			FieldPic	Format: U1	
	Value	Name Description			
	0	Video Frame			
	1	Video Field			
	Programming Notes				
	Must be zero for encoder only.				
	19	weighted_pred_flag		Format: U1	
18	weighted_bipred_flag	Format: U1			
17	tiles_enabled_flag				

**HCP_PIC_STATE**

		Format:	U1
		Programming Notes	
		Tiling is not supported and this bit should be set to 0.	
	16	entropy_coding_sync_enabled_flag	
		Format:	U1
		Not used in encoder mode	
	15	Reserved	
	15	loop_filter_across_tiles_enabled_flag	
		Format:	U1
	14	Reserved	
		Format:	MBZ
	13	sign_data_hiding_flag	
		Format:	Enable
		Value	Name
		0	Disable
		1	Enable
		Description	
		Specifies that sign bit hiding is disabled.	
		Specifies that sign bit hiding is enabled.	
		Programming Notes	
		Currently not supported in encoder, so must be set to 0 for encoding session.	
	12:10	log2_parallel_merge_level_minus2	
		Format:	U3
		Value	Name
		[0,4]	Valid Range
		The value of log2_parallel_merge_level_minus2 shall be in the range of 0 to Log2CtbSizeYCtbLog2SizeY - 2, inclusive.	
		Programming Notes	
		For encoder, always set to 0 (Intel restriction).	
	9	constrained_intra_pred_flag	
		Format:	U1
	8	pcm_loop_filter_disable_flag	
		Format:	U1
	7:6	diff_cu_qp_delta_depth (or named as max_dqp_depth)	



HCP_PIC_STATE				
5		Format: U2		
		Programming Notes		
		cu_qp_delta_enabled_flag/max_dqp_depth: 1/0: has cu qp delta. (cu depth <= max_dqp_depth) will have cu qp delta coded. Only allow QP change across Slices, no change across LCU or CU.		
	5	cu_qp_delta_enabled_flag		
		Format: U1		
		Value	Name	Description
		0	Disable	Does not allow QP change at CU or LCU level, the same QP is used for the entire slice. Max_DQP_Level = 0 (i.e. diff_cu_qp_delta_depath = 0).
		1	Enable	Allow QP change at CU level. MAX_DQP_level can be >0.
	4	pcm_enabled_flag		
		Format: U1		
3	sample_adaptive_offset_enabled_flag			
	Format: U1			
2:0	Reserved			
	Format: MBZ			
5	31:30	Reserved		
		Format: MBZ		
	29:27	bit_depth_luma_minus8		
		Format: U3		
		This specifies the number of bit allow for Luma pixels. In 8 bit mode, this must be set to 0. Encoder: Supports bit depths 8, 10 and 12 only. Encoder: Does not support 10 or 12 bit Source Pixels and 8bit PAK i.e. the source pixel depth should be less than or equal to PAK bit depth.		
		Value	Name	Description
		0	luma_8bit	
		1	luma_9bit	Only HEVC decoder supports 9 bits luma. HEVC encoder does not supports 9 bits luma.
		2	luma_10bit	
		3	luma_11bit	
	4	luma_12bit		
26:24	bit_depth_chroma_minus8			

**HCP_PIC_STATE**

HCP_PIC_STATE				
		Format: U3		
		This specifies the number of bit allow for Chroma pixels. In 8 bit mode, this must be set to 0. Encoder: Supports bit depths 8, 10 and 12 only. And also it must be same as Luma. Encoder: Does not support 10 or 12 bit Source Pixels and 8bit PAK. i.e. The source pixel depth should be less than or equal to the PAK bit depth.		
		Value	Name	Description
		0	chroma_8bit	
		1	chroma_9bit	Only HEVC decoder supports 9 bits chroma. HEVC encoder does not supports 9 bits chroma.
		2	chroma_10bit	
		3	chroma_11bit	
		4	chroma_12bit	
	23:20	pcm_sample_bit_depth_luma_minus1		
		Format: U4		
	19:16	pcm_sample_bit_depth_chroma_minus1		
		Format: U4		
	15:13	max_transform_hierarchy_depth_inter(or named as tu_max_depth_inter)		
		Format: U3		
		Maximum TU split depths for inter blocks		
	Programming Notes			
	For encoder, always set to 2 to allow max 2 levels of split. For more splitting rely on CU split to match the content (Intel restriction)			
12:10	max_transform_hierarchy_depth_intra (or named as tu_max_depth_intra)			
	Format: U3			
	Maximum TU split depth for intra blocks.			
	Programming Notes			
	For encoder, always set to 2 to allow max 2 levels of split. For more splitting, rely on CU split to match the content (Intel restriction).			
9:5	pic_cr_qp_offset			
	Format: S4			
	Valid range -12 to +12			
4:0	pic_cb_qp_offset			
	Format: S4			
	Valid range -12 to +12			
6	31:30	Reserved		
		Format: MBZ		
	29	Load Slice Pointer Flag		



HCP_PIC_STATE

		<table><tr><td>Format:</td><td>Enable</td></tr></table> LoadBitStreamPointerPerSlice (Encoder-only) To support multiple slice picture and additional header/data insertion before and after an encoded slice. When this field is set to 0, bitstream pointer is only loaded once for the first slice of a frame. For subsequent slices in the frame, bitstream data are stitched together to form a single output data stream. When this field is set to 1, bitstream pointer is loaded for each slice of a frame. Basically bitstream data for different slices of a frame will be written to different memory locations. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>Disable</td><td>Load BitStream Pointer only once for the first slice of a frame.</td></tr><tr><td>1</td><td>Enable</td><td>Load/reload BitStream Pointer only once for the each slice, reload the start location of the bitstream buffer from the Indirect PAK-BSE Object Data Start Address field.</td></tr></table> <table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">Must be zero for encoder</td></tr></table>	Format:	Enable	Value	Name	Description	0	Disable	Load BitStream Pointer only once for the first slice of a frame.	1	Enable	Load/reload BitStream Pointer only once for the each slice, reload the start location of the bitstream buffer from the Indirect PAK-BSE Object Data Start Address field.	Programming Notes		Must be zero for encoder	
	Format:	Enable															
	Value	Name	Description														
	0	Disable	Load BitStream Pointer only once for the first slice of a frame.														
	1	Enable	Load/reload BitStream Pointer only once for the each slice, reload the start location of the bitstream buffer from the Indirect PAK-BSE Object Data Start Address field.														
	Programming Notes																
	Must be zero for encoder																
	28:27	Reserved															
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ													
	Format:	MBZ															
26	FrameSzUnderStatusEn - FrameBitRateMinReportMask																
	<table><tr><td>Format:</td><td>Enable</td></tr></table> This is a mask bit controlling if the condition of frame level bit count is less than FrameBitRateMin. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>Disable</td><td>Do not update bit 2 (Frame Bit Count Violate -- under run) of HCP_IMAGE_STATUS control register. NOTE: This bit MUST BE set to zero for the last BRC pass if SAO first pass also enabled. This will ensure that HW picks up right accumulated deltaQP for SAO sencond pass.</td></tr><tr><td>1</td><td>Enable</td><td>Set bit 2 (Frame Bit Count Violate -- under run) of HCP_IMAGE_STATUS control register if the total frame level bit counter is less than or equal to Frame Bit Rate Minimum limit. HW does not use this bit to set the bit in HCP_IMAGE_STATUS_CONTROL register. It's used pass the bit in HCP_IMAGE_STATUS_MASK register</td></tr></table> <table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">Encoder Only</td></tr></table>	Format:	Enable	Value	Name	Description	0	Disable	Do not update bit 2 (Frame Bit Count Violate -- under run) of HCP_IMAGE_STATUS control register. NOTE: This bit MUST BE set to zero for the last BRC pass if SAO first pass also enabled. This will ensure that HW picks up right accumulated deltaQP for SAO sencond pass.	1	Enable	Set bit 2 (Frame Bit Count Violate -- under run) of HCP_IMAGE_STATUS control register if the total frame level bit counter is less than or equal to Frame Bit Rate Minimum limit. HW does not use this bit to set the bit in HCP_IMAGE_STATUS_CONTROL register. It's used pass the bit in HCP_IMAGE_STATUS_MASK register	Programming Notes		Encoder Only		
Format:	Enable																
Value	Name	Description															
0	Disable	Do not update bit 2 (Frame Bit Count Violate -- under run) of HCP_IMAGE_STATUS control register. NOTE: This bit MUST BE set to zero for the last BRC pass if SAO first pass also enabled. This will ensure that HW picks up right accumulated deltaQP for SAO sencond pass.															
1	Enable	Set bit 2 (Frame Bit Count Violate -- under run) of HCP_IMAGE_STATUS control register if the total frame level bit counter is less than or equal to Frame Bit Rate Minimum limit. HW does not use this bit to set the bit in HCP_IMAGE_STATUS_CONTROL register. It's used pass the bit in HCP_IMAGE_STATUS_MASK register															
Programming Notes																	
Encoder Only																	
25	FrameSzOverStatusEn - FrameBitRateMaxReportMask																
	<table><tr><td>Format:</td><td>Enable</td></tr></table> This is a mask bit controlling if the condition of frame level bit count exceeds FrameBitRateMax.	Format:	Enable														
Format:	Enable																

**HCP_PIC_STATE**

Value	Name	Description
0	Disable	Do not update bit 1 of HCP_IMAGE_STATUS control register. NOTE: This bit MUST BE set to zero for the last BRC pass if SAO first pass also enabled. This will ensure that HW picks up right accumulated deltaQP for SAO sencond pass.
1	Enable	Set bit 1 of HCP_IMAGE_STATUS control register if the total frame level bit counter is greater than or equal to Frame Bit Rate Maximum limit. HW does not use this bit to set the bit in HCP_IMAGE_STATUS_CONTROL register. It's used pass the bit inHCP_IMAGE_STATUS_MASK register
Programming Notes		
Encoder Only		

24	LCUMaxBitStatusEn - LCUMaxSizeReportMask	
Format:		Enable
This is a mask bit controlling if the condition of any LCU in the frame exceeds LCUMaxSize.		
Value	Name	Description
0	Disable	Do not update bit 0 of HCP_IMAGE_STATUS control register. NOTE: This bit MUST BE set to zero for the last BRC pass if SAO first pass also enabled. This will ensure that HW picks up right accumulated deltaQP for SAO second pass.
1	Enable	Set bit 0 of HCP_IMAGE_STATUS control register if the total bit counter for the current LCU is greater than the LCU Conformance Max size limit. HW does not use this bit to set the bit in HCP_IMAGE_STATUS_CONTROL register.
Programming Notes		
Encoder Only		

23:17	Reserved	
Format:		MBZ

16	NonFirstPassFlag	
Format:		Enable
This signals the current pass is not the first pass. It will imply designate HW behavior.		
Value	Name	Description
0	Disable	If it is initial-Pass, this bit is set to 0.
1	Enable	For subsequent passes, this bit is set to 1.



HCP_PIC_STATE												
		Programming Notes Encoder Only										
	15:0	LCU Max BitSize Allowed Format: U16 This field specifies the Max LCU Bit Size allowed in according to the spec conformance. However, driver can program a different value from the spec for other encoding purpose. If LCU Limit exceeds, LCUMaxBitStatus in MMIO would be set to 1 and also in CU Statistics Streamout, LCU Limit exceed field would be set to 1 at the last CU of a LCU Programming Notes Encoder Only										
		7 Programming Notes: Encoder Only	31 FrameBitrateMaxUnit Format: U1 This field is the Frame Bitrate Maximum Limit Units. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>Byte</td><td>32byte unit</td></tr><tr><td>1</td><td>Kilo Byte</td><td>4kbyte unit</td></tr></table> Programming Notes Encoder Only	Value	Name	Description	0	Byte	32byte unit	1	Kilo Byte	4kbyte unit
			Value	Name	Description							
			0	Byte	32byte unit							
			1	Kilo Byte	4kbyte unit							
30:14	Reserved Format: MBZ Reserved for future expansion of the Max Rate.											
	13:0	FrameBitRateMax Format: U14 This field is the Frame Bitrate Maximum Limit. This field along with FrameBitrateMaxUnit determines maximum allowed bits in a frame before multi-pass gets triggered (when enabled). In other words, multi-pass is triggered when the actual frame byte count exceeds this value. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0-512KB</td><td></td><td>The programmable range is 0-512KB when FrameBitrateMaxUnit is 0.</td></tr><tr><td>0-64MB</td><td></td><td>The programmable range is 0-64Mbyte when FrameBitrateMaxUnit is 1.</td></tr></table>	Value	Name	Description	0-512KB		The programmable range is 0-512KB when FrameBitrateMaxUnit is 0.	0-64MB		The programmable range is 0-64Mbyte when FrameBitrateMaxUnit is 1.	
		Value	Name	Description								
0-512KB			The programmable range is 0-512KB when FrameBitrateMaxUnit is 0.									
0-64MB			The programmable range is 0-64Mbyte when FrameBitrateMaxUnit is 1.									
8		31	FrameBitrateMinUnit Format: U1 This field is the Frame Bitrate Minimum Limit Units.									



HCP_PIC_STATE																		
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>Byte</td><td>32byte unit</td></tr><tr><td>1</td><td>Kilo Byte</td><td>4kbyte unit</td></tr><tr><td colspan="3">Programming Notes</td></tr><tr><td colspan="3">Encoder Only</td></tr></table>	Value	Name	Description	0	Byte	32byte unit	1	Kilo Byte	4kbyte unit	Programming Notes			Encoder Only			
		Value	Name	Description														
		0	Byte	32byte unit														
		1	Kilo Byte	4kbyte unit														
		Programming Notes																
	Encoder Only																	
	30:14	Reserved																
	Format:		MBZ															
	Reserved for future expansion of the Min Rate.																	
	13:0	FrameBitRateMin																
Format:		U14																
This field is the Frame Bitrate Minimum Limit. This field along with FrameBitrateMinUnit determines minimum allowed bits in a frame before multi-pass gets triggered (when enabled). In other words, multi-pass is triggered when the actual frame byte count happen to be below this value.																		
<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0-512KB</td><td></td><td>The programmable range is 0-512KB when FrameBitrateMinUnit is 0.</td></tr><tr><td>0-64MB</td><td></td><td>The programmable range is 0-64Mbyte when FrameBitrateMinUnit is 1.</td></tr></table>			Value	Name	Description	0-512KB		The programmable range is 0-512KB when FrameBitrateMinUnit is 0.	0-64MB		The programmable range is 0-64Mbyte when FrameBitrateMinUnit is 1.							
Value	Name	Description																
0-512KB		The programmable range is 0-512KB when FrameBitrateMinUnit is 0.																
0-64MB		The programmable range is 0-64Mbyte when FrameBitrateMinUnit is 1.																
Programming Notes																		
Encoder Only																		
9	31	Reserved																
		Format: MBZ																
	30:16	FrameBitRateMaxDelta																
		Exists If: //Always																
		Format: U15																
		This field is used to select the slice delta QP when FrameBitRateMax Is exceeded. It shares the same FrameBitrateMaxUnit.																
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>[Default]</td><td></td></tr><tr><td>0-1024KB</td><td></td><td>The Programmable range is 0-1024KB when FrameBitRateMaxUnit is 0.</td></tr><tr><td>0-128MB</td><td></td><td>The Programmable range is 0-128MB when FrameBitRateMaxUnit is 1.</td></tr></table>		Value	Name	Description	0	[Default]		0-1024KB		The Programmable range is 0-1024KB when FrameBitRateMaxUnit is 0.	0-128MB		The Programmable range is 0-128MB when FrameBitRateMaxUnit is 1.			
		Value	Name	Description														
		0	[Default]															
		0-1024KB		The Programmable range is 0-1024KB when FrameBitRateMaxUnit is 0.														
0-128MB		The Programmable range is 0-128MB when FrameBitRateMaxUnit is 1.																
Programming Notes																		



HCP_PIC_STATE				
		Encoder Only		
	15	Reserved		
		Format:	MBZ	
	14:0	FrameBitRateMinDelta		
		Format:	U15	
		This field is used to select the slice delta QP when FrameBitRateMin Is exceeded. It shares the same FrameBitrateMinUnit.		
		Value	Name	Description
		0	[Default]	
		0-1024KB		The Programmable range is 0-1024KB when FrameBitRateMinUnit is 0.
		0-128MB		The Programmable range is 0-128MB when FrameBitRateMinUnit is 1.
		Programming Notes		
HW requires the following condition: FrameBitRateMinDelta <= 2*FrameBitRateMinMust be true, otherwise it may cause unpredicted behavior.				
Encoder Only				
10..11	63:0	FrameDeltaQpMax		
	Format:	FrameDeltaQp		
	Range: [0:MAX_QP_DELTA]			
	Frame level delta QP which should be used in case FrameSize - FrameBitRateMax in the range of ((DeltaQpMaxRange[n] * FrameBitRateMaxDelta»5)), DeltaQpMaxRange[n+1] * FrameBitRateMaxDelta»5)).			
	Programming Notes			
	If n == 7, DeltaQpMaxRange is infinity.			
	Format: 8 bit sign-magnitude, Range: [0:63]			
	Encoder Only			



HCP_PIC_STATE		
12..13	63:0	FrameDeltaQpMin
		Format: FrameDeltaQp
		Range: [0:MIN_QP_DELTA]
		Frame level delta QP which should be used in case FrameSize - FrameBitRateMin in the range of $((\Delta QpMinRange[n] * FrameBitRateMinDelta \gg 5))$, $\Delta QpMinRange[n+1] * FrameBitRateMinDelta \gg 5$.
		Programming Notes
		If $n == 7$, DeltaQpMinRange is infinity. Format: 8 bit sign-magnitude Range: [-63:0] Encoder Only
14..15	63:0	FrameDeltaQpMaxRange
		Format: FrameDeltaQpRange
		Range: [0:U8_MAX]
		Condition: $FrameDeltaQpMaxRange[n] \geq FrameDeltaQpMaxRange[n-1]$
		This field is to calculate ranges for Frame level delta QP, specifically Frame level delta QP[n] and Frame level delta QP[n+1].
		Programming Notes If $n == 0$, FrameDeltaQpMaxRange is zero. Encoder Only
16..17	63:0	FrameDeltaQpMinRange
		Format: FrameDeltaQpRange
		Range: [0:U8_MAX]
		Condition: $FrameDeltaQpMinRange[n] \geq FrameDeltaQpMinRange[n-1]$
		This field is to calculate ranges for Frame level delta QP, specifically Frame level delta QP[n] and Frame level delta QP[n+1].
		Programming Notes If $n == 0$, FrameDeltaQpMinRange is zero. Encoder Only



HCP_PIC_STATE																	
18	31:30	MinFrameSizeUnits															
		Format: U2															
		This field is the Minimum Frame Size Units															
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>4Kb</td><td>Minimum Frame Size is in 4Kbytes.</td></tr><tr><td>1</td><td>16Kb</td><td>Minimum Frame Size is in 16Kbytes.</td></tr><tr><td>2</td><td>Reserved</td><td></td></tr><tr><td>3</td><td>Reserved</td><td></td></tr></table>	Value	Name	Description	0	4Kb	Minimum Frame Size is in 4Kbytes.	1	16Kb	Minimum Frame Size is in 16Kbytes.	2	Reserved		3	Reserved	
		Value	Name	Description													
		0	4Kb	Minimum Frame Size is in 4Kbytes.													
		1	16Kb	Minimum Frame Size is in 16Kbytes.													
		2	Reserved														
	3	Reserved															
	Programming Notes																
Encoder Only																	
29:16	Reserved																
	Format: MBZ																
15:0	MinFrameSize	Default Value: 0															
		Format: U16															
		Minimum Frame Size [15:0] (in Word, 16-bit)(Encoder Only) Mininum Frame Size is specified to compensate for intel Rate Control Currently zero fill (no need to perform emulation byte insertion) is done only to the end of the CABAC_ZERO_WORD insertion (if any) at the last slice of a picture. It is needed for CBR. Intel encoder parameter, not part of DXVA. The caller should always make sure that the value, represented by Mininum Frame Size, is always less than maximum frame size FrameBitRateMax. This field is reserved in Decode mode.															
	Programming Notes																
	Programmable range is 0..(2^16-1) * 2^12 when MinFrameSizeUnits is 0. (4KB unit)																
	Programmable range is 0..(2^16-1) * 2^14 when MinFrameSizeUnits is 1. (16KB unit)																
	Encoder Only																



HCP_PIPE_MODE_SELECT

HCP_PIPE_MODE_SELECT			
Source:		VideoCS	
Length Bias:		2	
The HCP is selected with the Media Instruction Opcode "7h" for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16. The workload for the HCP is based upon a single frame decode. There are no states saved between frame decodes in the HCP. Once the bit stream DMA is configured with the HCP_BSD_OBJECT command, and the bit stream is presented to the HCP, the frame decode will begin. The HCP_PIPE_MODE_SELECT command is responsible for general pipeline level configuration that would normally be set once for a single stream encode or decode and would not be modified on a frame workload basis. This is a picture level state command and is shared by both encoding and decoding processes.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	Pipeline Type	
		Default Value:	2h
		Format:	OpCode
	26:23	Media Instruction Opcode	
		Default Value:	7h Codec/Engine Name
		Format:	OpCode
		Codec/Engine Name = HCP = 7h	
	22:16	Media Instruction Command	
		Default Value:	0h HCP_PIPE_MODE_SELECT
		Format:	OpCode
	15:12	Reserved	
Format:		MBZ	
11:0	DWord Length		
	Format:	=n	
	(Excludes Dwords 0, 1).		
	Value	Name	
	4h	Value_4	
1	31:24	Reserved	
	23	Reserved	
		Format:	MBZ



HCP_PIPE_MODE_SELECT

	22:20	Reserved	
		Format:	MBZ
	19:18	Reserved	
		Format:	MBZ
	17	RESERVED	
		Format:	MBZ
	16:13	Reserved	
		Format:	MBZ
	12	Reserved	
		Format:	MBZ
	11	Reserved	
		Format:	MBZ
	10	Reserved	
	9	Reserved	
	8	Reserved	
	7:5	Codec Standard Select	
		Value	Name
		0	HEVC
	4	Reserved This bit is reserved since it is used by HUC_PIPE_MODE_SELECT. Making sure there is no overlap between the two commands.	
	3	Pic Status/Error Report Enable	
		Format:	Enable
		Value	Name
		0	Disable
		1	Enable
		Description	
		Disable status/error reporting	
		Status/Error reporting is written out once per picture. The Pic Status/Error Report ID in DWord3 along with the status/error status bits are packed into one cache line and written to the Status/Error Buffer address in the HCP_PIPE_BUF_ADDR_STATE command. Must be zero for encoder mode.	
	2	Reserved	
	1	Deblocker Streamout Enable	
		Format:	Enable
		Deblocker Streamout Enable not currently supported for Encode or Decode	
		Value	Name
		0	Disable
		1	Enable
		Description	
		Disable deblocker-only parameter streamout	
		Enable deblocker-only parameter streamout	



HCP_PIPE_MODE_SELECT											
	0	Codec Select									
		Format:U1									
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>Decode</td></tr><tr><td>1</td><td>Encode</td></tr></table>	Value	Name	0	Decode	1	Encode			
		Value	Name								
0	Decode										
1	Encode										
2	31:0	Media Soft-Reset Counter (per 1000 clocks)									
		Format:U32									
		In decoder modes, this counter value specifies the number of clocks (per 1000) of GAC inactivity before a media soft-reset is applied to the HCP and HuC. If counter value is set to 0, the media soft-reset feature is disabled and no reset will occur. In encoder modes, this counter must be set to 0 to disable media soft reset. This feature is not supported for the encoder.									
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>Disable</td></tr></table>	Value	Name	0	Disable					
		Value	Name								
0	Disable										
3	31:0	Pic Status/Error Report ID									
		Format:U32									
		The Pic Status/Error Report ID is a unique 32-bit unsigned integer assigned to each picture status/error output. Must be zero for encoder mode.									
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>32-bit unsigned</td><td>Unique ID Number</td></tr><tr><td>1</td><td>Reserved</td><td></td></tr></table>	Value	Name	Description	0	32-bit unsigned	Unique ID Number	1	Reserved	
		Value	Name	Description							
		0	32-bit unsigned	Unique ID Number							
		1	Reserved								
		Programming Notes									
		Software must program different Status/Error Buffer addresses between pictures; otherwise the hardware might overwrite previously written data.									



HCP_SLICE_STATE

HCP_SLICE_STATE			
Source:		VideoCS	
Length Bias:		2	
The HCP is selected with the Media Instruction Opcode "7h" for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16. This is a slice level command used in both encoding and decoding processes. For decoder, it is issued with the HCP_BSD_OBJECT command.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	Pipeline Type	
		Default Value:	2h
		Format:	OpCode
	26:23	Media Instruction Opcode	
		Default Value:	7h Codec/Engine Name
		Format:	OpCode
		Codec/Engine Name = HCP = 7h	
	22:16	Media Instruction Command	
		Default Value:	14h HCP_SLICE_STATE
		Format:	OpCode
15:12	Reserved		
	Format:	MBZ	
11:0	Dword Length		
	Format:	=n	
	(Excludes Dwords 0, 1).		
	Value	Name	
	7h		
1	31:25	Reserved	
		Format:	MBZ
	24:16	SliceStartCtbY or (slice_start_lcu_y encoder)	
		Format:	U9
		Specifies the starting row address of the first coding tree block in the current slice.	
	15:9	Reserved	
Format:		MBZ	



HCP_SLICE_STATE								
	8:0	SliceStartCtbX or (slice_start_lcu_x encoder) Format: U9 Specifies the starting column address of the first coding tree block in the current slice.						
	2	31:25 Reserved Format: MBZ						
	24:16	NextSliceStartCtbY or (next_slice_start_lcu_y encoder) Format: U9 Specifies the starting row address of the first coding tree block in the next slice. Must be set to zero when the current slice is the last slice of a picture. For the single slice per frame case, the only slice is also the last slice, so this parameter should be set to a number larger than the frame height (at least +1).						
	15	Reserved						
	14:9	Reserved Format: MBZ						
	8:0	NextSliceStartCtbX or (next_slice_start_lcu_x encoder) Format: U9 Specifies the starting column address of the first coding tree block in the next slice. Must be set to zero when the current slice is the last slice of a picture. For the single slice per frame case, the only slice is also the last slice, so this parameter should be set to a number larger than the frame width (at least +1).						
	3	31:26 Reserved Format: MBZ						
	25	Reserved Format: MBZ						
	24	Reserved Format: MBZ						
	23	Reserved Format: MBZ						
	22	Reserved						
	21:17	slice_cr_qp_offset Format: S4 For deblocking purpose, the pic and slice level cr qp offset must be provided separately. PAK needs to perform final_chroma_cr_qp_offset = pic_cr_qp_offset + slice_cr_qp_offset.						
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>14h</td><td>-12</td></tr><tr><td>15h</td><td>-11</td></tr></table>		Value	Name	14h	-12	15h	-11
	Value	Name						
	14h	-12						
	15h	-11						



HCP_SLICE_STATE		
		16h -10
		17h -9
		18h -8
		19h -7
		1Ah -6
		1Bh -5
		1Ch -4
		1Dh -3
		1Eh -2
		1Fh -1
		0h 0
		1h 1
		2h 2
		3h 3
		4h 4
		5h 5
		6h 6
		7h 7
		8h 8
		9h 9
		0Ah 10
		0Bh 11
		0Ch 12
	Programming Notes	
	The valid value is from -12 to 12 (or 14h to 0Ch).	
	16:12	slice_cb_qp_offset
		Format: S4
		For deblocking purpose, the pic and slice level cb qp offset must be provided separately.
		PAK needs to perform $\text{final\_chroma\_cb\_qp\_offset} = \text{pic\_cb\_qp\_offset} + \text{slice\_cb\_qp\_offset}$.
		Value Name
		14h -12
		15h -11
		16h -10



HCP_SLICE_STATE		
		17h
		-9
		18h
		-8
		19h
		-7
		1Ah
		-6
		1Bh
		-5
		1Ch
		-4
		1Dh
		-3
		1Eh
		-2
		1Fh
		-1
		0h
		0
		1h
		1
		2h
		2
		3h
		3
		4h
		4
		5h
		5
		6h
		6
		7h
		7
		8h
		8
		9h
		9
		0Ah
		10
		0Bh
		11
		0Ch
		12
	Programming Notes	
	The valid value is from -12 to 12 (or 14h to 0Ch).	
	11:6	SliceQp
	Format: U6	
	Specifies the initial absolute value of QPy quantization parameter for the slice as defined in the Slice Header Semantics section of the HEVC standard.	
	This signifies only the magnitude of SliceQp. In 8 bit, SliceQp only goes from 0 to 51. But in 10 bit, it needs to go from -12 to 51. There is a sign bit specifies at bit [3] below.	
	5	slice_temporal_mvp_enable_flag
	Format: U1	
	Programming Notes	
	Must be same for all the slices within a frame in encoder mode (follow spec)	



HCP_SLICE_STATE														
	4	dependent_slice_flag Format: U1 Decoder only.												
	3	SliceQp Sign Flag Format: U1 This specifies the sign bit of SliceQp. This is added for HEVC 10 bit. For 8 bit, SliceQp goes from 0 to 51 so this bit should be zero. In 10 bit, SliceQp goes from -12 to 51 and this bit can be set for negative value.												
	2	LastSliceofPic Format: U1 This indicates the current slice is the very last slice of the current picture <table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>Not the last slice of the picture</td></tr><tr><td>1</td><td>Last slice of the picture</td></tr></table>	Value	Name	0	Not the last slice of the picture	1	Last slice of the picture						
	Value	Name												
	0	Not the last slice of the picture												
	1	Last slice of the picture												
	1:0	slice_type Format: U2 <table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>B-slice</td></tr><tr><td>1</td><td>P-slice</td></tr><tr><td>2</td><td>I-slice</td></tr><tr><td>3</td><td>Illegal/Reserved</td></tr></table>	Value	Name	0	B-slice	1	P-slice	2	I-slice	3	Illegal/Reserved		
	Value	Name												
	0	B-slice												
	1	P-slice												
2	I-slice													
3	Illegal/Reserved													
4	31:29	Reserved Format: MBZ												
	28:26	CollocatedRefIDX Format: U3 Collocated Motion Vector Temporal Buffer Index.												
	25:23	MaxMergeIDX Format: U3 MaxNumMergeCand = 5 - five_minus_max_num_merge_cand -1. <table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td></tr><tr><td>2</td><td>2</td></tr><tr><td>3</td><td>3</td></tr><tr><td>4</td><td>4</td></tr></table>	Value	Name	0	0	1	1	2	2	3	3	4	4
Value	Name													
0	0													
1	1													
2	2													
3	3													
4	4													



HCP_SLICE_STATE						
		<table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">The valid value is from 0 to 4 (MaxNumMergeCand = 5 - five_minus_max_num_merge_cand - 1)</td></tr></table>	Programming Notes		The valid value is from 0 to 4 (MaxNumMergeCand = 5 - five_minus_max_num_merge_cand - 1)	
Programming Notes						
The valid value is from 0 to 4 (MaxNumMergeCand = 5 - five_minus_max_num_merge_cand - 1)						
22	cabac_init_flag					
	Format:	U1				
21:19	luma_log2_weight_denom					
	Format:	U3				
18:16	ChromaLog2WeightDenom					
	Format:	U3				
15	collocated_from_I0_flag					
	Format:	U1				
14	isLowDelay					
	Format:	U1				
	If the POCs of all pictures in both lists are less than the current POC, then set to one, else set to zero.					
13	mvd_l1_zero_flag					
	Format:	U1				
	Decoder only.					
12	slice_sao_luma_flag					
	Format:	U1				
11	slice_sao_chroma_flag					
	Format:	U1				
10	slice_loop_filter_across_slices_enabled_flag					
	Format:	U1				
9	Reserved					
	Format:	MBZ				
8:5	slice_beta_offset_div2 or (final Beta_Offset_div2 Encoder)					
	Format:	S3				
	Deblocking filter beta offset. Specified in 2's comp.					
	Value	Name				
	[1101b,0011b]	[-3,3]				
	<table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">Valid only in encoder mode</td></tr></table>		Programming Notes		Valid only in encoder mode	
Programming Notes						
Valid only in encoder mode						
4:1	slice_tc_offset_div2 or (final tc_offset_div2 Encoder)					
	Format:	S3				



HCP_SLICE_STATE																														
		Deblocking filter tc offset. Specified in 2's comp.																												
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>[1101b,0011b]</td><td>[-3,3]</td></tr></table>	Value	Name	[1101b,0011b]	[-3,3]																								
		Value	Name																											
		[1101b,0011b]	[-3,3]																											
	<table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">Valid only in encoder mode</td></tr></table>	Programming Notes		Valid only in encoder mode																										
Programming Notes																														
Valid only in encoder mode																														
0	slice_header_disable_deblocking_filter_flag																													
	<table><tr><td>Format:</td><td>U1</td></tr></table>	Format:	U1																											
Format:	U1																													
5	31:16	Reserved																												
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ																										
	Format:	MBZ																												
	15:0	SliceHeaderLength																												
		<table><tr><td>Format:</td><td>U16</td></tr></table>	Format:	U16																										
Format:		U16																												
Decoder only. Specifies the length in bytes of the slice header including the start code. The starting byte of the slice header in the bit stream buffer is indicated by the Indirect Data Start Address in the HCP_BSD_OBJECT command. The ending byte of the slice header in the same bit stream buffer is indicated by the last byte prior to the slice data (CABAC).																														
6	31:30	Reserved																												
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ																										
	Format:	MBZ																												
	29:26	RoundInter																												
		<table><tr><td>Format:</td><td>U4</td></tr></table>	Format:	U4																										
		Format:	U4																											
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0h</td><td>+1/32</td></tr><tr><td>1h</td><td>+2/32</td></tr><tr><td>2h</td><td>+3/32</td></tr><tr><td>3h</td><td>+4/32</td></tr><tr><td>4h</td><td>+5/32 [Default]</td></tr><tr><td>5h</td><td>+6/32</td></tr><tr><td>6h</td><td>+7/32</td></tr><tr><td>7h</td><td>+8/32</td></tr><tr><td>8h</td><td>+9/32</td></tr><tr><td>9h</td><td>+10/32</td></tr><tr><td>Ah</td><td>+11/32</td></tr><tr><td>Bh</td><td>+12/32</td></tr><tr><td>Ch</td><td>+13/32</td></tr></table>	Value	Name	0h	+1/32	1h	+2/32	2h	+3/32	3h	+4/32	4h	+5/32 [Default]	5h	+6/32	6h	+7/32	7h	+8/32	8h	+9/32	9h	+10/32	Ah	+11/32	Bh	+12/32	Ch	+13/32
		Value	Name																											
		0h	+1/32																											
		1h	+2/32																											
		2h	+3/32																											
		3h	+4/32																											
		4h	+5/32 [Default]																											
		5h	+6/32																											
		6h	+7/32																											
7h		+8/32																												
8h	+9/32																													
9h	+10/32																													
Ah	+11/32																													
Bh	+12/32																													
Ch	+13/32																													



HCP_SLICE_STATE			
		Dh	+14/32
		Eh	+15/32
		Fh	+16/32
		Programming Notes	
		Encoder only feature	
	25:24	Reserved	
		Format:	MBZ
	23:20	RoundIntra	
		Format:	U4
		Value	Name
		0h	+1/32
		1h	+2/32
		2h	+3/32
		3h	+4/32
		4h	+5/32 [Default]
		5h	+6/32
		6h	+7/32
		7h	+8/32
		8h	+9/32
		9h	+10/32
		Ah	+11/32
		Bh	+12/32
		Ch	+13/32
		Dh	+14/32
		Eh	+15/32
		Fh	+16/32
		Programming Notes	
		Encoder only feature	
	19:0	Reserved	
		Format:	MBZ
7	31:11	Reserved	
		Format:	MBZ



HCP_SLICE_STATE

10	Header Insertion Enable									
	Format:	U1								
	Must be followed by the PAK Insertion Object Command to perform the actual insertion.									
	<table> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0</td><td></td><td>No header insertion into the output bitstream buffer, before the current slice encoded bits.</td></tr> <tr> <td>1</td><td></td><td>Header insertion into the output bitstream buffer is present, and is before the current slice encoded bits.</td></tr> </table>	Value	Name	Description	0		No header insertion into the output bitstream buffer, before the current slice encoded bits.	1		Header insertion into the output bitstream buffer is present, and is before the current slice encoded bits.
Value	Name	Description								
0		No header insertion into the output bitstream buffer, before the current slice encoded bits.								
1		Header insertion into the output bitstream buffer is present, and is before the current slice encoded bits.								
Programming Notes Must be always enabled. Encoder Only feature										
9	SliceData Enable									
	Format:	U1								
	Must always be enabled. Encoder only feature.									
	<table> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0</td><td></td><td>No operation; no insertion.</td></tr> <tr> <td>1</td><td></td><td>Slice Data insertion by PAK Object Commands into the output bitstream buffer.</td></tr> </table>	Value	Name	Description	0		No operation; no insertion.	1		Slice Data insertion by PAK Object Commands into the output bitstream buffer.
Value	Name	Description								
0		No operation; no insertion.								
1		Slice Data insertion by PAK Object Commands into the output bitstream buffer.								
8	Tail Insertion Enable									
	Format:	U1								
	Must be followed by the PAK Insertion Object Command to perform the actual insertion.									
	<table> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0</td><td></td><td>No tail insertion into the output bitstream buffer, after the current slice encoded bits.</td></tr> <tr> <td>1</td><td></td><td>Tail insertion into the output bitstream buffer is present, and is after the current slice encoded bits.</td></tr> </table>	Value	Name	Description	0		No tail insertion into the output bitstream buffer, after the current slice encoded bits.	1		Tail insertion into the output bitstream buffer is present, and is after the current slice encoded bits.
Value	Name	Description								
0		No tail insertion into the output bitstream buffer, after the current slice encoded bits.								
1		Tail insertion into the output bitstream buffer is present, and is after the current slice encoded bits.								
Programming Notes Tail Insertion is allowed only at the end of last slice or last tile of a frame but not in the middle of frame. Also, no multiple tail insertions are allowed. Applies to all projects starting from SNB+ Encoder only feature										
7:3	Reserved									
	Format:	MBZ								



HCP_SLICE_STATE						
2	EmulationByteSliceInsertEnable	Format:	U1			
		To have PAK outputting SODB or EBSP to the output bitstream buffer.				
		Value	Name			
		0	outputting RBSP			
		1	outputting EBSP			
		Programming Notes				
		Encoder Only feature				
		1	CabacZeroWordInsertionEnable	Format:	U1	
				To pad the end of a SliceLayer RBSP to meet the encoded size requirement.		
				Value	Name	Description
				0		No Cabac_Zero_Word Insertion.
				1		Allow internal Cabac_Zero_Word generation and append to the end of RBSP (effectively can be used as an indicator for last slice of a picture, if the assumption is only the last slice of a picture needs to insert CABAC_ZERO_WORDS).
Programming Notes						
Encoder Only feature						
0	Reserved			Format:	MBZ	
8	31:29			Reserved	Format:	MBZ
	28:6			Indirect PAK-BSE Data Start Offset (Write)	Format:	U23
		This field specifies the memory starting address (offset) to write out the compressed bitstream data from the BSE processing. This pointer is relative to the HCP PAK-BSE Object Base Address.				
		It is a cacheline-aligned address for the HEVC bitstream data.				
		For Write, there is no need to have a data length field. It is assumed the global memory upper bound check specified in the IND_OBJ_BASE_ADDRESS command (Indirect PAK-BSE Object Access Upper Bound) will take care of any illegal write access.				
		Value	Name			
		0-512MB				



HCP_SLICE_STATE		
		Programming Notes
		Must be zero.
		Encoder Only feature
	5:0	Reserved
		Format: MBZ



HCP_SURFACE_STATE

HCP_SURFACE_STATE			
Source:		VideoCS	
Length Bias:		2	
The HCP is selected with the Media Instruction Opcode "7h" for all HCP Commands. Each HCP command has assigned a media instruction command as defined in DWord 0, BitField 22:16. The HCP_SURFACE_STATE command is responsible for defining the frame buffer pitch and the offset of the chroma component. This is a picture level state command and is shared by both encoding and decoding processes. Note : Only NV12 and Tile Y are being supported for HEVC. Hence full pitch and interleaved UV is always in use. U and V Xoffset must be set to 0; U and V Yoffset must be 16-pixel aligned. This Surface State is not the same as that of the 3D engine and of the MFX pipeline.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	Pipeline Type	
		Default Value:	2h
		Format:	OpCode
	26:23	Media Instruction Opcode	
		Default Value:	7h Codec/Engine Name
		Format:	OpCode
		Codec/Engine Name = HCP = 7h	
	22:16	Media Instruction Command	
		Default Value:	1h HCP_SURFACE_STATE
		Format:	OpCode
15:12	Reserved		
	Format:	MBZ	
11:0	Dword Length		
	Format:	=n	
	(Excludes Dwords 0, 1).		
	Value	Name	
	1h		
1	31:28	Surface Id	
		Format:	U4
		Value	Name
		Description	



HCP_SURFACE_STATE			
		0h	HEVC: For current decoded Picture
		1h	Source Input Picture (encoder)
		2h	Reserved
		3h	Reserved
		4h	Reserved
	27:17	Reserved	
		Format:	MBZ
	16:0	Surface Pitch Minus1	
		Format:	U17-1
This field specifies the surface pitch in (#Bytes - 1).			
Programming Notes For TileYF and TileYS surfaces, the range is dependent on the Cu parameter (refer to Memory Data Formats section for the definition of the Cu parameter depending on the case). The range in bytes is $[2^{Cu}-1, 131071]$ -> $[(2^{Cu})B, 128KB] = [1 \text{ tile}, 128KB/(2^{Cu} \text{ tiles})]$ The field specifies the surface pitch in (#Bytes - 1) For tiled surfaces, the pitch must be a multiple of the tile width (i.e.128 bytes aligned). If Half Pitch for Chroma is set, this field must be a multiple of two tile widths for tiled surfaces, or a multiple of 2 bytes for linear surfaces.For Y-tiled surfaces: Range = [127, 131071] to [128B,128KB] = [1 tile, 1024 tiles]			
2	31:28	Surface Format	
		Format:	U4
		Specifies the format of the surface.	
		Value	Name
		0h-2h	Reserved
		4h	PLANAR_420_8
		5h-Ch	Reserved
		Dh	P010
		Fh	Reserved
	27:15	Reserved	
		Format:	MBZ
	14:0	Y Offset for U(Cb) in pixel	
		Format:	U15_Pixel_Row_Offset
		This field specifies the vertical offset in rows from the Surface Base Address to the start (origin) of the U(Cb) plane or the interleaved UV plane if Interleave Chroma is enabled. This field is only used for PLANAR surface formats.	
		Programming Notes The following restrictions are applicable when Memory compression is enabled.	



HCP_SURFACE_STATE

- For PLANAR_420 surface formats, the alignment of this field follows the tile mode described in bits 14:13 of the **Memory Address Attributes** table.
- TileY (legacy 4k) - 8 pixel aligned
- TileYF (New 4k) - 64 pixel aligned
- TileYS (64k) - 256 pixel aligned

When Memory compression is not enabled, This field should be multiple of 8 pixels.



HUC_PIPE_MODE_SELECT

HUC_PIPE_MODE_SELECT			
Source:		VideoCS	
Length Bias:		2	
The HUC is selected with the Media Instruction Opcode "Bh" for all HUC Commands. Each HUC command has assigned a media instruction command as defined in DWord 0, BitField 22:16.			
The HUC_PIPE_MODE_SELECT command is responsible for general pipeline level configuration that would normally be set once for a single stream decode and would not be modified on a frame workload basis.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	Pipeline Type	
		Default Value:	2h
		Format:	OpCode
	26:23	Media Instruction Opcode	
		Default Value:	Bh Codec/Engine Name
		Format:	OpCode
		Codec/Engine Name = HUP = Bh	
	22:16	Media Instruction Command	
		Default Value:	0h HUC_PIPE_MODE_SELECT
		Format:	OpCode
	15:12	Reserved	
Format:		MBZ	
11:0	DWord Length		
	Format:	=n	
	(Excludes Dwords 0, 1).		
	Value	Name	
	1h		
1	31:24	Reserved	
	23:11	Reserved	
		Format:	MBZ
	10	HUC Stream Object Enable	
		This indicates that HUC Stream Object command is going to be programmed. This bit should be set to "1" if HUC_STREAM_OBJECT command is going to be programmed. If this bit is not set, HUC_STREAM_OBJECT should not be programmed in the current operation. This bit is only used by hardware to prepare for bitstream processing.	



HUC_PIPE_MODE_SELECT										
	9:5	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ						
	Format:	MBZ								
	4	Indirect Stream Out Enable <table><tr><td>Format:</td><td>Enable</td></tr></table> Enables the bitstream to be written out to memory. The memory buffer is addressed through the HuC Indirect Stream Out ObjectBase Address. <table><tr><th>Value</th><th>Name</th></tr><tr><td>0h</td><td>Disable Indirect Stream Out</td></tr><tr><td>1h</td><td>Enable Indirect Stream Out</td></tr></table>	Format:	Enable	Value	Name	0h	Disable Indirect Stream Out	1h	Enable Indirect Stream Out
		Format:	Enable							
		Value	Name							
		0h	Disable Indirect Stream Out							
		1h	Enable Indirect Stream Out							
3:0	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ							
Format:	MBZ									
2	31:0	Media Soft-Reset Counter (per 1000 clocks) <table><tr><td>Format:</td><td>U32</td></tr></table> In decoder modes, this counter value specifies the number of clocks (per 1000) of GAC inactivity before a media soft-reset is applied to the HCP and HuC. If counter value is set to 0, the media soft-reset feature is disabled and no reset will occur. In encoder modes, this counter must be set to 0 to disable media soft reset. This feature is not supported for the encoder. <table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>Disable</td></tr></table>	Format:	U32	Value	Name	0	Disable		
		Format:	U32							
		Value	Name							
		0	Disable							
3	31:0	Reserved This field is intentionally left blank to match the format of HCP_PIPE_MODE_SELECT.								
4	31:0	Reserved								
5	31:0	Reserved								



HUC_STREAM_OBJECT

HUC_STREAM_OBJECT				
Source:		VideoCS		
Length Bias:		2		
The HUC is selected with the Media Instruction Opcode "Bh" for all HUC Commands. Each HUC command has assigned a media instruction command as defined in DWord 0, BitField 22:16.				
The HUC_STREAM_OBJECT command is used to define the bit stream address offset to the Stream Indirect Object base Address and the length of the bit stream. The bitstream buffer the HUC operates upon is specified through indirect addressing.				
DWord	Bit	Description		
0	31:29	Command Type		
		Default Value:	3h PARALLEL_VIDEO_PIPE	
		Format:	OpCode	
	28:27	Pipeline Type		
		Default Value:	2h	
		Format:	OpCode	
	26:23	Media Instruction Opcode		
		Default Value:	Bh Codec/Engine Name	
		Format:	OpCode	
		Codec/Engine Name = HUC = Bh		
	22:16	Media Instruction Command		
		Default Value:	20h HUC_STREAM_OBJECT	
		Format:	OpCode	
	15:12	Reserved		
		Format:	MBZ	
	11:0	Dword Length		
		Format:	=n	
		(Excludes Dwords 0, 1).		
		Value		Name
3h				



HUC_STREAM_OBJECT				
1	31:0	Indirect Stream In Data Length		
		Format:	U32	
		Specifies the length in bytes of the bit stream input data.		
		Value	Name	Description
		[0,268435455]	Data_Length_with_28_bits_only	Valid range is only from 0 to 268435455, which is corresponding to lower 28 bits. This restriction is for old project which only use 28 bits data length.
		[268435456,2147483547]	Data_Length_beyond_28_bits	This is an added valid range when the bit length is extended from 28 bits to 32 bits. This is added to support 16k x 16k picture size bitstream.
2	31	Reserved		
	30:29	Reserved		
		Format:	MBZ	
	28:0	Indirect Stream In Start Address		
Format:		U29		
Specifies the byte-aligned graphics memory starting address of the input bit stream relative to the HUC Indirect Stream In ObjectBase Address [31:12].				
3	31:29	Reserved		
		Format:	MBZ	
	28:0	Indirect Stream Out Start Address		
		Format:	U29	
Specifies the byte-aligned graphics memory starting address of the output bit stream relative to the HUC Indirect Stream Out ObjectBase Address [31:12].				
4	31:30	Reserved		
		Format:	MBZ	
	29	HuC Bitstream Enable		
		Format:	Enable	
		Enables the bitstream to be sent to the HuC		
		Value	Name	
0h	Disable			
1h	Enable			



HUC_STREAM_OBJECT

	28:27	DRMLengthMode	
		Format:	U2
		Value	Name
			Description
		00b	Start Code Mode
			Stops on a start code
		01b	Length Mode
			Stops after a number of bytes are reached in the length counter
		10b	Reserved
		11b	Reserved
	26	Reserved	
	25	Emulation Prevention Byte Removal	
		Format:	Enable
		Value	Name
			Description
		0	Disable
			Bypass Emulation Prevention Byte Removal.
		1	Enable
			Emulation prevention bytes will be removed after the start code search engine.
	24	Start Code Search Engine	
		Format:	Enable
		Value	Name
			Description
		0	Disable
			Bypass Start Code Search Engine
		1	Enable
			Enables the start code search engine to stop on every third byte start code defined by Start Code Byte [2:0] defined in this DWord.
	23:16	Start Code Byte [2]	
		Format:	U8
		Third byte of the start code	
	15:8	Start Code Byte [1]	
		Format:	U8
		Second byte of the start code	
	7:0	Start Code Byte [0]	
		Format:	U8
		First byte of the start code	



MEDIA_OBJECT_GRPID

MEDIA_OBJECT_GRPID			
Source:	RenderCS		
Length Bias:	2		
The MEDIA_OBJECT_GRPID command is a variation of MEDIA_OBJECT which includes a group id which is used to allocate and track Barriers and Shared Local Memory. The Interface Descriptor is used to specify how much SLM is needed and how many threads will be reporting to the Barrier. All MEDIA_OBJECT_GRPIDs with the same group id should have the same interface descriptor and be dispatched to the same Tslice – the dispatcher will ensure this if Force Destination = 0, but software must ensure this if Force Destination = 1. Software should also ensure that all the threads needed for the Barrier will fit into a Tslice, or the Barrier will never be satisfied. Either SLM or a barrier must be used with MEDIA_OBJECT_GRPID, if neither is needed then a MEDIA_OBJECT must be used instead. MEDIA_OBJECT_GRPID supports the GPGPU version of payload delivery – either indirect or CURBE can be split between the threads in a group (per-thread payload), as well as a section which is sent to all threads (cross-thread payload). See the GPGPU payload section. For indirect, the same pointer must be sent with all the commands associated with the thread group for payload splitting to work properly. Inline data is not split, but the payload attached to each command is sent with that thread. Only one of inline, indirect, or CURBE is allowed, but at least one form of payload must be sent. MEDIA_STATE_FLUSH with the watermark bit must be placed between groups created by MEDIA_OBJECT_GRPID. The Interface Descriptor associated with the watermark must match the Interface Descriptor used for the following group.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	Media Command Pipeline	
		Default Value:	2h Media
		Format:	OpCode
	26:24	Media Command Opcode	
		Default Value:	1h MEDIA_OBJECT_GRPID
		Format:	OpCode
	23:16	Media Command Sub-Opcode	
		Default Value:	6h MEDIA_OBJECT_GRPID SubOp
		Format:	OpCode
	15:0	DWord Length	
		Default Value:	5h DWORD_COUNT_n
		Format:	=n Total Length - 2
		Excludes DWords 0,1	
Generic Mode: DWord Length = N+5, where N is in the range of [0,504]. The maximum is 504 DW (equivalent to 63 8-DW registers).			



MEDIA_OBJECT_GRPID			
		When both inline and indirect data are fetched for this command, the total size in 8-DW registers must be less than 112 (with both inline data length N and indirect data length rounded up to 8-DW aligned individually). The minimal inline data length is 0.	
1	31:8	Reserved	
	7:6	Reserved	
		Format:	MBZ
	5:0	Interface Descriptor Offset	
		Format:	U6
		This field specifies the offset from the interface descriptor base pointer to the interface descriptor which will be applied to this object. It is specified in units of interface descriptors.	
		Value	Name
		[0,30]	
2	31:25	Reserved	
		Format:	MBZ
	24	Reserved	
	23	End of Thread Group	
		This bit indicates that this dispatch is the last for the current thread group.	
	22	Force Destination	
		Description	
		If set, bits 20:17 are used to determine the destination of this dispatch, if clear the destination will be chosen based on load.	
		When using Force Destination=1 and Pooled EUs with BXT-A, the size of the maximum thread group using either barriers or SLM for subslice 1 is 18 rather than 36, since subslice 1 is split between 2 pools. If neither barriers nor SLM are used then the normal thread group size of 36 is allowed. BXT-C is not impacted and all 36 thread can be forced to either subslice.	
	21	Use Scoreboard	
	This field specifies whether the thread associated with this command uses hardware scoreboard. Only when this field is set, the scoreboard control fields in the VFE Dword are valid. If this field is cleared, the thread associated with this command bypasses hardware scoreboard.		
	Value	Name	
	0	Not using scoreboard	
	1	Using scoreboard	
20:19	Slice Destination Select		
	This bit along with the SubSlice destination select determines the slice that this thread must be sent to. Ignored if Force Destination = 0, or if product only has 1 slice.		
	Value	Name	Description
	00b	Slice 0	



MEDIA_OBJECT_GRPID					
3		01b	Slice 1	Cannot be used in products without a Slice 1.	
		10b	Slice 2	Cannot be used in products without a Slice 2.	
		11b	Reserved		
	18:17	SubSlice Destination Select This field selects the SubSlice that this thread must be sent to. Ignored if Force Destination = 0			
		Value		Name	
		11b		Subslice3	
		10b		SubSlice 2	
		01b		SubSlice 1	
		00b		SubSlice 0	
	16:0	Indirect Data Length			
		Format:		U17 In bytes	
	This field provides the length in bytes of the indirect data. A value zero indicates that indirect data fetching is disabled - subsequently, the Indirect Data Start Address field is ignored. This field must have the same alignment as the Indirect Object Data Start Address. It must be DQWord (32-byte) aligned. As the indirect data are sent directly to URB, range is limited to(URB Entry Allocation Size)*(Number of URB Entries) in the MEDIA_VFE_STATE command.				
	31:0	Indirect Data Start Address			
		Format:		GraphicsAddress[31:0]	
		Description			
This field specifies the Graphics Memory starting address of the data to be loaded into the kernel for processing. This pointer is relative to the Indirect Object Base Address . Hardware ignores this field if indirect data is not present. Alignment of this address depends on the mode of operation. It is the 64-byte aligned address of the indirect data.					
Value		Name	Description		
[0-512MB]			Bits 31:29 MBZ		
31:25	Reserved				
	Format:			MBZ	
24:16	Scoreboard Y				
	Format:			U9	
	This field provides the Y term of the scoreboard value of the current thread.				
15:9	Reserved				
	Format:			MBZ	



MEDIA_OBJECT_GRPID				
5	8:0	Scoreboard X <table><tr><td>Format:</td><td>U9</td></tr></table> This field provides the X term of the scoreboard value of the current thread.	Format:	U9
	Format:	U9		
	31:20	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ
	Format:	MBZ		
	19:16	Scoreboard Color <table><tr><td>Format:</td><td>U4</td></tr></table> This field specifies which dependency color the current thread belongs to. It affects the dependency scoreboard control.	Format:	U4
Format:	U4			
15:8	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ	
Format:	MBZ			
7:0	Scoreboard Mask <table><tr><td>Format:</td><td>Boolean</td></tr></table> Each bit indicates the corresponding dependency scoreboard is dependent on. This field is AND'd with the corresponding Scoreboard Mask field in the MEDIA_VFE_STATE command. Bit n (for n = 0...7): Scoreboard n is dependent, where bit 0 maps to n = 0.	Format:	Boolean	
Format:	Boolean			
6	31:0	GroupID A unique identifying number which describes the threads which share a barrier and/or SLM. Reuse of numbers is allowed as long as the old group is not currently running.		
7..n	31:0	Inline Data The format of this data is specified by software. Hardware does not interpret this data; it merely passes it to the kernel for processing. The total size for the inline data and indirect data must not exceed 112 registers.		



MEDIA_POOL_STATE

MEDIA_POOL_STATE																					
Source:	RenderCS																				
Length Bias:	2																				
The MEDIA_POOL_STATE command is used to enable pooled-mode and assign EUs to pools. This command applies to both GPGPU & media operations. If pooled operation is desired, this command must be performed prior to sending any work to the pool. Failure to send this command prior to work commands results in the default 'LegacyMode' operation which contains thread groups to single subslices. The mechanism for assigning EUs to pools via a bitfield mapping as part of this command. Note that not all possible pool combinations available in the bit-mask may be supported on any given SKU and/or across architectural generations. This command is ignored in 3D mode (as determined by pipeline choice in the most recent PIPELINE_SELECT command). This command sets context state which is saved/restored with any context switch. This command is normally only issued once with each context initialization. PoolBitFields called for below map bit positions to individual EUs as follows: • bit0 = row0, eu0 • bit1 = row0, eu1 • bit2 = row0, eu2 • bit3 = row0, eu3 • bit4 = row1, eu0 • bit5 = row2, eu1 • bit6 = row3, eu2 • bit7 = row4, eu3 Valid Pool Sizes and Configurations: The table below identifies the valid pool configurations, depending on the subslice organization in the slice. There may be performance implications with the various settings depending on the size of the thread group as discussed in this feature's overview. The table ignores cases where one EU may be held back for manufacturability. For example, the 2x6 configuration may have a total of 12 or 11 valid EUs depending on SKUing, but only 12,0 is used in this command to cover both cases. Note: For BXT 3x6 a pool must consist of a subslice and a row from the center subslice, while for BXT 2x6 a pool must consist of a complete subslice, so only 9,9 is valid for 3x6 and 12,0 is valid for 2x6. <table><tr><th colspan="5">PoolBitField</th></tr><tr><th>BXT Config</th><th>Slice 0</th><th>Slice 1</th><th>Slice 2</th><th>Slice 3</th></tr><tr><td>2x6*</td><td>00000000h</td><td>0h</td><td>0h</td><td>0h</td></tr><tr><td>3x6*</td><td>00777000h</td><td>0h</td><td>0h</td><td>0h</td></tr></table> * Includes cases where all EUs in the slice are available and cases where 1 EU in the slice is disabled.		PoolBitField					BXT Config	Slice 0	Slice 1	Slice 2	Slice 3	2x6*	00000000h	0h	0h	0h	3x6*	00777000h	0h	0h	0h
PoolBitField																					
BXT Config	Slice 0	Slice 1	Slice 2	Slice 3																	
2x6*	00000000h	0h	0h	0h																	
3x6*	00777000h	0h	0h	0h																	
DWord	Bit	Description																			



MEDIA_POOL_STATE				
0	31:29	Command Type		
		Default Value:		3h GFXPIPE
		Format:		OpCode
	28:27	Pipeline		
		Default Value:		2h Media
		Format:		OpCode
	26:24	Media Command Opcode		
		Default Value:		0h
		Format:		OpCode
	23:16	SubOpcode		
		Default Value:		5h MEDIA_POOL_STATE
		Format:		OpCode
15:0	DWord Length			
	Format:		=n	
	n = Total Length - 2			
	Value	Name	Description	
	04h	DWORD_COUNT_n [Default]	Excludes DWord (0,1)	
1	31	PoolEnable		
		Format:		U1
		- When set to 1, this field enables the GPGPU Pool mechanism for all slices in the system. - When set to 0, legacy mode is in effect and pools are not defined; instead thread groups will be dispatched in such a way that each is contained to a single subslice. This legacy mode is provided <i>primarily</i> for backward <i>driver</i> compatibility, and may <i>in some cases</i> be non-performant <i>due to thread loading or SLM bandwidth</i>. - Mixing of LegacyMode and PooledMode across contexts is not allowed; i.e. the setting of the 'PooledMode' bit must be identical across all contexts until a subsequent HW reset.		
		Value	Name	
		0b	Disable [Default]	
	1b	Enable		
	30	Reserved		
		Format:		MBZ
	29:0	Reserved		
		Format:		MBZ
2	31:0	PoolBitField-Slice0		
		Format:		SubslicePool



MEDIA_POOL_STATE		
3	31:0	PoolBitField-Slice1
		<table><tr><td>Format:</td><td>SubslicePool</td></tr></table>
Format:	SubslicePool	
4	31:0	PoolBitField-Slice2
		<table><tr><td>Format:</td><td>SubslicePool</td></tr></table>
Format:	SubslicePool	
5	31:0	PoolBitField-Slice3
		<table><tr><td>Format:</td><td>SubslicePool</td></tr></table>
Format:	SubslicePool	



MEDIA_STATE_FLUSH

MEDIA_STATE_FLUSH			
Source:	RenderCS		
Length Bias:	2		
This command updates the Message Gateway state. In particular, it updates the state for a selected Interface Descriptor. This command can be considered same as a MI_Flush except that only media parser will get flushed instead of the entire 3D/media render pipeline. The command should be programmed prior to new Media state, curbe and/or interface descriptor commands when switching to a new context or programming new state for the same context. With this command, pipelined state change is allowed for the media pipe. Be cautious when using this command when child_present flag in the media state is enabled. This is because that CURBE state as well as Interface Descriptor state are shared between root threads and child threads. Changing these states while child threads are generated on the fly may cause unexpected behavior. Combining with MI_ARB_ON/OFF command, it is possible to support interruptability with the following command sequence where interrupt may be allowed only when MI_ARB_ON_OFF is ON: <pre>MEDIA_STATE_FLUSH VFE_STATE // VFE will hold CS if watermark isn't met MI_ARB_OFF // There must be at least one VFE command before this one MEDIA_OBJECT ... MI_ARB_ON</pre>			
Workaround			
Due to the known HW issue MEDIA_STATE_FLUSH command is not preemptable in GPGPU workloads. This might result in reduced frequency of preempting GPGPU walker in below programming sequence. <pre>//State Commands GPGPU_WALKER MEDIA_STATE_FLUSH //State Commands GPGPU_WALKER MEDIA_STATE_FLUSH //State Commands</pre> Below workaround must be applied to address the above issue. MI_ARB_CHK command must be programmed following MEDIA_STATE_FLUSH command. PIPECONTROL (“Command Streamer Stall Enable” set and “Render Target Cache Flush Enable” set) must be programmed prior to MEDIA_STATE_FLUSH command with “Flush to GO” bit set. “Water Mark Required” field must not be set in “MEDIA_STATE_FLUSH” command.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h GFXPIPE
		Format:	OpCode
	28:27	Pipeline	
		Default Value:	2h Media
		Format:	OpCode



MEDIA_STATE_FLUSH			
	26:24	Media Command Opcode	
		Default Value:	0h MEDIA_STATE_FLUSH
		Format:	OpCode
	23:16	SubOpcode	
		Default Value:	4h MEDIA_STATE_FLUSH SubOp
		Format:	OpCode
	15:0	DWord Length	
		Format:	=n Total Length - 2
		Value	Name
		0h	DWORD_COUNT_n [Default]
1	31:9	Reserved	
		Format:	MBZ
	8	Reserved	
	7	Flush to GO	
		Format:	Enable
		This bit indicates that the write data out of this thread group should be flushed to the point where it is visible to following commands.	
		Workaround	
		Workaround: PIPECONTROL ("Command Streamer Stall Enable" set and "Render Target Cache Flush Enable" set) must be programmed prior to MEDIA_STATE_FLUSH command with "Flush to GO" bit set.	
	6	Watermark Required	
		This is a single bit specifying if the MEDIA_STATE_FLUSH should stall further commands until there is enough room in a half-slice for the following thread group. The characteristics of the thread group are specified in the Interface Descriptor Offset.	
		If set, the MEDIA_STATE_FLUSH stalls CS until there are enough threads in a half-slice, and enough SLM available in the same half-slice, and a free barrier if one is required. An Interface Descriptors can be updated after a Watermarked MEDIA_STATE_FLUSH only if it has not been used in the current context. Reusing an interface descriptor requires that this bit is clear to ensure the ID cache is reloaded.	
		If clear, the MEDIA_STATE_FLUSH stalls CS until the TDL has dispatched the last thread, allowing the CURBE and Interface Descriptors to be updated by following commands.	
		Programming Notes	
		The Interface Descriptor Offset used for the flush must be the same as that used for the GPGPU_OBJECTs. GPGPU_WALKER automatically checks the Watermark conditions before starting a thread, so this bit should not be set before GPGPU_WALKER.	
		Workaround	



MEDIA_STATE_FLUSH		
		Workaround: If pre-emption is used, the WatermarkRequired bit must not be set.
	5:0	Interface Descriptor Offset
		Format: U6
		This field specifies the offset from the interface descriptor base pointer to the interface descriptor which describes what resources are required to meet the watermark.



MFD_VC1_LONG_PIC_STATE

MFD_VC1_LONG_PIC_STATE			
Source:		VideoCS	
Length Bias:		2	
MFX_VC1_LONG_PIC_STATE command encapsulates the decoding parameters that are read or derived from bitstream syntax elements above (inclusive) picture header layer. These parameters are static for a picture and when slice structure is present, these parameters are not changed from slice to slice of the same picture. Hence, this command is only issued at the beginning of processing a new picture and prior to the VC1_*_OBJECT command. The values set for these state variables are retained internally across slices.Only the parameters needed by hardware (BSD unit) to decode bit sequence for the macroblocks in a picture layer or a slice layer are presented in this command. Other parameters such as the ones used for inverse transform or motion compensation are provided in MFX_VC1_PRED_PIPE_STATE command.This Long interface format is intel proprietary interface. Driver will need to perform addition operations to generate all the fields in this command.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	Pipeline	
		Default Value:	2h MFD_VC1_LONG_PIC_STATE
		Format:	OpCode
	26:24	Media Command Opcode	
		Default Value:	2h VC1_DEC
		Format:	OpCode
	23:21	SubOpcode A	
		Default Value:	1h
		Format:	OpCode
	20:16	SubOpcode B	
		Default Value:	1h
		Format:	OpCode
	15:12	Reserved	
Format:		MBZ	
11:0	DWord Length		
	Default Value:	0004h Excludes DWord (0,1)	
	Format:	=n Total Length - 2	
1	31:24	Reserved	
		Format:	MBZ



MFD_VC1_LONG_PIC_STATE

	23:16	PictureHeightInMBsMinus1 (Picture Height Minus 1 in Macroblocks)	
		Format:	U8
		This field indicates the height of the picture in unit of macroblocks. For example, for a 1920x1080 frame picture, PictureHeightInMBs equals 68 (1080 divided by 16, and rounded up, i.e. effectively specified as 1088 instead).This field is used in VLD and IT modes.	
		Value	Name
		255	Value_255
		Programming Notes	
		Note: Even though the Advanced Profile allows frame dimensions (width, height) to not be aligned to macroblock boudary, it doesn't affect the bitstream decoding. And it is preferable to use 'intermediate buffer' that is macroblock aligned for decoding. In order to simplify the out-of-bound reference pixel access, the out-of-bound extrapolation rule in VC1 spec can be used to expand the expected decoded frame to the intermediate buffer dimension.	
	15:8	Reserved	
		Format:	MBZ
	7:0	PictureWidthInMBsMinus1 (Picture Width Minus 1 in Macroblocks)	
		Format:	U8-1
		This field indicates the width of the picture in unit of macroblocks. For example, for a 1920x1080 frame picture, PictureWidthInMBs equals 120 (1920 divided by 16).This field is used in VLD and IT modes	
		Value	Name
		255	Value_255
2	31:24	Bitplane Buffer Pitch Minus 1	
		Format:	U7-1 Pitch in (Bytes - 1).
		Specifies the bitplane buffer pitch in (#Bytes - 1). Bitplane buffer is a linear buffer. It is needed only when the bitplane is not encoded as raw, and therefore is present in the header explicitly. In VC1 Long Format (Gen6 and Gen7), it is written by an application and later read by the HW. But in VC1 Short Format (Gen7 only), it is written and read by H/W only.This field is specified for better performance	
		Value	Name
		[0, FFFFFFFFh]	
		Programming Notes	

**MFD_VC1_LONG_PIC_STATE**

		For Gen6 : The pitch must be equal to $\text{PictureWidthInMBs}/2$. For Gen7 VC1 Long Format : The pitch must be equal to $\text{PictureWidthInMBs}/2$. For Gen7 VC1 Short Format : If Pic Width is less than or equal to 2K pixels, bitplane pitch is set to 64 (one cacheline; programmed as 63) bytes per MB row. If Pic Width is greater than 2K pixels, bitplane pitch is set to 128 (two cachelines; programmed as 127) bytes per MB row. This field is not used in IT mode, used in VLD mode only. For VC1 DXVA2 Short Format, the bitplane specification is between H/W and Driver only. For Long Format, application is responsible for allocation with the driver.									
23:16	Reserved										
	Format:	MBZ									
15	DmvSurfaceValid	Indicated when the DMV read surface is valid. This surface stored the direct motion vectors and Mb type. This field is set for B pictures that can refer to a previous P picture for DMV. If there is an I-picture before a B (in decoding order) then this field is not set (as a result, zero's DMV's will be assumed while decoding the B picture. That is, there is no explicit DMV buffer for an I-picture). When the current picture being decoded is an I, P or BI, this bit is set to 0, since there is no DMV read in these picture decoding process. This field is not used in IT mode, used in VLD mode only.									
14	ImplicitQuantizer	Derived by driver from QUANTIZER. This field is used in intel VC1 VLD Long Format only, not used in IT and DXVA2 VC1. This bit is set to 1 when syntax element QUANTIZER=0, else its set to 0									
13	Interpolation Runder Contro	Used only in MC operation. This field specifies the rounding control value used in interpolation operation of motion prediction process. This field is used in VLD and IT modes.									
	Programming Notes										
	This bit field is taken from bRcontrol in DXVA_PictureParameters data structure										
12	SyncMarker	Indicates whether sync markers are enabled/disabled. If enable, sync markers "may be" present in the current video sequence being decoded. It is a sequence level syntax element and is valid only for Simple and Main Profiles.									
	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Not Present</td><td>Sync Marker is not present in the bitstream</td></tr><tr><td>1h</td><td>Maybe present</td><td>Sync Marker maybe present in the bitstream</td></tr></table>	Value	Name	Description	0h	Not Present	Sync Marker is not present in the bitstream	1h	Maybe present	Sync Marker maybe present in the bitstream	
Value	Name	Description									
0h	Not Present	Sync Marker is not present in the bitstream									
1h	Maybe present	Sync Marker maybe present in the bitstream									
	Programming Notes										
	This field is only valid in VLD mode. For Simple Profile, SyncMarker must set to 0. For Main Profile, SyncMarker can be set to 0 or 1. This field is used in both intel and MS DXVA2 VLD interface, but not used in IT mode.										
11:8	Motion Vector Mode	This field indicates one of the following motion compensation interpolation modes for P and B pictures. The MC interpolation modes apply to prediction values of luminance blocks and are									



MFD_VC1_LONG_PIC_STATE

always in quarter-sample. For chrominance blocks, it always performs bilinear interpolation with either half-pel or quarter-pel precision. Before the polarity of Chroma Half-pel or Q-pel is reversed from DXVA2 Spec, now I have fixed it to match with DXVA2 VC1 Spec.

Value	Name	Description
0XX0b		Chroma Quarter -pel + Luma bicubic. (can only be 1MV)
0XX1b		Chroma Half-pel + Luma bicubic. (can be 1MV or 4MV)
1XX0b		Chroma Quarter -pel + Luma bilinear. (can only be 1MV)
1XX1b		Chroma Half-pel + Luma bilinear

Programming Notes

Bits 11:8 are taken from bMVprecisionAndChromaRelation in DXVA_PictureParameters data structure. Bit 11 of Motion Vector Mode = 1 for Luma Bilinear MC; = 0 for Luma Bicubic MC. Bit 8 of Motion Vector Mode = 1 for half-sample Chroma motion = 0 for quarter-sample Chroma motion. This field is used in both VLD and IT modes.

7 RangeReductionScale

This field specifies whether the reference picture pixel values should be scaled up or scaled down on-the-fly, if RangeReduction is Enabled.

Value	Name	Description
0h		Scale down reference picture by factor of 2
1h		Scale up reference picture by factor of 2

Programming Notes

This bit is derived by driver for Main Profile only. Ignored in Simple and Advanced Profiles. This field is used in both VLD and IT modes. This is derived by driver from the history of RANGERED and RANGEREDFRM syntax elements (i.e. of forward/preceding reference picture) and those of the current picture. RANGERED is the same as (bPicOverflowBlocks » 3) & 1. RANGEREDFRM is the same as (bPicDeblocked » 5) & 1. For the current picture is a B picture, this field represents the state of the forward/preceding reference picture only. Driver is responsible to keep RangeReductionScale, RangeReduction Enable and RANGERED Present Flag of current picture coherent.

6 RangeReduction Enable

This field specifies whether on-the-fly pixel value range reduction should be performed for the preceding (or forward) reference picture. Along with RangeReductionScale to specify whether scale up or down should be performed. It is not the same value as RANGEREDFRM Syntax Element (DXVA_PictureParameters bPicDeblocked bit 5) in the Picture Header.

Value	Name	Description
0h	Disable	Range reduction is not performed
1h	Enable	Range reduction is performed

Programming Notes

**MFD_VC1_LONG_PIC_STATE**

MFD_VC1_LONG_PIC_STATE																	
		This field is for Main Profile only. Simple Profile is always disable, and not applicable to Advanced Profile. This field is used in both VLD and IT modes.This is derived by driver from the history of RANGERED and RANGEREDFRM syntax elements (i.e. of forward/preceding reference picture) and those of the current picture.RANGERED is the same as (bPicOverflowBlocks » 3) & 1. RANGEREDFRM is the same as (bPicDeblocked » 5) & 1.For the current picture is a B picture, this field represents the state of the forward/preceding reference picture onlyDriver is responsible to keep RangeReductionScale, RangeReduction Enable and RANGERED Present Flag of current picture coherent.															
5	LOOPFILTER Enable Flag This filed is the decoded syntax element LOOPFILTER in bitstream. It indicates if In-loop Deblocking is ON according to picture level bitstream syntax control. This bit affects BSD unit and also the loop filter unit.When this bit is set to 1, PostDeblockOutEnable field in MFX_PIPE_MODE_SELECT command must also be set to 1. In this case, in-loop deblocking operation follows the VC1 standard - deblocking doesn't cross slice boundary.When this bit is set to 0, but PostDeblockOutEnable field in MFX_PIPE_MODE_SELECT command is set to 1. It indicates the loop filter unit is used for out-of-loop deblocking. In this case, deblocking operation does cross slice boundary.This field is used in VLD mode only, not in IT mode.	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable</td><td>Disables loop filter</td></tr><tr><td>1h</td><td>Enable</td><td>Enables loop filter</td></tr></table>	Value	Name	Description	0h	Disable	Disables loop filter	1h	Enable	Enables loop filter						
Value	Name	Description															
0h	Disable	Disables loop filter															
1h	Enable	Enables loop filter															
4	Overlap Smoothing Enable Flag This field is the decoded syntax element OVERLAP in bitstreamIndicates if Overlap smoothing is ON at the picture levelThis field is used in both VLD and IT modes.	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable</td><td>to disable overlap smoothing filter</td></tr><tr><td>1h</td><td>Enable</td><td>to enable overlap smoothing filter</td></tr></table>	Value	Name	Description	0h	Disable	to disable overlap smoothing filter	1h	Enable	to enable overlap smoothing filter						
Value	Name	Description															
0h	Disable	to disable overlap smoothing filter															
1h	Enable	to enable overlap smoothing filter															
3	Secondfield This flag is set for the second field in field pictures.This field is used in both VLD and IT modes.																
2:1	Reserved	<table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ													
Format:	MBZ																
0	VC1 Profile specifies the bitstream profile.This field is used in both VLD and IT modes.	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable</td><td>current picture is in Simple or Main Profile (No need to distinguish Simple and Main Profile)</td></tr><tr><td>1h</td><td>Enable</td><td>current picture is in Advanced Profile</td></tr></table> <table><tr><th colspan="3">Programming Notes</th></tr><tr><td colspan="3">This is required because 128 is added for intra blocks post inverse transform in advanced profile and also to find out if Motion vectors are adjusted or not.</td></tr></table>	Value	Name	Description	0h	Disable	current picture is in Simple or Main Profile (No need to distinguish Simple and Main Profile)	1h	Enable	current picture is in Advanced Profile	Programming Notes			This is required because 128 is added for intra blocks post inverse transform in advanced profile and also to find out if Motion vectors are adjusted or not.		
Value	Name	Description															
0h	Disable	current picture is in Simple or Main Profile (No need to distinguish Simple and Main Profile)															
1h	Enable	current picture is in Advanced Profile															
Programming Notes																	
This is required because 128 is added for intra blocks post inverse transform in advanced profile and also to find out if Motion vectors are adjusted or not.																	



MFD_VC1_LONG_PIC_STATE																	
3	31	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ													
	Format:	MBZ															
	30:29	CondOver This field is the decoded syntax element CONDOVER in a bitstream of advanced profile. It controls the overlap smoothing filter operation for an I frame or an BI frame when the picture level qualization step size PQUANT is 8 or lower.This field is used in intel VC1 VLD mode only, not in DXVA2 VC1 and IT modes. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>00b</td><td></td><td>No overlap smoothing</td></tr><tr><td>01b</td><td></td><td>Reserved</td></tr><tr><td>10b</td><td></td><td>Always perform overlap smoothing filter</td></tr><tr><td>11b</td><td></td><td>Overlap smoothing on a per macroblock basis based on OVERFLAGS</td></tr></table>	Value	Name	Description	00b		No overlap smoothing	01b		Reserved	10b		Always perform overlap smoothing filter	11b		Overlap smoothing on a per macroblock basis based on OVERFLAGS
	Value	Name	Description														
	00b		No overlap smoothing														
	01b		Reserved														
	10b		Always perform overlap smoothing filter														
	11b		Overlap smoothing on a per macroblock basis based on OVERFLAGS														
	28:26	PicType (Picture Type) This field specifies the coding type of the picture according to the Frame Coding Mode. When FCM = 00 01 (a Progressive or Interlaced Frame Picture):000 = I001 = P010 = B011 = BI100 = SkippedOther encodings are reservedWhen FCM = 10 11 (a Field Picture)000 = I/I001 = I/P010 = P/I011 = P/P100 = B/B101 = B/BI110 = BI/B111 = BI/BIAlthough, for a field picture, it is set for a field-pair, but HW will only look at one field state only, and the other field state is don't care. This field is read and qualified with the SecondField flag internally.This field is unique to intel VC1 VLD Long format, and is used in IT mode as well. For DXVA2 VC1 IT mode, driver needs to convert the DXVA2 interface to intel HW VLD Long Format interface.															
	25:24	FCM (Frame Coding Mode) This is the same as the variable FCM defined in VC1.This field must be set to 0 for Simple and Main ProfilesThis field is unique to intel VC1 VLD Long format, and is used in IT mode as well. For DXVA2 VC1 IT mode, driver needs to convert the DXVA2 interface to intel HW VLD Long Format interface. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>00b</td><td>Disable</td><td>Progressive Frame Picture</td></tr><tr><td>01b</td><td>Enable</td><td>Interlaced Frame Picture</td></tr><tr><td>10b</td><td></td><td>Field Picture with Top Field First</td></tr><tr><td>11b</td><td></td><td>Field Picture with Bottom Field First</td></tr></table>	Value	Name	Description	00b	Disable	Progressive Frame Picture	01b	Enable	Interlaced Frame Picture	10b		Field Picture with Top Field First	11b		Field Picture with Bottom Field First
Value	Name	Description															
00b	Disable	Progressive Frame Picture															
01b	Enable	Interlaced Frame Picture															
10b		Field Picture with Top Field First															
11b		Field Picture with Bottom Field First															
23:21	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ														
Format:	MBZ																
20:16	AltPQuant (Alternative Picture Quantization Value) This field is identical to the variable ALTPQUANT which is derived from VOPDQUANT configuration in the VC1 standard.This field must be set to 0 for Simple/Main I and BI pictures as VOPDQUANT is not present.This field is used in intel VC1 VLD Long Format mode only, not used in DXVA2 VC1 VLD and IT modes.																
15:13	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ														
Format:	MBZ																

**MFD_VC1_LONG_PIC_STATE**

MFD_VC1_LONG_PIC_STATE																
	12:8	PQuant (Picture Quantization Value)														
		Format:	U5													
		This is the same as the calculated variable PQUANT in VC1 standard where PQuant = PQINDEX, except when QUANTIZER = 0 and PQINDEX > 8, it is given asPQuant = (PQINDEX < 29) ? PQINDEX - 3 : PQINDEX*2 - 31This field is used in all picture types (I, P, B and BI) and all operating modes (IT mode and intel and DXVA2 VLD modes).														
	7:0	BScaleFactor BScaleFactorThis field is the scale factor for computing Direct-mode motion vectors. It is derived from the variable BFRACTION in the VC1 standard, section 8.4.5.4. There are only 21 valid values corresponding to the 21 encodings of BFRACTION as shown in the table here. Other values are reserved.MSB of this field can be used to determine if BFRACTION is greater than or equal to 1/2, which is used to determine Motion Prediction Type for B pictures. Effectively, condition "BFRACTION >= 1/2" is equivalent to condition "BScaleFactor >= 128".This field is only valid for B pictures. This field is used only in intel VC1 VLD Long format mode, it is not used in DXVA2 VC1 VLD and IT modes.BFRACTION VLCBFRACTIONBScaleFactor0001/21280011/3850102/31700111/4641003/41921011/5511102/510211100003/515311100014/520411100101/64311100115/621511101001/73711101012/77411101103/711111101114/714811110005/718511110016/722211110101/83211110113/89611111005/816011111017/8224														
4	31:30	Reserved														
		Format:	MBZ													
	29:28	UnifiedMvMode (Unified Motion Vector Mode) This field is a combination of the variables MVMODE and MVMODE2 in the VC1 standard, for parsing Luma MVD from the bitstream. This field is used to signal 1MV vs 4MVallowed (Mixed Mode). This field is also used to signal Q-pel or Half-pel MVD read from the bitstream. The bicubic or bilinear Luma MC interpolation mode is duplicate information from Motion Vector Mode field, and is ignored here.This field is used in intel VC1 VLD Long Format mode only, it is not used in DXVA2 VC1 VLD and IT modes.														
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>00b</td><td></td><td>Mixed MV, Q-pel bicubic</td></tr><tr><td>01b</td><td></td><td>1-MV, Q-pel bicubic</td></tr><tr><td>10b</td><td></td><td>1-MV half-pel bicubic</td></tr><tr><td>11b</td><td></td><td>1-MV half-pel bilinear</td></tr></table>	Value	Name	Description	00b		Mixed MV, Q-pel bicubic	01b		1-MV, Q-pel bicubic	10b		1-MV half-pel bicubic	11b	
Value	Name	Description														
00b		Mixed MV, Q-pel bicubic														
01b		1-MV, Q-pel bicubic														
10b		1-MV half-pel bicubic														
11b		1-MV half-pel bilinear														
27	FourMvSwitch (Four Motion Vector Switch) This field indicates if 4-MV is present for an interlaced frame P picture. It is identical to the variable 4MVSWITCH (4 Motion Vector Switch) in VC1 standard.This field is used in intel VC1 VLD Long Format mode only, it is not used in DXVA2 VC1 VLD and IT modes.															
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable</td><td>only 1-MV</td></tr><tr><td>1h</td><td>Enable</td><td>1, 2, or 4 MVs</td></tr></table>	Value	Name	Description	0h	Disable	only 1-MV	1h	Enable	1, 2, or 4 MVs					
	Value	Name	Description													
	0h	Disable	only 1-MV													
1h	Enable	1, 2, or 4 MVs														



MFD_VC1_LONG_PIC_STATE

26	FastUVMCFlag (Fast UV Motion Compensation Flag) This field specifies whether the motion vectors for UV is rounded to half or full pel position. It is identical to the variable FASTUVMC in VC1 standard.This field is used in both VLD and IT modes.It is derived from FASTUVMC = (bPicSpatialResid8 » 4) & 1 in both VLD and IT modes, and should have the same value as Motion Vector Mode LSBIt.		
	Value	Name	Description
	0h		no rounding
	1h		quarter-pel offsets to half/full pel positions
25	RefFieldPicPolarity (Reference Field Picture Polarity) This field specifies the polarity of the one reference field picture used for a field P picture. It is derived from the variable REFFIELD defined in VC1 standard and is only valid when one field is referenced (NUMREF = 0) for a field P picture.When NUMREF = 0 and REFFIELD = 0, this field is the polarity of the reference I/P field that is temporally closest; When NUMREF = 0 and REFFIELD = 1, this field is the polarity of the reference I/P field that is the second most temporally closest. The distance is measured based on display order but ignoring the repeated field if present (due to RFF = 1).This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.		
	Value	Name	Description
	0h		Top (even) field
	1h		Bottom (odd) field
24	NumRef (Number of References) This field indicates how many reference fields are referenced by the current (field) picture. It is identical to the variable NUMREF in the VC1 standard. This field is only valid for field P picture (FCM = 10 11).This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.		
	Value	Name	Description
	0h		One field referenced
	1h		Two fields referenced
23:20	BwdRefDist (Reference Distance) This field is valid only in B field pictures giving the value of BRFD. The field is ignored in P Picture.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.		
19:16	FwdRefDist (Reference Distance)		
	Format:		U4
	This field is the number of frames between the current frame and its reference frame. It is derived from the syntax element REFDIST (P Reference Distance) in the VC1 standard. 0 means that the previous frame is the reference frame.It has the same value as of FRFD for both P and B field pictures.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.		
	Value	Name	
	[0, 15]		

**MFD_VC1_LONG_PIC_STATE**

	15:12	Reserved	
		Format:	MBZ
	11:10	ExtendedDMVRange (Extended Differential Motion Vector Range Flag)	
		This field specifies the differential motion vector range in interlaced pictures. It is equivalent to the variable DMVRANGE in the VC1 standard. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.	
		Value	Name
		00b	No extended range
		01b	Extended horizontally
		10b	Extended vertically
		11b	Extended in both directions
	9:8	ExtendedMVRRange (Extended Motion Vector Range Flag)	
		This field specifies the motion vector range in quarter-pel or half-pel modes. It is equivalent to the variable MVRANGE in the VC1 standard. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes	
		Value	Description
		00b	[-256, 255] x [-128, 127]
		01b	512, 511] x [-256, 255]
		10b	[-2048, 2047] x [-1024, 1023]
		11b	[-4096, 4095] x [-2048, 2047]
	7:4	AltPQuantEdgeMask (Alternative Picture Quantization Edge Mask)	
		This field is a bit mask for the four edges in clock-wise order, indicating whether AltPQuant is used for the edge macroblocks. It is derived based on the following variables DQUANT, DQUANTFRM, DQPROFILE, DQSBEDGE, DQDBEDGE, and DQBILEVEL defined in the VC1 standard, as shown in Error! Reference source not found.. This field is valid only if AltPQuantConfig is 01. Bit 0: Left picture edge macroblocks Bit 1: Top picture edge macroblocks Bit 2: Right picture edge macroblocks Bit 3: Bottom picture edge macroblocks This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.	
	3:2	AltPQuantConfig (Alternative Picture Quantization Configuration)	
		This field specifies the way AltPQuant is used in the picture. It determines how to compute the macroblock quantizer step size, MQQUANT. It is derived based on the following variables DQUANT, DQUANTFRM, DQPROFILE, DQSBEDGE, DQDBEDGE, and DQBILEVEL defined in the VC1 standard, as shown in Error! Reference source not found.. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.	
		Value	Description
		00b	AltPQuant not used
		01b	AltPQuant is used and applied to edge macroblocks only
		10b	MQQUANT is encoded in macroblock layer
		11b	AltPQuant and PQuant are selected on macroblock basis



MFD_VC1_LONG_PIC_STATE

	1	HalfQP This field is used for inverse quantization of AC coefficients. It is valid only when PQuant is used.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.									
	0	PQuantUniform Indicating if uniform quantization applies to the picture. It is used for inverse quantization of the AC coefficients.QUANTIZER 001123PQUANTIZER - -01--PQINDEX>=9<=8---- PQuantUniform010201ImplicitQuantizer = 0, and PQuantUniform = 0 is used to represent 2 cases : 1) QUANTIZER=01 and PQUANTIZER=0; and 2) QUANTIZER = 10b.ImplicitQuantizer = 0, and PQuantUniform = 1 is used to represent 2 cases : 1) QUANTIZER=01 and PQUANTIZER=1; and 2) QUANTIZER = 11bThis field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td></td><td>Non-uniform</td></tr><tr><td>1h</td><td></td><td>Uniform</td></tr></table>	Value	Name	Description	0h		Non-uniform	1h		Uniform
	Value	Name	Description								
0h		Non-uniform									
1h		Uniform									
5	31	BitplanePresentFlag (Bitplane Buffer Present Flag) This field indicates whether the bitplane buffer is present for the picture. If set, at least one of the fields listed in bits 22:16 is coded in non-raw mode, and Bitplane Buffer Base Address field in the VC1_BSD_BUF_BASE_STATE command points to the bitplane buffer. Otherwise, all the fields that are applicable for the current picture in bits 22:16 must be coded in raw mode.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td></td><td>bitplane buffer is not present</td></tr><tr><td>1h</td><td></td><td>bitplane buffer is present</td></tr></table>	Value	Name	Description	0h		bitplane buffer is not present	1h		bitplane buffer is present
Value	Name	Description									
0h		bitplane buffer is not present									
1h		bitplane buffer is present									
	30	ForwardMbRaw This field indicates whether the FORWARDMB field is coded in raw or non-raw mode.This field is only valid when PictureType is B.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td></td><td>non-raw mode</td></tr><tr><td>1h</td><td></td><td>raw mode</td></tr></table>	Value	Name	Description	0h		non-raw mode	1h		raw mode
Value	Name	Description									
0h		non-raw mode									
1h		raw mode									
	29	MvTypeMbRaw This field indicates whether the MVTYPEPREMB field is coded in raw or non-raw mode.This field is only valid when PictureType is P.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td></td><td>Non-Raw Mode</td></tr><tr><td>1h</td><td></td><td>Raw Mode</td></tr></table>	Value	Name	Description	0h		Non-Raw Mode	1h		Raw Mode
Value	Name	Description									
0h		Non-Raw Mode									
1h		Raw Mode									

**MFD_VC1_LONG_PIC_STATE**

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SkipMbRaw

This field indicates whether the SKIPMB field is coded in raw or non-raw mode.This field is only valid when PictureType is P or B.0 = non-raw mode1 = raw modeThis field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.

Value	Name	Description
0h	Disable	Non-Raw Mode
1h	Enable	Raw Mode

27

DirectMbRaw

This field indicates whether the DIRECTMB field is coded in raw or non-raw mode.This field is only valid when PictureType is P or B.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.

Value	Name	Description
0h		Non-Raw Mode
1h		Raw Mode

26

OverflagsRaw

This field indicates whether the OVERFLAGS field is coded in raw or non-raw mode.This field is only valid when PictureType is I or BI.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.

Value	Name	Description
0h		Non-Raw Mode
1h		Raw Mode

25

AcPredRaw

This field indicates whether the ACPRED field is coded in raw or non-raw mode.This field is only valid when PictureType is I or BI.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.

Value	Name	Description
0h	Disable	Non-Raw Mode
1h	Enable	Raw Mode

24

FieldTxRaw

This field indicates whether the FIELDTX field is coded in raw or non-raw mode.This field is only valid when PictureType is I or BI.This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.

Value	Name	Description
0h	Disable	Non-Raw Mode
1h	Enable	Raw Mode

23

Reserved

Format:	MBZ



MFD_VC1_LONG_PIC_STATE

22:20	MvTab (Motion Vector Table)
Format:	U3
This field specifies which motion vector table(s) is (are) used for motion vector (differential) decoding in a P or B picture. This field is the combination of the variables MVTAB and IMVTAB in the VC1 standard. Two bits are defined for progressive frame pictures; And two or three bits are defined for interlaced field/frame pictures depending on NUMREF and P or B picture types. This field is valid for P and B pictures. It is not valid for I pictures. For P or B progressive frame pictures 0 = Motion Vector Differential VLD Table 01 = Motion Vector Differential VLD Table 12 = Motion Vector Differential VLD Table 23 = Motion Vector Differential VLD Table 3. The other encodings are reserved. For P interlace field pictures with NUMREF = 0 or P/B interlace frame pictures 0 = 1-Reference Table 01 = 1-Reference Table 12 = 1-Reference Table 23 = 1-Reference Table 3. The other encodings are reserved. For P interlace field picture with NUMREF = 1 or B interlaced field pictures 0 = 2-Reference Table 01 = 2-Reference Table 12 = 2-Reference Table 23 = 2-Reference Table 34 = 2-Reference Table 45 = 2-Reference Table 56 = 2-Reference Table 67 = 2-Reference Table 7. The other encodings are reserved. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.	
19:18	FourMvBpTab (4-MV Block Pattern Table)
This field specifies which table is used to decode the 4-MV block pattern (4MVBPTAB) syntax element in 4-MV macroblocks. It is identical to the variables 4MVBPTAB in the VC1 standard, section 9.1.1.37. This field is valid only in interlace frame P, B pictures, or interlace field P, B pictures. It is not valid for I picture. For interlace field P and B pictures, it is only valid if UnifiedMvMode is equal to Mixed-MV Type. For interlace frame P picture, it is only valid if FourMvSwitch is 1. For interlace frame B picture, it is always valid. 0 = 4MVBPTAB Table 01 = 4MVBPTAB Table 12 = 4MVBPTAB Table 23 = 4MVBPTAB Table 3. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.	
17:16	TwoMvBpTab (2MV Block Pattern Table)
This field specifies which table is used to decode the 2MV block pattern (2MVBPTAB) syntax element in 2MV field macroblocks. It is identical to the variables 2MVBPTAB in the VC1 standard, section 9.1.1.36. This field is valid only in interlace frame P/B pictures. It is not valid for I picture, nor for interlace field P or B pictures. 0 = 2MVBPTAB Table 01 = 2MVBPTAB Table 12 = 2MVBPTAB Table 23 = 2MVBPTAB Table 3. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.	
15:14	Reserved
Format:	MBZ
13:12	TransType (Picture-level Transform Type)
Format:	U2
This field specifies the Transform Type at picture level. It is identical to the variable TTFRM in the VC1 standard, section 7.1.1.41. This field is only valid when TransTypeMbFlag is 1. Otherwise, it is reserved and MBZ. This field is set to 00 when VSTRANSFORM is 0 in the entry point layer. 00 = 8x8 Transform 01 = 8x4 Transform 10 = 4x8 Transform 11 = 4x4 Transform. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.	

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	11	TransTypeMbFlag (Macroblock Transform Type Flag) This field indicates whether Transform Type is fixed at picture level or variable at macroblock level. It is identical to the variable TTMBF in the VC1 standard, section 7.1.1.40. This field is set to 1 when VSTRANSFORM is 0 in the entry point layer. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td></td><td>variable transform type in macroblock layer</td></tr><tr><td>1h</td><td></td><td>use picture level transform type TransType</td></tr></table>	Value	Name	Description	0h		variable transform type in macroblock layer	1h		use picture level transform type TransType
Value	Name	Description									
0h		variable transform type in macroblock layer									
1h		use picture level transform type TransType									
	10:8	MbModeTab (Macroblock Mode Table) This field signals which code table is used to decode the macroblock mode syntax element (MBMODE) in the macroblock layer in a P or B picture. This field is identical to the variables MBMODETAB in the VC1 standard, section 9.1.1.33. This field is valid for interlace frame P, B picture and interlace field P, B picture. It is not valid for I picture, nor progressive frame P, B pictures. Two bits are defined for interlace frame P, B pictures; And three bits are defined for interlaced field P, B pictures. Two bits are defined for interlace frame P, B pictures. There are two set of code tables selected based on if UnifiedMvMode is equal to 4-MV Type or not. 0 = Code Table 01 = Code Table 12 = Code Table 23 = Code Table 30 Other encodings are invalid Three bits are defined for interlace field P, B pictures. There are two set of code tables selected based on if UnifiedMvMode is equal to Mixed-MV Type or not. 0 = Code Table 01 = Code Table 12 = Code Table 23 = Code Table 34 = Code Table 45 = Code Table 56 = Code Table 67 = Code Table 7 This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.									
	7:6	TransAcY (Picture-level Transform Luma AC Coding Set Index, TRANSACTABLE2) BitFieldDesc									
	5:4	TransAcUV (Picture-level Transform Chroma AC Coding Set Index, TRANSACTABLE) This field, together with PQINDEX, specifies which intra AC coding set to be used for decoding the non-zero AC coefficients in a coded luma (Y) block. This field is the combination of the variables TRANSACFRM and TRANSACFRM2 in the VC1 standard. For I pictures, TransAcY is the same as TRANSACFRM2. For other pictures, it is the same as TRANSACFRM, and therefore must be programmed to be the same as TransAcUV. This field is valid for all picture types. 0 = Coding set index 01 = Coding set index 12 = Coding set index 23 is invalid This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.									
	3	TransDcTab (Intra Transform DC Table) This field specifies whether the low motion tables or the high motion tables are used to decode the Transform DC coefficients in intra-coded blocks. This field is identical to the variable TRANSDCTAB in the VC1 standard, section 8.1.1.2. This field is valid for all picture types. This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td></td><td>The high motion tables</td></tr><tr><td>1h</td><td></td><td>The low motion tables</td></tr></table>	Value	Name	Description	0h		The high motion tables	1h		The low motion tables
Value	Name	Description									
0h		The high motion tables									
1h		The low motion tables									



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	2:0	CbpTab (Coded Block Pattern Table) This field specifies the table used to decode the CBPCY syntax element for each coded macroblock in P and B pictures. This field is combination of the variable CBPTAB for P and B frame pictures and the variable ICBPTAB in interlace field P, B pictures and interlace frame P, B pictures in the VC1 standard (Table 52 and Table 102). This field is reserved and MBZ for I or BI pictures as I only has a fixed table. 000 = Table 0 (Table 169 for P, B frames or Table 124 otherwise) 001 = Table 1 (Table 170 for P, B frames or Table 125 otherwise) 010 = Table 2 (Table 171 for P, B frames or Table 126 otherwise) 011 = Table 3 (Table 172 for P, B frames or Table 127 otherwise) 100 = Table 4 (Table 128 for interlace field/frame P, B pictures) 101 = Table 5 (Table 129 for interlace field/frame P, B pictures) 110 = Table 6 (Table 130 for interlace field/frame P, B pictures) 111 = Table 7 (Table 131 for interlace field/frame P, B pictures) This field is unique to intel VC1 VLD Long format mode, and is not used in IT and DXVA2 VC1 modes.



MFD_VC1_SHORT_PIC_STATE

MFD_VC1_SHORT_PIC_STATE		
Source:		VideoCS
Length Bias:		2
DWord	Bit	Description
0	31:29	Command Type
		Default Value: 3h PARALLEL_VIDEO_PIPE
	28:27	Format: OpCode
		Pipeline
	26:24	Default Value: 2h MFD_VC1_SHORT_PIC_STATE
		Format: OpCode
	23:21	Media Command Opcode
		Default Value: 2h VC1_DEC
1	20:16	Format: OpCode
		SubOpcode A
	15:12	Default Value: 1h
		Format: OpCode
	11:0	SubOpcode B
		Default Value: 0h
	31:24	Format: MBZ
		Reserved
	23:16	Format: U8-1 Picture Height in Macroblocks
		Picture Height This field indicates the height of the picture in unit of macroblocks. For example, for a 1920x1080 frame picture, PictureHeightInMBs equals 68 (1080 divided by 16, and rounded up, i.e. effectively specified as 1088 instead). This field is used in VLD and IT modes. Note: Even though the Advanced Profile allows frame dimensions (width, height) to not be aligned to macroblock boundary, it doesn't affect the bitstream decoding. And it is preferable to use 'intermediate buffer' that is macroblock aligned for decoding. In order to simplify the out-of-bound reference pixel access, the out-of-bound extrapolation rule in VC1 spec can be used to expand the expected decoded frame to the intermediate buffer dimension.



MFD_VC1_SHORT_PIC_STATE													
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[0,127]</td><td>Value_0_to_127</td><td>[1, 128] MB</td></tr><tr><td>[128,255]</td><td>Value_128_to_255</td><td></td></tr></table>	Value	Name	Description	[0,127]	Value_0_to_127	[1, 128] MB	[128,255]	Value_128_to_255			
	Value	Name	Description										
	[0,127]	Value_0_to_127	[1, 128] MB										
	[128,255]	Value_128_to_255											
	15:8	Reserved											
		Format:	MBZ										
	7:0	Picture Width											
		Format:	U8-1 Picture Width in Macroblocks										
		This field indicates the width of the picture in unit of macroblocks. For example, for a 1920x1080 frame picture, PictureWidthInMBs equals 120 (1920 divided by 16).This field is used in VLD and IT modes.											
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[0,127]</td><td>Value_0_to_127</td><td>[1, 128] MB</td></tr><tr><td>[128,255]</td><td>Value_128_to_255</td><td></td></tr></table>	Value	Name	Description	[0,127]	Value_0_to_127	[1, 128] MB	[128,255]	Value_128_to_255			
	Value	Name	Description										
[0,127]	Value_0_to_127	[1, 128] MB											
[128,255]	Value_128_to_255												
2	31:24	Bitplane Buffer Pitch Minus 1											
		Format:	U7-1 Pitch in Bytes										
		Specifies the bitplane buffer pitch in (#Bytes - 1). Bitplane buffer is a linear buffer. It is needed only when the bitplane is not encoded as raw, and therefore is present in the header explicitly. In VC1 Long Format (Gen6 and Gen7), it is written by an application and later read by the HW. In VC1 Long Format (Gen6 and Gen7), it is written by an application, and later read by the HW. But in VC1 Short Format (Gen7 only), it is written and read by H/W only.This field is specified for better performanceFor Gen6 : The pitch must be equal to PictureWidthInMBs/2.For Gen7 VC1 Long Format : The pitch must be equal to PictureWidthInMBs/2.For Gen7 VC1 Short Format : If Pic Width is less than or equal to 2K pixels, bitplane pitch is set to 64 (one cacheline; programmed as 63) bytes per MB row. If Pic Width is greater than 2K pixels, bitplane pitch is set to 128 (two cachelines; programmed as 127) bytes per MB row.This field is not used in IT mode, used in VLD mode only.For VC1 DXVA2 Short Format, the bitplane specification is between H/W and Driver only. For Long Format, application is responsible for allocation with the driver.											
	23	Interpolation Rounder Control											
		Used only in MC operation. This field specifies the rounding control value used in interpolation operation of motion prediction process. Note: This bit field is taken from bRcontrol in DXVA_PictureParameters data structure This field is used in VLD and IT modes.											
	22:20	Reserved											
	Format:	MBZ											
19:16	Motion Vector Mode												
	This field indicates one of the following motion compensation interpolation modes for P and B pictures. The MC interpolation modes apply to prediction values of luminance blocks and are always in quarter-sample. For chrominance blocks, it always performs bilinear interpolation with either half-pel or quarter-pel precision.0XX0 = Chroma Quarter -pel + Luma bicubic. (can only be 1MV)0XX1 = Chroma Half-pel + Luma bicubic. (can be 1MV or 4MV)1XX0 = Chroma Quarter -pel + Luma bilinear. (can only be 1MV)1XX1 = Chroma Half-pel + Luma bilinearNote: Bits 19:16 are												

**MFD_VC1_SHORT_PIC_STATE**

MFD_VC1_SHORT_PIC_STATE											
		taken from bMVPrecisionAndChromaRelation in DXVA_PictureParameters data structure.Bit 19 of Motion Vector Mode = 1 for Luma Bilinear MC; = 0 for Luma Bicubic MCBit 16 of Motion Vector Mode = 1 for half-sample Chroma motion = 0 for quarter-sample Chroma motion.This field is used in both VLD and IT modes.Before the polarity of Chroma Half-pel or Q-pel is reversed from DXVA2 Spec, now I have fixed it to match with DXVA2 VC1 Spec. ???									
15	DmvSurfaceValid	Indicated when the DMV read surface is valid. This surface stored the direct motion vectors. This field is set fo B pictures that can refer to a previous P picture for DMV. If there is an I-picture before a B (in decoding order) then this field is not set (as a result, zero's DMV's will be assumed while decoding the B picture. That is, there is no explicit DMV buffer for an I-picture). This field is not used in IT mode, used in VLD mode only.									
14:12	Reserved	<table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ							
Format:	MBZ										
11	VC1 Profile	specifies the bitstream profile. Note: This is required because 128 is added for intra blocks post inverse transform in advanced profile and also to find out if Motion vectors are adjusted or not. This field is used in both VLD and IT modes. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>[Default]</td><td>current picture is in Simple or Main Profile (No need to distinguish Simple and Main Profile)</td></tr><tr><td>1h</td><td></td><td>current picture is in Advanced Profile</td></tr></table>	Value	Name	Description	0h	[Default]	current picture is in Simple or Main Profile (No need to distinguish Simple and Main Profile)	1h		current picture is in Advanced Profile
Value	Name	Description									
0h	[Default]	current picture is in Simple or Main Profile (No need to distinguish Simple and Main Profile)									
1h		current picture is in Advanced Profile									
10:6	Reserved	<table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ							
Format:	MBZ										
5	Backward Prediction Present Flag	Note : a B picture that only uses forward prediction may have this flag set to 1 as well. Driver may still need to provide a valid reference picture index. This field is used in both DXVA2 VC1 VLD mode and IT mode. It is the same parameter as bPicBackwardPrediction in DXVA2 VC1 spec. The Intra Picture Flag, Backward Prediction Present Flag and RefPicFlag are used to derive the picture type, as specified in PTYPE for a frame, and in FPTYPE for a field, in DXVA2 VC1 VLD and IT mode.									
4	Intra Picture Flag	This field is used in both DXVA2 VC1 VLD mode and IT mode. It is the same parameter as bPicIntra in DXVA2 VC1 spec. The Intra Picture Flag, Backward Prediction Present Flag and RefPicFlag are used to derive the picture type, as specified in PTYPE for a frame, and in FPTYPE for a field, in DXVA2 VC1 VLD and IT mode. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td></td><td>entire picture can have a mixture of intra and inter MB type or just inter MB type.</td></tr></table>	Value	Name	Description	0h		entire picture can have a mixture of intra and inter MB type or just inter MB type.			
Value	Name	Description									
0h		entire picture can have a mixture of intra and inter MB type or just inter MB type.									



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		1h		entire picture is coded in intra MB type														
	3	SecondField This flag is set for the second field in field pictures.This field is used in both VLD and IT modes.																
	2	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>			Format:	MBZ												
	Format:	MBZ																
	1:0	Picture Structure This field is used in both DXVA2 VC1 VLD mode and IT mode. It is the same parameter as bPicStructure in DXVA2 VC1 spec. The Picture Structure and Progressive Pic Type are used to derive the picture structure as specified in FCM, in DXVA2 VC1 VLD and IT mode. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>01b</td><td></td><td>top field (bit 0)</td></tr><tr><td>10b</td><td></td><td>bottom field (bit 1)</td></tr><tr><td>11b</td><td></td><td>frame (both fields are present)</td></tr><tr><td>00b</td><td></td><td>illegal</td></tr></table>			Value	Name	Description	01b		top field (bit 0)	10b		bottom field (bit 1)	11b		frame (both fields are present)	00b	
Value	Name	Description																
01b		top field (bit 0)																
10b		bottom field (bit 1)																
11b		frame (both fields are present)																
00b		illegal																
3	31	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>			Format:	MBZ												
	Format:	MBZ																
	30	Overlap Smoothing Enable Flag This field is the decoded syntax element OVERLAP in bitstreamIndicates if Overlap smoothing is ON at the picture levelThis field is used in both VLD and IT modes <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable</td><td>to disable overlap smoothing filter</td></tr><tr><td>1h</td><td>Enable</td><td>to enable overlap smoothing filter</td></tr></table>			Value	Name	Description	0h	Disable	to disable overlap smoothing filter	1h	Enable	to enable overlap smoothing filter					
	Value	Name	Description															
0h	Disable	to disable overlap smoothing filter																
1h	Enable	to enable overlap smoothing filter																
29	Range Reduction Scale <table><tr><td>Access:</td><td>None</td></tr></table> This field specifies whether the reference picture pixel values should be scaled up or scaled down on-the-fly, if RangeReduction is Enabled.NOTE: This bit is derived by driver for Main Profile only. Ignored in Simple and Advanced Profiles. This field is used in both VLD and IT modes.This is derived by driver from the history of RANGERED and RANGEREDFRM syntax elements (i.e. of forward/preceding reference picture) and those of the current picture. RANGERED is the same as (bPicOverflowBlocks » 3) & 1. RANGEREDFRM is the same as (bPicDeblocked » 5) & 1. For the current picture is a B picture, this field represents the state of the forward/preceding reference picture onlyDriver is responsible to keep RangeReductionScale, RangeReduction Enable and RANGERED Present Flag of current picture coherent. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable [Default]</td><td>Scale down reference picture by factor of 2</td></tr><tr><td>1h</td><td>Enable</td><td>Scale up reference picture by factor of 2</td></tr></table>			Access:	None	Value	Name	Description	0h	Disable [Default]	Scale down reference picture by factor of 2	1h	Enable	Scale up reference picture by factor of 2				
Access:	None																	
Value	Name	Description																
0h	Disable [Default]	Scale down reference picture by factor of 2																
1h	Enable	Scale up reference picture by factor of 2																

**MFD_VC1_SHORT_PIC_STATE**

28

Range Reduction Enable

This field specifies whether on-the-fly pixel value range reduction should be performed for the preceding (or forward) reference picture. Along with RangeReductionScale to specify whether scale up or down should be performed. It is not the same value as RANGEREDFRM Syntax Element (DXVA_PictureParameters bPicDeblocked bit 5) in the Picture Header. This field is for Main Profile only. Simple Profile is always disable, and not applicable to Advanced Profile. This field is used in both VLD and IT modes. This is derived by driver from the history of RANGERED and RANGEREDFRM syntax elements (i.e. of forward/preceding reference picture) and those of the current picture. RANGERED is the same as (bPicOverflowBlocks » 3) & 1. RANGEREDFRM is the same as (bPicDeblocked » 5) & 1. For the current picture is a B picture, this field represents the state of the forward/preceding reference picture only. Driver is responsible to keep RangeReductionScale, RangeReduction Enable and RANGERED Present Flag of current picture coherent.

Value	Name	Description
0h	Disable [Default]	Range reduction is not performed
1h	Enable	Range reduction is performed

27:24

Reserved

Format:	MBZ

23:22

Progressive Pic Type

This field is used in both DXVA2 VC1 VLD mode and IT mode. It is the same parameter as bPicExtrapolation in DXVA2 VC1 spec. The Picture Structure and Progressive Pic Type are used to derive the picture structure as specified in FCM, in DXVA2 VC1 VLD and IT mode.

Value	Name	Description
0		progressive only picture
1		progressive only picture
2		interlace picture (frame-interlace or field-interlace)
3		illegal

21

Reserved

Format:	MBZ

20:16

P-Pic Ref Distance

Access:

None

This element defines the number of frames between the current frame and the reference frame. It is the same as the REFDIST SE in VC1 interlaced field picture header. It is present if the entry-level flag REFDIST_FLAG == 1, and if the picture type is not one of the following types: B/B, B/BI, BI/B, BI/BI. If the entry level flag REFDIST_FLAG == 0, REFDIST shall be set to the default value of 0. This field is used in DXVA2 VC1 VLD mode only, not used in IT and intel VC1 VLD Long Format modes.

Value	Name
0-16	unsigned integer
0h	[Default]



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	15:14	QUANTIZER		
		Value	Name	Description
		00b		implicit quantizer at frame leve
		01b		explicit quantizer at frame level, and use PQUANTIZER SE to specify uniform or non-uniform
		10b		explicit quantizer, and non-uniform quantizer for all frames
		11b		explicit quantizer, and uniform quantizer for all frames
	13	MULTIRES Present Flag (for Simple/Main Profile only)		
		Value	Name	Description
		0h		RESPIC Parameter is present in the picture header
		1h		RESPIC Parameter is present in the picture header
	12	SYNCMARKER Present Flag (for Simple/Main Profile only)		
		Value	Name	Description
		0		Bitstream for Simple and Main Profile has no sync marker
		1		Bitstream for Simple and Main Profile may have sync marker(s)
	11	RANGERED Present Flag (for Simple/Main Profile only)		
		It is needed for Picture Header Parsing.Driver is responsible to keep RangeReductionScale, RangeReduction Enable and RANGERED Present Flag of current picture coherent.		
		Value	Name	Description
		0		Range Reduction Parameter (RANGEREDFRM) is not present in the picture header
	10:8	1		Range Reduction Parameter (RANGEREDFRM) is present in the picture header.
		MAXBFRAMES Number of consecutive B Frames.		
	7	PANSCAN Present Flag		
		Value	Name	Description
		0		Pan Scan Parameters are not present in the picture header
		1		Pan Scan Parameters are present in the picture header
	6	REFDIST_FLAG For header parsing REFDIST.This is used in DXVA2 VC1 VLD mode only, not used in IT and intel VC1 VLD modes.		
	5	LOOPFILTER Enable Flag This filed is the decoded syntax element LOOPFILTER in bitstream. It indicates if In-loop Deblocking is ON according to picture level bitstream syntax control. This bit affects BSD unit and also the loop filter unit.When this bit is set to 1, PostDeblockOutEnable field in MFX_PIPE_MODE_SELECT command must also be set to 1. In this case, in-loop deblocking operation follows the VC1 standard - deblocking doesn't cross slice boundary.When this bit is set to 0, but PostDeblockOutEnable field in MFX_PIPE_MODE_SELECT command is set to 1. It		

**MFD_VC1_SHORT_PIC_STATE**

		indicates the loop filter unit is used for out-of-loop deblocking. In this case, deblocking operation does cross slice boundary.This field is used in VLD mode only, not in IT mode.																									
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td></td><td>In-Loop-Deblocking-Filter is disabled</td></tr><tr><td>1</td><td></td><td>In-Loop-Deblocking-Filter is enabled</td></tr></table>	Value	Name	Description	0		In-Loop-Deblocking-Filter is disabled	1		In-Loop-Deblocking-Filter is enabled																
Value	Name	Description																									
0		In-Loop-Deblocking-Filter is disabled																									
1		In-Loop-Deblocking-Filter is enabled																									
	4	FastUVMCFlag (Fast UV Motion Compensation Flag) This field specifies whether the motion vectors for UV is rounded to half or full pel position. It is identical to the variable FASTUVMC in VC1 standard.This field is used in both VLD and IT modes.It is derived from FASTUVMC = (bPicSpatialResid8 » 4) & 1 in both VLD and IT modes, and should have the same value as Motion Vector Mode LSBIt.																									
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td></td><td>no rounding</td></tr><tr><td>1h</td><td></td><td>quarter-pel offsets to half/full pel positions</td></tr></table>	Value	Name	Description	0h		no rounding	1h		quarter-pel offsets to half/full pel positions																
Value	Name	Description																									
0h		no rounding																									
1h		quarter-pel offsets to half/full pel positions																									
	3	EXTENDED_MV Present Flag BitFieldDesc																									
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td></td><td>Extended_MV is not present in the picture header</td></tr><tr><td>1h</td><td></td><td>Extended_MV is present in the picture header</td></tr></table>	Value	Name	Description	0h		Extended_MV is not present in the picture header	1h		Extended_MV is present in the picture header																
Value	Name	Description																									
0h		Extended_MV is not present in the picture header																									
1h		Extended_MV is present in the picture header																									
	2:1	DQUANT <table><tr><td colspan="2">Access:</td><td>None</td></tr><tr><td colspan="2">Format:</td><td>U2</td></tr></table> Use for Picture Header Parsing of VOPDUANT elements <table><tr><th>Value</th><th colspan="2">Name</th></tr><tr><td>0h</td><td>[Default]</td><td></td></tr><tr><td>00b</td><td></td><td>no VOPDQUANT elements; Quantizer cannot vary in frame, same quantization step size PQUANT is used for all MBs in the frame</td></tr><tr><td>01b</td><td></td><td>refer to VC1 Spec. for all the MB position dependent quantizer selection</td></tr><tr><td>10b</td><td></td><td>The macroblocks located on the picture edge boundary shall be quantized with ALTPQUANT while the rest of the macroblocks shall be quantized with PQUANT.</td></tr><tr><td>11b</td><td>Reserved</td><td></td></tr></table>		Access:		None	Format:		U2	Value	Name		0h	[Default]		00b		no VOPDQUANT elements; Quantizer cannot vary in frame, same quantization step size PQUANT is used for all MBs in the frame	01b		refer to VC1 Spec. for all the MB position dependent quantizer selection	10b		The macroblocks located on the picture edge boundary shall be quantized with ALTPQUANT while the rest of the macroblocks shall be quantized with PQUANT.	11b	Reserved	
Access:		None																									
Format:		U2																									
Value	Name																										
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10b		The macroblocks located on the picture edge boundary shall be quantized with ALTPQUANT while the rest of the macroblocks shall be quantized with PQUANT.																									
11b	Reserved																										
	0	VSTRANSFORM flag <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable</td><td>variable-sized transform coding is not enabled</td></tr><tr><td>1h</td><td>Enable</td><td>variable-sized transform coding is enabled</td></tr></table>		Value	Name	Description	0h	Disable	variable-sized transform coding is not enabled	1h	Enable	variable-sized transform coding is enabled															
Value	Name	Description																									
0h	Disable	variable-sized transform coding is not enabled																									
1h	Enable	variable-sized transform coding is enabled																									
4	31:29	Reserved <table><tr><td>Format:</td><td>MBZ (for possible future change to BFraction Enumeration)</td></tr></table>		Format:	MBZ (for possible future change to BFraction Enumeration)																						
Format:	MBZ (for possible future change to BFraction Enumeration)																										



MFD_VC1_SHORT_PIC_STATE

28:24	BFraction Enumeration This field is the scale factor for computing Direct-mode motion vectors. It is derived from the variable BFRACTION in the VC1 standard, section 8.4.5.4. There are only 21 valid values corresponding to the 21 encodings of BFRACTION as shown in the table here. Other values are reserved. The VLD decoded value of BFRACTION (from the picture header) is mapped into an enum value from 0 to 20. (??? MSB of this field can be used to determine if BFRACTION is greater than or equal to 1/2, which is used to determine Motion Prediction Type for B pictures. Effectively, condition "BFRACTION >= 1/2" is equivalent to condition "ScaleFactor >= 128". ??? How can the enum replicate this feature ???) This field is only valid for B pictures. This field is used only in DXVA2 VC1 VLD mode, it is not used in Intel VC1 VLD Long Format mode and IT mode. BFRACTION VLCBFRACTION Enum 0001/200011/310102/320111/431003/441011/551102/5611100003/5711100014/5811100101/6911100115/61011101001/71111101012/71211101103/71311101114/71411110005/71511110016/71611110101/81711110113/81811111005/81911111017/82011111111BI Pic Indicator31 (optional)
23	Reserved Format: MBZ Advanced Profile only; RANGE_MAPY_FLAG Range Mapping not supported
22:20	Reserved Format: MBZ Advanced Profile only; RANGE_MAPY Range Mapping not supported
19	Reserved Format: MBZ Advanced Profile only; RANGE_MAPUV_FLAG Range Mapping not supported
18:16	Reserved Format: MBZ Advanced Profile only; RANGE_MAPUV Range Mapping not supported
15:9	Reserved Format: MBZ
8	4MV Allowed Flag
7	POSTPROC Flag
6	PULLDOWN
5	INTERLACE
4	TFCNTRFLAG
3	FINTERFLAG
2	REFPIC Flag For a BI picture, REFPIC flag must set to 0. For I and P picture, REFPIC flag must set to 0. For a B picture, REFPIC flag must set to 0, except for a B-field in interlaced field mode which can be 0 or 1 (e.g. the top B field can be used as a reference for decoding its corresponding bottom B-field in a field pair). In VLD mode, this flag cannot be used as an optimization signaling for an I or P picture that is not used as a reference picture. This field is used in both DXVA2 VC1 VLD mode and IT mode. It is the same parameter as bPicDeblockConfined[bit2] in DXVA2 VC1 spec. The Intra Picture Flag, Backward Prediction Present Flag and RefPicFlag are used to derive the picture type, as specified in PTYPE for a frame, and in FPTYPE for a field, in DXVA2 VC1 VLD and IT mode.



MFD_VC1_SHORT_PIC_STATE				
		Value	Name	Description
		0h		the current picture after decoded, will never used as a reference picture
		1h		the current picture after decoded, will be used as a reference picture later
	1	PSF		
	0	EXTENDED_DMV Present Flag		
		Value	Name	Description
		0h	[Default]	Extended_DMV is not present in the picture header
		1h		Extended_DMV is present in the picture header



MFX_AVC_IMG_STATE

MFX_AVC_IMG_STATE			
Source:		VideoCS	
Length Bias:		2	
This must be the very first command to issue after the surface state, the pipe select and base address setting commands. This command supports both Long and Short VLD and IT DXVA2 AVC Decoding Interface.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	Pipeline	
		Default Value:	2h MFX_AVC_IMG_STATE
		Format:	OpCode
	26:24	Media Command Opcode	
		Default Value:	1h AVC_COMMON
		Format:	OpCode
	23:21	SubOpcode A	
		Default Value:	0h
		Format:	OpCode
	20:16	SubOpcode B	
		Default Value:	0h
Format:		OpCode	
15:12	Reserved		
	Format:	MBZ	
11:0	DWord Length		
	Default Value:	0Ch Excludes DWord (0,1)	
	Format:	=n 00Eh, used for normal decode and encode mode000h, a special case to provide a dummy image state for stitch mode operation. In this case, fields in DW1 which is part of the dummy image state command are ignored by hardware.	
1	31:16	Reserved	
		Format:	MBZ

**MFX_AVC_IMG_STATE**

MFX_AVC_IMG_STATE				
	15:0	Frame Size		
		Format: U16 in MB unit		
		This field is only valid for encoder. Its ignored for decoder.The value for FrameSizeInMBs must match the product of FrameWidthInMBs and FrameHeightInMBs. For encode mode if frame size is 4Kx4K, then we need to specify 65535 in this field as we dont have enough bits to specify 65536. This is used only for cabac zero work insertion when in encode mode.		
		Value	Name	Description
		[1,65535]		representing Number of MBs [1,65535]
2	31:24	Reserved		
		Format: MBZ		
		(bit[31:24] must be zero to match the DXVA 16-bit definition for FrameHeightInMBsMinus1)		
	23:16	Frame Height		
		Format: U8-1 in MB unit		
		It is set to the value of (FrameHeightInMBsMinus1+ 1). Since the max value for FrameHeightInMBs is 255, the max allowed value for FrameHeightInMBsMinus1 is only 254. The min value for FrameHeightInMBs is 1.Although the max. value that can be specified for FrameHeightInMBs is 255 (in the current implementation), FrameWidthInMBs * FrameHeightInMBs must not exceed the max value of FrameSizeInMBs[14:0].e.g. for 1920x1080, FrameHeightInMBs[7:0] is equal to 68 (1080 divided by 16, and rounded up, i.e. effectively specified as 1088 instead).It is derived from FrameHeightInMbs = (2 - frame_mbs_only_flag) * PicHeightInMapUnits and PicHeightInMbs = FrameHeightInMbs / (1 + field_pic_flag) internally done. For MBAFF, PicHeightInMapUnits is in MB pair unit, so the bitstream sends only half frame height.		
		Value	Name	Description
		[0,255]		representing height [1,256]
	15:8	Reserved		
		Format: MBZ		
(bit[15:8] must be zero to match the DXVA 16-bit definition for FrameWidthInMBsMinus1)				
7:0	Frame Width			
	Format: U8-1 in MB unit			
	It is set to the value of (FrameWidthInMBsMinus1+ 1). Since the max value for FrameWidthInMBs is 255, the max allowed value for FrameWidthInMBsMinus1 is only 254. The min value for FrameWidthInMBs is 1.Although the max. value that can be specified for FrameWidthInMBs is 255 (in the current implementation), FrameWidthInMBs * FrameWidthInMBs must not exceed the max value of FrameSizeInMBs[14:0].e.g. for 1920x1080, FrameHeightInMBs[7:0] is equal to 68 (1080 divided by 16, and rounded up, i.e. effectively specified as 1088 instead).It is derived from FrameWidthInMbs = (2 - frame_mbs_only_flag) * PicWidthInMapUnits and			



MFX_AVC_IMG_STATE													
		PicWidthInMbs = FrameWidthInMbs / (1 + field_pic_flag) internally done. For MBAFF, PicWidthInMapUnits is in MB pair unit, so the bitstream sends only half frame width. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[0,255]</td><td></td><td>representing width [1,256]</td></tr></table>	Value	Name	Description	[0,255]		representing width [1,256]					
Value	Name	Description											
[0,255]		representing width [1,256]											
3	31:29	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table> (bit[31:29] must be zero to match the DXVA2 8-bit definition for InitQpChroma[1])	Format:	MBZ									
	Format:	MBZ											
	28:24	Second Chroma QP Offset Signed integer value. It should be in the range of -12 to +12 (according to AVC spec).It specifies the offset for determining QP Cr from QP Y. It is set to the upper 5 bits of the value of the syntax element (Chroma_qp_offset[9:0]) read from the current active PPS.Chroma_qp_offset [4:0] - chroma_qp_offset_bits (from the current active PPS)Chroma_qp_offset [9:5] - second_chroma_qp_offset_bits											
	23:21	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table> (bit[23:21] must be zero to match the DXVA2 8-bit definition for InitQpChroma[1])	Format:	MBZ									
	Format:	MBZ											
	20:16	First Chroma QP Offset Signed integer value. It should be in the range of -12 to +12 (according to AVC spec).It specifies the offset for determining QP Cb from QP Y. It is set to the lower 5 bits of the value of the syntax element (Chroma_qp_offset[9:0]) read from the current active PPS.Chroma_qp_offset [4:0] - chroma_qp_offset_bits (from the current active PPS)Chroma_qp_offset [9:5] - second_chroma_qp_offset_bits											
	15:14	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ									
	Format:	MBZ											
	13	RhoDomain Rate Control Enable <table><tr><td>Format:</td><td>Enable</td></tr></table> This field indicates if RhoDomain related parameters are present in the MFX_AVC_IMAGE_STATE. (AverageMacroblockQP). It enables the Rho Domain statistics collection. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>Disable</td><td>RhoDomain rate control parameters are not present in MFX_AVC_IMAGE_STATE</td></tr><tr><td>1</td><td>Enable</td><td>RhoDomain rate control parameters are present in MFX_AVC_IMAGE_STATE.</td></tr></table> Programming Notes This field must set to '0' for B pictures.	Format:	Enable	Value	Name	Description	0	Disable	RhoDomain rate control parameters are not present in MFX_AVC_IMAGE_STATE	1	Enable	RhoDomain rate control parameters are present in MFX_AVC_IMAGE_STATE.
	Format:	Enable											
Value	Name	Description											
0	Disable	RhoDomain rate control parameters are not present in MFX_AVC_IMAGE_STATE											
1	Enable	RhoDomain rate control parameters are present in MFX_AVC_IMAGE_STATE.											
12	Weighted_Pred_Flag <table><tr><td>Format:</td><td>Enable</td></tr></table> (This field is defined differently from Gen6, Gen7 follows strictly DXVA2 AVC interface.)	Format:	Enable										
Format:	Enable												

**MFX_AVC_IMG_STATE**

MFX_AVC_IMG_STATE																	
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>Disable [Default]</td><td>specifies that weighted prediction is not used for P and SP slices</td></tr><tr><td>1</td><td>Enable</td><td>specifies that weighted prediction is used for P and SP slices</td></tr></table>	Value	Name	Description	0	Disable [Default]	specifies that weighted prediction is not used for P and SP slices	1	Enable	specifies that weighted prediction is used for P and SP slices						
		Value	Name	Description													
		0	Disable [Default]	specifies that weighted prediction is not used for P and SP slices													
		1	Enable	specifies that weighted prediction is used for P and SP slices													
	Programming Notes																
	This field must set to '0' for B and I pictures.																
	11:10	Weighted_BiPred_Idc (This field is defined differently from DevSNB; DevIVB follows strictly DXVA2 AVC interface.)															
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>DEFAULT [Default]</td><td>Specifies that the default weighted prediction is used for B slices</td></tr><tr><td>1</td><td>EXPLICIT</td><td>Specifies that explicit weighted prediction is used for B slices</td></tr><tr><td>2</td><td>IMPLICIT</td><td>Specifies that implicit weighted prediction is used for B slices.</td></tr><tr><td>3</td><td>Reserved</td><td>Illegal value</td></tr></table>	Value	Name	Description	0	DEFAULT [Default]	Specifies that the default weighted prediction is used for B slices	1	EXPLICIT	Specifies that explicit weighted prediction is used for B slices	2	IMPLICIT	Specifies that implicit weighted prediction is used for B slices.	3	Reserved	Illegal value
		Value	Name	Description													
		0	DEFAULT [Default]	Specifies that the default weighted prediction is used for B slices													
1		EXPLICIT	Specifies that explicit weighted prediction is used for B slices														
2		IMPLICIT	Specifies that implicit weighted prediction is used for B slices.														
3		Reserved	Illegal value														
Programming Notes																	
This field must set to 0 for P and I pictures.																	
9:8	ImgStruct - Image Structure, img_structure[1:0] The current encoding picture structure can only takes on 3 possible values																
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>00b</td><td>Frame Picture</td></tr><tr><td>01b</td><td>Top Field Picture</td></tr><tr><td>11b</td><td>Bottom Field Picture</td></tr><tr><td>10b</td><td>Invalid, not allowed.</td></tr></table>	Value	Name	00b	Frame Picture	01b	Top Field Picture	11b	Bottom Field Picture	10b	Invalid, not allowed.						
	Value	Name															
	00b	Frame Picture															
	01b	Top Field Picture															
	11b	Bottom Field Picture															
	10b	Invalid, not allowed.															
	Programming Notes																
	img_structure[0] can be used as a flag to distinguish between frame and field structure. It must be consistent with the field_pic_flag setting in the Slice Header.This parameter is specified for Intel interface only, not present in the DXVA as a separate state (instead the img_structure[1] is embedded inside the DXVA picture definition).																
	7:0	Reserved															
Format:		MBZ															



MFX_AVC_IMG_STATE

4	31:16	MinFrameWSize									
		Default Value:		0h							
		Format:		U16							
		Minimum Frame Size [15:0] (in Word, 16-bit)(Encoder Only) Mininum Frame Size is specified to compensate for intel Rate Control Currently zero fill (no need to perform emulation byte insertion) is done only to the end of the CABAC_ZERO_WORD insertion (if any) at the last slice of a picture. Intel encoder parameter, not part of DXVA. The caller should always make sure that the value, represented by Mininum Frame Size, is always less than maximum frame size FrameBitRateMax (DWORD 10 bits 29:16) .This field is reserved in Decode mode. The programmable range 0...2^18-1 When MinFrameWSizeUnits is 00. Programmable range is 0...2^20-1 when MinFrameWSizeUnits is 01. Programmable range is 0...2^26-1 when MinFrameWSizeUnits is 10. Programmable range is 0...2^32-1 when MinFrameWSizeUnits is 11.									
	15	MbStatEnabled									
		Format:		Enable							
		Enable reading in MB status buffer (a.k.a. encoding stream-out buffer) Note: For multi-pass encoder, all passes except the first one need to set this value to 1. By setting the first pass to 0, it does save some memory bandwidth.									
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>Disable</td><td>Disable Reading of Macroblock Status Buffer</td></tr><tr><td>1</td><td>Enable</td><td>Enable Reading of Macroblock Status Buffer</td></tr></table>	Value	Name	Description	0	Disable	Disable Reading of Macroblock Status Buffer	1	Enable	Enable Reading of Macroblock Status Buffer
	Value	Name	Description								
	0	Disable	Disable Reading of Macroblock Status Buffer								
1	Enable	Enable Reading of Macroblock Status Buffer									
14	LoadSlicePointerFlag										
	Format:		Enable								
	LoadBitStreamPointerPerSlice (Encoder-only)To support multiple slice picture and additional header/data insertion before and after an encoded slice.When this field is set to 0, bitstream pointer is only loaded once for the first slice of a frame. For subsequent slices in the frame, bitstream data are stitched together to form a single output data stream.When this field is set to 1, bitstream pointer is loaded for each slice of a frame. Basically bitstream data for different slices of a frame will be written to different memory locations.										
	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>Disable</td><td>Load BitStream Pointer only once for the first slice of a frame</td></tr><tr><td>1</td><td>Enable</td><td>Load/reload BitStream Pointer only once for the each slice, reload the start location of the bitstream buffer from the Indirect PAK-BSE Object Data Start Address field</td></tr></table>	Value	Name	Description	0	Disable	Load BitStream Pointer only once for the first slice of a frame	1	Enable	Load/reload BitStream Pointer only once for the each slice, reload the start location of the bitstream buffer from the Indirect PAK-BSE Object Data Start Address field	
Value	Name	Description									
0	Disable	Load BitStream Pointer only once for the first slice of a frame									
1	Enable	Load/reload BitStream Pointer only once for the each slice, reload the start location of the bitstream buffer from the Indirect PAK-BSE Object Data Start Address field									
13	Reserved										
12	MvUnpackedFlag										
	MVUnPackedEnable (Encoder Only)This field is reserved in Decode mode.										
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr></table>	Value	Name	Description						
Value	Name	Description									

**MFx_AVC_IMG_STATE**

MFX_AVC_IMG_STATE					
		0	PACKED	use packed MV format (compliant to DXVA)	
		1	UNPACKED	use unpacked 8MV/32MV format only	
	11:10	ChromaFormatIdc Chroma Format IDC, ChromaFormatIdc[1:0]It specifies the sampling of chroma component (Cb, Cr) in the current picture as follows :			
		Value	Name	Description	
		00b	monochrome picture	Desc	
		01b	4:2:0 picture	Desc	
		10b	4:2:2 picture (not supported)		
		11b	4:4:4 picture (not supported)		
		Programming Notes			
		It is set to the value of the syntax element read from the current active SPS.The corresponding Monochrome Flag (monochrome_flag) can be derived from this field.			
		9	Reserved		
			Format:	MBZ	
	8	MbMvFormatFlag Use MB level MvFormat flag (Encoder Only)(This bit must be set to zero in IVB:GT2:A0)			
		Value	Name	Description	
		0	IGNORE	HW PAK ignore MvFormat in the MB data. When bit 12 == 0, all MBs use packed MV formatWhen bit 12 == 1, each MB data must use unpacked MV format, 8MV when there is no minor MV involved, and 32MV if there are some minor MVs.	
1		FOLLOW	HW PAK will follow MvFormat value set within each MB data.		
Programming Notes					
They must take one of the two values: the 8MV unpacked format (MvFormat =101b), and the 32MV unpacked format (MvFormat =110b).This bit can be set only when MvUnpackedFlag (bit 12 of this register) is set otherwise system could hang.					
7		EntropyCodingFlag Entropy Coding Flag, entropy_coding_flag			
		Value	Name	Description	
		0	CAVLC bit-serial encoding mode	Desc	
		1	CABAC bit-serial encoding mode.	Desc	
	Programming Notes				
	It specifies one of the two possible bit stream encoding modes in the AVC. It is set to the value of the syntax element read from the current active PPS.				



MFX_AVC_IMG_STATE

	6	ImgDisposableFlag		
		Current Img Disposable Flag or Non-Reference Picture Flag		
		Value	Name	Description
		0	REFERENCE	the current decoding picture may be used as a reference picture for others
	5	1	DISPOSABLE	the current decoding picture is not used as a reference picture (e.g. a B-picture cannot be a reference picture for any subsequent decoding)
		Programming Notes		
		It is derived from <code>ImgDisposableFlag = (nal_ref_idc == 0)</code> . <code>nal_ref_idc</code> is a syntax element from a NAL unit. When this flag is set, no reference picture and DMV are written out. This field is only valid for VLD decoding mode.		
	4	ConstrainedIPredFlag		
		Constrained Intra Prediction Flag, <code>constrained_ipred_flag</code> It is set to the value of the syntax element in the current active PPS.		
		Value	Name	Description
		0	INTRA_AND_INTER	allows both intra and inter neighboring MB to be used in the intra-prediction encoding of the current MB.
	3	1	INTRA_ONLY	allows only to use neighboring Intra MBs in the intra-prediction encoding of the current MB. If the neighbor is an inter MB, it is considered as not available.
		Direct8x8InffFlag		
		Direct 8x8 Inference Flag, <code>direct_8x8_inference_flag</code> It is set to the value of the syntax element in the current active SPS. It specifies the derivation process for luma motion vectors in the Direct MV coding modes (B_Skip, B_Direct_16x16 and B_Direct_8x8). When <code>frame_mbs_only_flag</code> is equal to 0, <code>direct_8x8_inference_flag</code> shall be equal to 1. It must be consistent with the <code>frame_mbs_only_flag</code> and <code>transform_8x8_mode_flag</code> settings.		
		Value	Name	Description
		0	SUBBLOCK	allows subpartitioning to go below 8x8 block size (i.e. 4x4, 8x4 or 4x8)
		1	BLOCK	allows processing only at 8x8 block size. MB Info is stored for 8x8 block size.
		Transform8x8Flag		
		8x8 IDCT Transform Mode Flag, <code>trans8x8_mode_flag</code> Specifies 8x8 IDCT transform may be used in this picture. It is set to the value of the syntax element in the current active PPS.		
		Value	Name	Description
		0	4x4	no 8x8 IDCT Transform, only 4x4 IDCT transform blocks are present
		1	8x8	8x8 Transform is allowed

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MFX_AVC_IMG_STATE				
	2	FrameMbOnlyFlag Frame MB only flag, frame_mbs_only_flagIt is set to the value of the syntax element in the current active SPS.		
		Value	Name	Description
		0	FALSE	not true ; effectively enables the possibility of MBAFF mode.
		1	TRUE	true, only frame MBs can occur in this sequence, hence disallows the MBAFF mode and field picture.
	1	MbaffFlameFlag MBAFF mode is active, mbaff_frame_flag.It is derived from MbaffFrameFlag = (mb_adaptive_frame_field_flag && ! field_pic_flag). mb_adaptive_frame_field_flag is a syntax element in the current active SPS and field_pic_flag is a syntax element in the current Slice Header. They both are present only if frame_mbs_only_flag is 0. Although mbaff_frame_flag is a Slice Header parameter, its value is expected to be the same for all the slices of a picture.It must be consistent with the mb_adaptive_frame_field_flag, the field_pic_flag and the frame_mbs_only_flag settings.This bit is valid only when the img_structure[1:0] indicates the current picture is a frame.		
		Value	Name	Description
		0	FALSE	not in MBAFF mode
		1	TRUE	in MBAFF mode
	0	FieldPicFlag Field picture flag, field_pic_flag, specifies the current slice is a coded field or not.It is set to the same value as the syntax element in the Slice Header. It must be consistent with the img_structure[1:0] and the frame_mbs_only_flag settings.Although field_pic_flag is a Slice Header parameter, its value is expected to be the same for all the slices of a picture.		
		Value	Name	Description
0h		FRAME	a slice of a coded frame	
1h		FIELD	a slice of a coded field	
5 [ExistsIf]Encode Only	31	Trellis Quantization Enabled (TQEnb)		
		Format: Enable		
		The TQ improves output video quality of AVC CABAC encoder by selecting quantized values for each non-zero coefficient so as to minimize the total R-D cost.This flag is only valid AVC CABAC mode. Otherwise, this flag should be disabled.		
		Value	Name	Description
	0h	Disable	Use Normal	
	1h	Enable	Use Trellis quantization	
30:28	Trellis Quantization Rounding (TQR) This rounding scheme is only applied to the quantized coefficients ranging from 0 to 1 when TQEnb is set to 1 in AVC CABAC mode. One of the following values is added to quantized coefficients before truncating fractional part.			



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Value	Name	Description
000b		Add 1/8
001b		Add 2/8
010b		Add 3/8
011b		Add 4/8 (rounding 0.5)
100b		Add 5/8
101b		Add 6/8
110b	Default	Add 7/8 (Default rounding 0.875)

27	Trellis Quantization Chroma Disable (TQChromaDisable) This signal is used to disable chroma TQ. To enable TQ for both luma and chroma, TQEnb=1, TQChromaDisable=0. To enable TQ only for luma, TQEnb=1, TQChromaDisable=1.	
	Value	Name
	0h	Enable Trellis Quantization chroma
	1h	Default Disable Trellis Quantization chroma

26:17	Reserved	
	Format:	MBZ

16	NonFirstPassFlag This signals the current pass is not the first pass. It will imply designate HW behavior: e.g	
	Value	Name
	0h	Disable Always use the MbQpY from initial PAK inline object for all passes of PAK
	1h	Enable Use MbQpY from stream-out buffer if MbRateCtrlFlag is set to 1

15:13	Reserved	
	Format:	MBZ

12	Reserved	
	Format:	MBZ

11:10	MinFrameWSizeUnits This field is the Minimum Frame Size Units	
	Value	Name
	00b	compatibility mode Minimum Frame Size is in old mode (words, 2bytes)
	01b	16 byte Minimum Frame Size is in 16bytes
	10b	4Kb Minimum Frame Size is in 4Kbytes
	11b	16Kb Minimum Frame Size is in 16Kbytes

9	MbRateCtrlFlag - MB level Rate Control Enabling Flag MB Rate Control conformance mask	

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MFX_AVC_IMG_STATE											
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable</td><td>Apply accumulative delta QP for consecutive passes on top of the macroblock QP values in inline data</td></tr><tr><td>1h</td><td>Enable</td><td>Apply RC QP delta to suggested QP values in Macroblock Status Buffer except the first pass.</td></tr></table>	Value	Name	Description	0h	Disable	Apply accumulative delta QP for consecutive passes on top of the macroblock QP values in inline data	1h	Enable	Apply RC QP delta to suggested QP values in Macroblock Status Buffer except the first pass.
		Value	Name	Description							
		0h	Disable	Apply accumulative delta QP for consecutive passes on top of the macroblock QP values in inline data							
		1h	Enable	Apply RC QP delta to suggested QP values in Macroblock Status Buffer except the first pass.							
		<table><tr><th colspan="3">Programming Notes</th></tr><tr><td colspan="3">This field is ignored when MacroblockStatEnable is disabled or MB level Rate control flag for the current MB is disable in Macroblock Status Buffer.</td></tr></table>	Programming Notes			This field is ignored when MacroblockStatEnable is disabled or MB level Rate control flag for the current MB is disable in Macroblock Status Buffer.					
	Programming Notes										
	This field is ignored when MacroblockStatEnable is disabled or MB level Rate control flag for the current MB is disable in Macroblock Status Buffer.										
	8	Reserved									
	Format:		MBZ								
	7	Intra/InterMblpcmFlag - ForceIPCMControlMask This field is to Force IPCM for Intra or Inter Macroblock size conformance mask.									
<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable</td><td>Do not change intra or Inter macroblocks even</td></tr><tr><td>1h</td><td>Enable</td><td>Change intra or Inter macroblocks MB_type to IPCM</td></tr></table>	Value	Name	Description	0h	Disable	Do not change intra or Inter macroblocks even	1h	Enable	Change intra or Inter macroblocks MB_type to IPCM		
Value	Name	Description									
0h	Disable	Do not change intra or Inter macroblocks even									
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<table><tr><th colspan="3">Programming Notes</th></tr><tr><td colspan="3">This field is ignored when MacroblockStatEnable is disabled or MB level Intra MB conformance flag for the current MB is disable in Macroblock Status Buffer.</td></tr></table>	Programming Notes			This field is ignored when MacroblockStatEnable is disabled or MB level Intra MB conformance flag for the current MB is disable in Macroblock Status Buffer.							
Programming Notes											
This field is ignored when MacroblockStatEnable is disabled or MB level Intra MB conformance flag for the current MB is disable in Macroblock Status Buffer.											
6:4	Reserved										
Format:		MBZ									
3	FrameSzUnderFlag - FrameBitRateMinReportMask This is a mask bit controlling if the condition of frame level bit count is less than FrameBitRateMin										
<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable</td><td>Do not update bit0 of MFC_IMAGE_STATUS control register.</td></tr><tr><td>1h</td><td>Enable</td><td>set bit0 and bit 1of MFC_IMAGE_STATUS control register if the total frame level bit counter is less than or equal to Frame Bit rate Minimum limit.</td></tr></table>	Value	Name	Description	0h	Disable	Do not update bit0 of MFC_IMAGE_STATUS control register.	1h	Enable	set bit0 and bit 1of MFC_IMAGE_STATUS control register if the total frame level bit counter is less than or equal to Frame Bit rate Minimum limit.		
Value	Name	Description									
0h	Disable	Do not update bit0 of MFC_IMAGE_STATUS control register.									
1h	Enable	set bit0 and bit 1of MFC_IMAGE_STATUS control register if the total frame level bit counter is less than or equal to Frame Bit rate Minimum limit.									
2	FrameSzOverFlag - FrameBitRateMaxReportMask This is a mask bit controlling if the condition of frame level bit count exceeds FrameBitRateMax.										
<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>Disable</td><td>Do not update bit0 of MFC_IMAGE_STATUS control register.</td></tr><tr><td>1</td><td>Enable</td><td>Set bit0 and bit 1 of MFC_IMAGE_STATUS control register if the total frame level bit counter is greater than or equal to Frame Bit rate Maximum limit.</td></tr></table>	Value	Name	Description	0	Disable	Do not update bit0 of MFC_IMAGE_STATUS control register.	1	Enable	Set bit0 and bit 1 of MFC_IMAGE_STATUS control register if the total frame level bit counter is greater than or equal to Frame Bit rate Maximum limit.		
Value	Name	Description									
0	Disable	Do not update bit0 of MFC_IMAGE_STATUS control register.									
1	Enable	Set bit0 and bit 1 of MFC_IMAGE_STATUS control register if the total frame level bit counter is greater than or equal to Frame Bit rate Maximum limit.									



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	1	InterMbMaxBitFlag - InterMBMaxSizeReportMask This is a mask bit controlling if the condition of any inter MB in the frame exceeds InterMBMaxSize.		
		Value	Name	Description
		0	Disable	Do not update bit0 of MFC_IMAGE_STATUS control register.
		1	Enable	Set bit0 of MFC_IMAGE_STATUS control register if the total bit counter for the current MB is greater than the Inter MB Conformance Max size limit.
	0	IntraMbMaxBitFlag - IntraMBMaxSizeReportMask This is a mask bit controlling if the condition of any intra MB in the frame exceeds IntraMBMaxSize.		
		Value	Name	Description
0h		Disable	Do not update bit0 of MFC_IMAGE_STATUS control register.	
1		Enable	set bit0 of MFC_IMAGE_STATUS control register if the total bit counter for the current MB is greater than the Intra MB Conformance Max size limit.	
6 [ExistsIf]Encode Only	31:28	Reserved		
	27:16	InterMbMaxSz		
		Format:	U12	
	This field, Inter MB Conformance Max size limit,indicates the allowed max bit count size for Inter MB			
	15:12	Reserved		
		Format:	MBZ	
	11:0	IntraMbMaxSz		
		Exists If:	//Intra Only	
		Format:	U12	
		This field, Intra MB Conformance Max size limit,indicates the allowed max bit count size for Intra MB		
All IPCM MBs should ignore this Max size limit.				
7 [ExistsIf]Encode Only	31:17	Reserved		
	16	Reserved		
	15:1	Reserved		
	0	VSL Top MB Trans8x8flag		
		Value	Name	Description
0		Disable [Default]	VSL will only fetch the current MB data.	



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		1	Enable	When this bit is set VSL will make extra fetch to memory to fetch the MB data for top MB.
8 [ExistsIf]Encode Only	31:24	SliceDeltaQpMax[3]		
		Format:		S7
		Range: [0:MAX_QP_DELTA]		
		This field is the Slice level delta QP for total bit-count above FrameBitRateMax - first 1/8 regionThis field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame exceeds FrameBitRateMax but is within 1/8 of FrameBitRateMaxDelta above FrameBitRateMax, i.e., in the range of (FrameBitRateMax, (FrameBitRateMax+ FrameBitRateMaxDelta»3).		
	23:16	SliceDeltaQpMax[2]		
		Format:		U8
		Range: [0:MAX_QP_DELTA]		
		This field is the Slice level delta QP for bit-count above FrameBitRateMax - above 1/8 and below 1/ 4 This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between 1/8 and ¼ of FrameBitRateMaxDelta above FrameBitRateMax, i.e., in the range of ((FrameBitRateMax+ FrameBitRateMaxDelta»3), (FrameBitRateMax+ FrameBitRateMaxDelta»2).		
	15:8	SliceDeltaQpMax[1]		
		Format:		S7
		Range: [0:MAX_QP_DELTA]		
		This field is the Slice level delta QP for bit-count above FrameBitRateMax - above1/ 4 and below 1/2 This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between ¼ and ½ of FrameBitRateMaxDelta above FrameBitRateMax, i.e., in the range of ((FrameBitRateMax+ FrameBitRateMaxDelta»2), (FrameBitRateMax+ FrameBitRateMaxDelta»1).		
	7:0	SliceDeltaQpPMax[0]		
		Format:		S7
		Range: [0:MAX_QP_DELTA]		
		This field is the Slice level delta QP for bit-count above FrameBitRateMax - above 1/ 2This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is above FrameBitRateMax by more than half the distance of FrameBitRateMaxDelta , i.e., in the range of ((FrameBitRateMax+ FrameBitRateMaxDelta»1), infinite).		



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9 [ExistsIf]Encode Only	31:24	SliceDeltaQpMin[3] <table><tr><td>Format:</td><td>S7</td></tr><tr><td colspan="2">Range: [0:MAX_QP_DELTA]</td></tr><tr><td colspan="2">This field is the Slice level delta QP for total bit-count below FrameBitRateMin - first 1/8 regionThis field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is less than FrameBitRateMin and greater than or equal to 1/8 the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»3), FrameBitRateMin).</td></tr></table>	Format:	S7	Range: [0:MAX_QP_DELTA]		This field is the Slice level delta QP for total bit-count below FrameBitRateMin - first 1/8 regionThis field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is less than FrameBitRateMin and greater than or equal to 1/8 the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»3), FrameBitRateMin).	
		Format:	S7					
		Range: [0:MAX_QP_DELTA]						
		This field is the Slice level delta QP for total bit-count below FrameBitRateMin - first 1/8 regionThis field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is less than FrameBitRateMin and greater than or equal to 1/8 the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»3), FrameBitRateMin).						
23:16	SliceDeltaQpMin[2] <table><tr><td>Format:</td><td>S7</td></tr><tr><td colspan="2">Range: [0:MAX_QP_DELTA]</td></tr><tr><td colspan="2">This field is the Slice level delta QP for bit-count below FrameBitRateMin - below 1/ 8 and above 1/ 4This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between one-eighth and quarter the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»2), (FrameBitRateMin- FrameBitRateMinDelta»3)).</td></tr></table>	Format:	S7	Range: [0:MAX_QP_DELTA]		This field is the Slice level delta QP for bit-count below FrameBitRateMin - below 1/ 8 and above 1/ 4This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between one-eighth and quarter the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»2), (FrameBitRateMin- FrameBitRateMinDelta»3)).		
	Format:	S7						
	Range: [0:MAX_QP_DELTA]							
	This field is the Slice level delta QP for bit-count below FrameBitRateMin - below 1/ 8 and above 1/ 4This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between one-eighth and quarter the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»2), (FrameBitRateMin- FrameBitRateMinDelta»3)).							
15:8	SliceDeltaQpMin[1] <table><tr><td>Format:</td><td>S7</td></tr><tr><td colspan="2">Range: [0:MAX_QP_DELTA]</td></tr><tr><td colspan="2">This field is the Slice level delta QP for bit-count below FrameBitRateMin- below 1/4 and above 1/ 2This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between quarter and half the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»1), (FrameBitRateMin- FrameBitRateMinDelta»2)).</td></tr></table>	Format:	S7	Range: [0:MAX_QP_DELTA]		This field is the Slice level delta QP for bit-count below FrameBitRateMin- below 1/4 and above 1/ 2This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between quarter and half the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»1), (FrameBitRateMin- FrameBitRateMinDelta»2)).		
	Format:	S7						
	Range: [0:MAX_QP_DELTA]							
	This field is the Slice level delta QP for bit-count below FrameBitRateMin- below 1/4 and above 1/ 2This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is between quarter and half the distance of FrameBitRateMinDelta from FrameBitRateMin, i.e., in the range of [(FrameBitRateMin- FrameBitRateMinDelta»1), (FrameBitRateMin- FrameBitRateMinDelta»2)).							
7:0	SliceDeltaQpMin[0] <table><tr><td>Format:</td><td>S7</td></tr><tr><td colspan="2">Range: [0:MAX_QP_DELTA]</td></tr><tr><td colspan="2">This field is the Slice Level Delta QP for bit-count below FrameBitRateMin - below 1/ 2This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is below FrameBitRateMin by more than half the distance of FrameBitRateMinDelta , i.e., in the range of [0, (FrameBitRateMin- FrameBitRateMinDelta»1).</td></tr></table>	Format:	S7	Range: [0:MAX_QP_DELTA]		This field is the Slice Level Delta QP for bit-count below FrameBitRateMin - below 1/ 2This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is below FrameBitRateMin by more than half the distance of FrameBitRateMinDelta , i.e., in the range of [0, (FrameBitRateMin- FrameBitRateMinDelta»1).		
	Format:	S7						
	Range: [0:MAX_QP_DELTA]							
	This field is the Slice Level Delta QP for bit-count below FrameBitRateMin - below 1/ 2This field is used to calculate the suggested slice QP into the MFC_IMAGE_STATUS control register when total bit count for the entire frame is below FrameBitRateMin by more than half the distance of FrameBitRateMinDelta , i.e., in the range of [0, (FrameBitRateMin- FrameBitRateMinDelta»1).							
10 [ExistsIf]Encode	31	FrameBitrateMaxUnit This field is the Frame Bitrate Maximum Limit Units.						

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Only		Value	Name	Description
		0	Byte	FrameBitRateMax is in units of 32 Bytes when FrameBitRateMaxUnitMode is 1 and in units of 128 Bytes if FrameBitRateMaxUnitMode is 0
		1	Kilo Byte	FrameBitRateMax is in units of 4KBytes Bytes when FrameBitRateMaxUnitMode is 1 and in units of 16KBytes if FrameBitRateMaxUnitMode is 0
	30	FrameBitRateMaxUnitMode This field is the Frame Bitrate Maximum Limit Units.		
		Value	Name	Description
		0h	compatibility mode	FrameBitRateMaxUnit is in old mode (128b/16Kb)
		1h	New mode	FrameBitRateMaxUnit is in new mode (32byte/4Kb)
	29:16	FrameBitRateMax This field is the Frame Bitrate Maximum Limit. This field along with FrameBitRateMaxUnit determines maximum allowed bits in a frame before multi-pass gets triggered (when enabled). In other words, multi-pass is triggered when the actual frame byte count exceeds this value. When FrameBitRateMaxUnitMode is 0(compatibility mode) bits 16:27 should be used, bits 28 and 29 should be 0..		
		Value	Name	Description
		0-512KB		The programmable range is 0-512KB when FrameBitRateMaxUnit is 0.
		0-8190KB		The programmable range is 0-8190KB when FrameBitRateMaxUnit is 1.
	15	FrameBitRateMinUnit This field is the Frame Bitrate Minimum Limit Units.		
		Value	Name	Description
		0	Byte	FrameBitRateMax is in units of 32 Bytes when FrameBitRateMinUnitMode is 1 and in units of 128 Bytes if FrameBitRateMinUnitMode is 0
		1	Kilo Byte	FrameBitRateMax is in units of 4KBytes Bytes when FrameBitRateMaxUnitMode is 1 and in units of 16KBytes if FrameBitRateMaxUnitMode is 0
	14	FrameBitRateMinUnitMode This field is the Frame Bitrate Minimum Limit Units.		
		Value	Name	Description
		0h	Compatibility mode	FrameBitRateMaxUnit is in old mode (128b/16Kb)
		1h	New mode	FrameBitRateMaxUnit is in new mode (32byte/4Kb)
	13:0	FrameBitRateMin RangeThe programmable range 0-512KB When FrameBitRateMinUnit is in 0.Programmable range is 0-8190 KB when FrameBitRateMinUnit is in 1.This field is the		



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		Frame Bitrate Minimum Limit ()This field along with FrameBitrateMinUnit determines minimum allowed bits in a Frame before Multi-Pass gets triggered (when enabled). In other words, multi-pass is triggered when the actual frame byte count is less than this value. When FrameBitrateMinUnitMode is 0 (compatibility mode) bits 0:11 should be used, bits 12 and 13 should be 0.		
11 [ExistsIf]Encode Only	31	Slice Stats Streamout Enable		
	30:16	FrameBitRateMaxDelta		
		Format: U15		
		This field is used to select the slice delta QP when FrameBitRateMax Is exceeded. It shares the same FrameBitrateMaxUnit. When FrameBitrateMaxUnitMode is 0(compatibility mode) bits 16:27 should be used, bits 28, 29 and 30 should be 0.		
		Value	Name	Description
		0-1024KB		The Programmable range 0-1024KB when FrameBitRateMaxUnit is 0.
	0-16380KB		The Programmable range is 0-16380KB when FrameBitRateMaxUnit is 1.	
	0h	[Default]		
	15	Reserved		
	Format: MBZ			
14:0	FrameBitRateMinDelta			
	Range: The programmable range 0-1024KB When FrameBitrateMinUnit is in 32Bytes. Programmable range is 0-16380KB when FrameBitrateMinUnit is in 4Kbytes. This field is used to select the slice delta QP when FrameBitRateMin Is exceeded. It shares the same FrameBitrateMinUnit. When FrameBitrateMinUnitMode is 0(compatibility mode) bits 0:11 should be used, bits 12, 13 and 14 should be 0.Note: HW requires the following condition FrameBitRateMinDelta <= 2*FrameBitRateMinMust be true, otherwise it may cause unpredicted behavior.			
12	31:21	Reserved		
		Format: MBZ		
	20	VMD Error Logic		
		Value	Name	Description
		0	Disable [Default]	
	1	Enable	Error Handling	
	19	Reserved		
	Format: MBZ			
	18	VAD Error Logic		
		Value	Name	Description
0	Enable	Error reporting ON in case of premature Slice done		



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13			[Default]	
		1	Disable	CABAC Engine will auto decode the bitstream in case of premature slice done.
	17	Reserved		
	16	Reserved		
	15:0	Reserved		
		Format:		MBZ
	31:30	Reserved		
		Format:		MBZ
	29	Current Picture Has Performed MMCO5 Set to 1 if the current Pic has performed the memory_management_control_operation = 5.		
	28:24	Number of Reference Frames		
		Format:		U5
		Range: Range 0 to MaxDpbSize (=16 for Level 4.1)		
		Specifies the maximum number of reference frames (frames, field pairs, unpaired field) existed in the current DBP for decoding the current picture.		
	23:22	Reserved		
		Format:		MBZ
	21:16	Number of Active Reference Pictures from L1		
		Format:		U6-1
		Specifies the initial maximum reference index value minus 1 to access the L1 Reference List. It is extracted from PPS. It corresponds to the number of active reference pictures from L1 to decode the current picture. It can be modified by the slice header if num_ref_idx_active_override_flag is set. Only valid for B picture.		
		Value		Name
	[0,31]			
15:14	Reserved			
	Format:		MBZ	
13:8	Number of Active Reference Pictures from L0			
	Format:		U6-1	
	Specifies the initial maximum reference index value minus 1 to access the L0 Reference List. It is extracted from PPS. It corresponds to the number of active reference pictures from L0 to decode the current picture. It can be modified by the slice header if num_ref_idx_active_override_flag is set. Valid for both P and B pictures.			
	Value		Name	
	[0,31]			



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	7:0	Initial QP Value <table><tr><td>Format:</td><td>S7</td></tr></table> Range: [-26,25] Initial QP value for a Slice, extracted from PPS. It may further get modified by slice_qp_delta in slice header and mb_qp_delta in MB header.	Format:	S7	
	Format:	S7			
	14 [ExistsIf] Short Format only	31:24	Log2_max_pic_order_cnt_lsb_minus4 <table><tr><td>Exists If:</td><td>//Short Format Only</td></tr></table> It is a SPS syntax element, used to determine how many bits in the bitstream are used to represent pic_order_cnt_lsb syntax element in the slice header.Unsigned	Exists If:	//Short Format Only
		Exists If:	//Short Format Only		
23:16		Log2_max_frame_num_minus4 <table><tr><td>Exists If:</td><td>//Short Format Only</td></tr></table> It is a SPS syntax element, used to determine how many bits in the bitstream are used to represent frame_num syntax element in the slice header.Unsigned.	Exists If:	//Short Format Only	
Exists If:		//Short Format Only			
15		deblocking_filter_control_present_flag <table><tr><td>Exists If:</td><td>//Short Format Only</td></tr></table> It is a PPS syntax element, indicates if more deblocking filter control syntax elements are present in the slice header.	Exists If:	//Short Format Only	
Exists If:		//Short Format Only			
14:12	num_slice_groups_minus1 <table><tr><td>Exists If:</td><td>//Short Format Only</td></tr></table> BitField It is a PPS syntax element.Use for Slice Header parsing only, to read in slice_group_change_cycle, if any, but is not used by H/W, i.e. no slice group support.Desc	Exists If:	//Short Format Only		
Exists If:	//Short Format Only				
11	redundant_pic_cnt_present_flag <table><tr><td>Exists If:</td><td>//Short Format Only</td></tr></table> It is a PPS syntax element.Use for Slice Header parsing only, to read-in redundant_pic_cnt, if any, but is not used by H/W, i.e. no support for redundant slice processing.	Exists If:	//Short Format Only		
Exists If:	//Short Format Only				
10:8	slice_group_map_type <table><tr><td>Exists If:</td><td>//Short Format Only</td></tr></table> It is a PPS syntax element.Use for Slice Header parsing only, to read in slice_group_change_cycle, if any, but is not used by H/W, i.e. no slice group support.	Exists If:	//Short Format Only		
Exists If:	//Short Format Only				
	7:4	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ	
Format:	MBZ				



MFX_AVC_IMG_STATE											
		IDR flag is decoded from NAL Header Byte									
	3:2	Pic_order_cnt_type <table><tr><td>Exists If:</td><td colspan="2">//Short Format Only</td></tr></table> It is a SPS syntax element.Use for Slice Header parsing only.			Exists If:	//Short Format Only					
	Exists If:	//Short Format Only									
	1	Delta_pic_order_always_zero_flag <table><tr><td>Exists If:</td><td colspan="2">//Short Format Only</td></tr></table> It is a SPS syntax element.Use for Slice Header parsing only.			Exists If:	//Short Format Only					
Exists If:	//Short Format Only										
0	Pic_order_present_flag <table><tr><td>Exists If:</td><td colspan="2">//Short Format Only</td></tr></table> It is a PPS syntax element.Use for Slice Header parsing only.			Exists If:	//Short Format Only						
Exists If:	//Short Format Only										
15 [ExistsIf] Short Format only	31:16	Curr Pic Frame Num <table><tr><td>Exists If:</td><td colspan="2">//Short Format Only</td></tr><tr><td>Format:</td><td colspan="2">U16</td></tr></table> Derived from Slice Header syntax element			Exists If:	//Short Format Only		Format:	U16		
	Exists If:	//Short Format Only									
Format:	U16										
	15:0	Slice Group Change Rate <table><tr><td>Exists If:</td><td colspan="2">//Short Format Only</td></tr><tr><td>Format:</td><td colspan="2">U16-1</td></tr></table> It is a PPS syntax element Use for Slice Header parsing only, to read in slice_group_change_cycle, if any, but is not used by H/W, i.e. no slice group support.			Exists If:	//Short Format Only		Format:	U16-1		
Exists If:	//Short Format Only										
Format:	U16-1										
16 [ExistsIf]: Short Format only	31	Inter View Order Disable <table><tr><td>Exists If:</td><td colspan="2">//Short Format Only</td></tr></table> It indicates how to append inter-view picture into initial sorted reference list. (due to ambiguity in the MVC Spec)			Exists If:	//Short Format Only					
		Exists If:	//Short Format Only								
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Default [Default]</td><td>View Order Ascending</td></tr><tr><td>1h</td><td>Disable</td><td>View ID Ascending</td></tr></table>	Value	Name	Description	0h	Default [Default]	View Order Ascending	1h	Disable	View ID Ascending
		Value	Name	Description							
	0h	Default [Default]	View Order Ascending								
1h	Disable	View ID Ascending									
30:22	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>		Format:	MBZ							
Format:	MBZ										
21:18	Max View IDX L1 <table><tr><td>Exists If:</td><td>//Short Format Only</td></tr></table> It is a PPS syntax element corresponding to Anchor/Non-Anchor Reference List L1 It indicates the maximum number of inter-view picture for Reference List L1		Exists If:	//Short Format Only							
Exists If:	//Short Format Only										



MFX_AVC_IMG_STATE										
	17:16	Reserved								
		Format:	MBZ							
	15:12	Max View IDXLO								
		Exists If:	//Short Format Only							
		Reference ListL0								
		It indicates the maximum number of inter-view picture for Reference List L0								
	11:10	Reserved								
		Format:	MBZ							
	9:0	Current Frame View ID								
		Exists If:	//Short Format Only							
		It indicates the View ID of the current decoding frame								
17	31:22	Reserved								
		Format:	MBZ							
	21:16	RhoDomain AverageMacroblockQP								
		Exists If:	//[RhoDomain Rate Control] == 1							
		Format:	U6							
	15:9	Reserved								
		Format:	MBZ							
	8	Extended RhoDomain Statistics Enable								
		This parameter enables PAK to generate RhoDomain statistics from marcoblock QP and fractional QP computation.								
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>Disable</td><td>RhoDomain statistics generated from Frame Qp and no fractional QP computation.</td></tr><tr><td>1</td><td>Enable</td><td>Enable MB QP based RhoDomain statistics and fractional QP computation.</td></tr></table>	Value	Name	Description	0	Disable	RhoDomain statistics generated from Frame Qp and no fractional QP computation.	1	Enable
Value	Name	Description								
0	Disable	RhoDomain statistics generated from Frame Qp and no fractional QP computation.								
1	Enable	Enable MB QP based RhoDomain statistics and fractional QP computation.								
7:6	Reserved									
	Format:	MBZ								
5:3	Fractional QP offset									
	Format:	U3								
	Start position from the top of the Frame where increased Quantization parameter is added.									
2:0	Fractional QP input									
	In a set of 8 rows, Qp is incremented by 1 for F_qp rows.									
18	31:0	Reserved								
		Format:	MBZ							



MFX_AVC_IMG_STATE		
19	31:0	Threshold Size in Bytes
		<table><tr><td>Format:</td><td>U32</td></tr></table> When a slice exceeds this value in bytes, hardware will end current slice as soon as possible and insert a new slice boundary. Note there is no guarantee that the actual slice size will meet this value, it is a hint to the HW to end the slice as soon as possible (which could be 2-5 macroblocks in the future from this detection point).
Format:	U32	
20	31:0	Target Slice Size in Bytes
		<table><tr><td>Format:</td><td>U32</td></tr></table>
Format:	U32	



MFX_AVC_SLICE_STATE

MFX_AVC_SLICE_STATE			
Source:		VideoCS	
Length Bias:		2	
Description			
This is a slice level command and can be issued multiple times within a picture that is comprised of multiple slices. The same command is used for AVC encoder (PAK mode) and decoder (VLD and IT modes).			
Programming Notes			
MFX_AVC_SLICE_STATE command is not issued for AVC DXVA2 Short Format Bitstream decode, instead MFD_AVC_SLICEADDR command is executed to retrieve the next slice MB Start Address X and Y by H/W itself.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	Pipeline	
		Default Value:	2h MFX_AVC_SLICE_STATE
		Format:	OpCode
	26:24	Command Opcode	
		Default Value:	1h AVC
		Format:	OpCode
	23:21	SubOpcodeA	
		Default Value:	0h MFX_AVC_SLICE_STATE
		Format:	OpCode
	20:16	Command SubOpcodeB	
		Default Value:	3h MFX_AVC_SLICE_STATE
		Format:	OpCode
15:12	Reserved		
	Format:	MBZ	
11:0	DWord Length		
	Default Value:	8h DWORD_COUNT_n	
	Format:	=n	
	Excludes DWords 0,1		
1	31:4	Reserved	
		Format:	MBZ
	3:0	Slice Type It is set to the value of the syntax element read from the Slice Header.	

**MFx_AVC_SLICE_STATE**

		Value	Name
		0000b	P Slice
		0001b	B Slice
		0010b	I Slice
		0011b-1111b	Reserved
		Programming Notes	
		Bits[3:2] must be 0	
2	31:30	Reserved	
		Format:	MBZ
	29:24	Number of Reference Pictures in Inter-prediction List 1	
		Format:	U6
		This field is valid only for encoding a B Slice, for which it is expected to have at least one entry in the reference list L1; otherwise (if Slice Type is not a B Slice), this field must be set to 0. This field can be derived for a B Slice from the Slice Header syntax element NumRefIdxActiveMinus1 as, Num_Ref_Idx_L1 = NumRefIdxActiveMinus1[1] + 1.	
		Value	Name
		0-32	
	23:22	Reserved	
		Format:	MBZ
	21:16	Number of Reference Pictures in Inter-prediction List 0	
		Format:	U6
		This field is valid for encoding a P or B Slice, for which it is expected to have at least one entry in the reference list L0; otherwise (if Slice Type is not a P or B Slice), this field must be set to 0. This field can be derived for a P or B Slice from the Slice Header syntax element NumRefIdxActiveMinus1 as, Num_Ref_Idx_L0 = NumRefIdxActiveMinus1[0] + 1.	
		Value	Name
		0-32	
	15:11	Reserved	
		Format:	MBZ
	10:8	Log 2 Weight Denom Chroma	
		Format:	U3
		Value	Name
		0-7	
	7:3	Reserved	
		Format:	MBZ



MFX_AVC_SLICE_STATE			
3	2:0	Log 2 Weight Denom Luma	
		Format:	U3
		It is the base 2 logarithm of the denominator for all Luma weighting factors. It is set to the value of the syntax element read from the Slice Header Pred_Weight_Table().	
		Value	Name
		0-7	
3	31:30	Weighted Prediction Indicator	
		This field indicates the Weighted Prediction mode for a P or B Slice. It is a combined field corresponding to the syntax element WeightedBiPredIdc or WeightedPredFlag read from the current active PPS.	
		If it is a B-Slice, these bits are interpreted as:	
		00b - Specifies the default weighted inter-prediction to be applied	
		01b - Specifies the explicit weighted inter-prediction to be applied	
		10b - Specifies the implicit weighted inter-prediction to be applied	
		11b - Reserved (not allowed)	
		If it is a P Slice, these bits are interpreted as:	
		00b - Disables weighted inter-prediction (Default weighted)	
		01b - Enables weighted inter-prediction (Explicit weighted)	
		10b - 11b - Reserved	
		Programming Notes	
		Only when in B Slice with Weighted_Pred_Idc = 1 (explicit weighted prediction), will there be a L1 and/or a L0 weight+offset tables being sent to the BSD unit through the Slice_State command.	
		Only when in P Slice with Weighted_Pred_Idc = 1, will there be a L0 weight+offset table being sent to the BSD.	
		If Weighted_Pred_Idc != 1 for B Slice or Weighted_Pred_Idc = 0 for P Slice, no Slice_State command should be issued to send these tables. If still being issued, the data is read but ignored.	
		DXVA specifies Weighted_Bipred and Weighted_Pred in frame-level state. However, these two flags are combined and specified in slice level for both P and B slice type.	
	29	Direct Prediction Type	
		Type of direct prediction used for B Slices. This field is valid only for Slice_Type = B Slice; otherwise, it must be set to 0.	
		Value	Name
		0	Temporal
		1	Spatial
	28:27	Disable Deblocking Filter Indicator	
		Value	Name
		00b	FilterInternalEdgesFlag is set equal to 1

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		01b	Disable all deblocking operation, no deblocking parameter syntax element is read; filterInternalEdgesFlag is set equal to 0	
		10b	Macroblocks in different slices are considered not available; filterInternalEdgesFlag is set equal to 1	
		11b	Reserved Not defined in AVC	
	26	Reserved		
		Format:		MBZ
	25:24	Cabac Init Idc[1:0] Specifies the index for determining the initialization table used in the context variable initialization process.		
		Value		Name
		0-2		
		Programming Notes		
		Cabac initialization is also dependent on the field/frame picture type, Slice type, and the current SliceQP value.		
	23:22	Reserved		
		Format:		MBZ
	21:16	Slice Quantization Parameter Quantization Parameter for current slice. Derived from PPS and slice_delta_qp syntax element in Slice Header. It is needed for CABAC context initialization and deblocking filter control. And it is also used as the starting QP value in the very first MB of a slice. It is in the range of unsigned integer 0 to 51, for 8-bit pixel bit-depth.		
	15:12	Reserved		
	Format:		MBZ	
11:8	Slice Beta Offset Div2			
	Format:		S3 2's Complement	
	Range: [-6, 6] Inclusive			
	Specifies the offset used in accessing the deblocking filter strength tables.			
7:4	Reserved			
	Format:		MBZ	
3:0	Slice Alpha C0 Offset Div2			
	Format:		S3 2's Complement	
	Range: [-6, 6] Inclusive			
	Specifies the offset used in accessing the deblocking filter strength tables.			



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4	31:24	Slice Vertical Position This field specifies the position in y-direction of the first macroblock in the Slice in unit of macroblocks. The fields (Slice_MB_Start_Hor_Pos, Slice_MB_Start_Vert_Pos) are valid in VLD (decoding) mode only. They are ignored by hardware in decoding IT mode and encoding mode (whereas the position is provided by the per-macroblock object command). Derived Programming Notes Error Handling: Driver needs to check if FirstMbY starts at 0 on the first slice of frame. If not, driver needs to add a phantom slice with FirstMbX and FirstMbY set to 0.
	23:16	Slice Horizontal Position This field specifies the position in x-direction of the first macroblock in the Slice in unit of macroblocks. Derived Programming Notes Error Handling: Driver needs to check if FirstMbY starts at 0 on the first slice of frame. If not, driver needs to add a phantom slice with FirstMbX and FirstMbY set to 0.
	15	Reserved Format: MBZ
	14:0	Slice Start Mb Num Exists If: //Decoder Only The MB number (linear MB address in a picture) at the start of a Slice, it must match with the Slice Horizontal Position (Slice_MB_Start_Hor_Pos) and Vertical Position (Slice_MB_Start_Vert_Pos) in the picture. Programming Notes In creating the Phantom Slice for error concealment, this field should set to the total number of MB in the current picture + 1.
5	31:24	Reserved Format: MBZ
	23:16	Next Slice Vertical Position This field specifies the position in y-direction of the first macroblock in the next Slice in unit of macroblocks. This field is primarily used for error concealment. In the case that current slice is the last slice, this field should set to the height of picture (since y-direction is zero-based numbering).
	15:8	Reserved Format: MBZ
	7:0	Next Slice Horizontal Position This field specifies the position in x-direction of the first macroblock in the next Slice in unit of macroblocks. This field is primarily used for error concealment. In the case that current slice is the last slice,

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		this field should set to 0.																
6 Encoder Only	31	Rate Control Counter Enable To enable the accumulation of bit allocation for rate control This field enables hardware Rate Control logic. The rest of the RC control fields are only valid when this field is set to 1. Otherwise, hardware ignores these fields. <table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table>	Value	Name	0	Disable	1	Enable										
		Value	Name															
		0	Disable															
		1	Enable															
	30	ResetRateControlCounter To reset the bit allocation accumulation counter to 0 to restart the rate control. <table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>Not Reset</td></tr><tr><td>1</td><td>Reset</td></tr></table>	Value	Name	0	Not Reset	1	Reset										
		Value	Name															
		0	Not Reset															
	1	Reset																
	29:28	RC Triggler Mode <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>00b</td><td>Always Rate Control</td><td>Whereas RC becomes active if sum_act > sum_target or sum_act < sum_target</td></tr><tr><td>01b</td><td>Gentle Rate Control</td><td>whereas RC becomes active if sum_act > upper_midpt or sum_act < lower_midpt</td></tr><tr><td>10b</td><td>Loose Rate Control</td><td>whereas RC becomes active if sum_act > sum_max or sum_act < sum_min</td></tr><tr><td>11b</td><td>Reserved</td><td></td></tr></table>		Value	Name	Description	00b	Always Rate Control	Whereas RC becomes active if sum_act > sum_target or sum_act < sum_target	01b	Gentle Rate Control	whereas RC becomes active if sum_act > upper_midpt or sum_act < lower_midpt	10b	Loose Rate Control	whereas RC becomes active if sum_act > sum_max or sum_act < sum_min	11b	Reserved	
		Value	Name	Description														
00b		Always Rate Control	Whereas RC becomes active if sum_act > sum_target or sum_act < sum_target															
01b		Gentle Rate Control	whereas RC becomes active if sum_act > upper_midpt or sum_act < lower_midpt															
10b		Loose Rate Control	whereas RC becomes active if sum_act > sum_max or sum_act < sum_min															
11b	Reserved																	
27:24	RC Stable Tolerance <table><tr><td>Format:</td><td>U4</td></tr><tr><td colspan="2">This field specifies the tolerance required to deactivate RC once it has been triggered.</td></tr><tr><th>Value</th><th>Name</th></tr><tr><td>0-15</td><td></td></tr></table>		Format:	U4	This field specifies the tolerance required to deactivate RC once it has been triggered.		Value	Name	0-15									
	Format:	U4																
	This field specifies the tolerance required to deactivate RC once it has been triggered.																	
Value	Name																	
0-15																		
23	RC Panic Enable If this field is set to 1, RC enters panic mode when sum_act > sum_max. RC Panic Type field controls what type of panic behavior is invoked. <table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table>		Value	Name	0	Disable	1	Enable										
	Value	Name																
	0	Disable																
	1	Enable																
22	RC Panic Type This field selects between two RC Panic methods <table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>QP Panic</td></tr><tr><td>1</td><td>CBP Panic</td></tr></table>		Value	Name	0	QP Panic	1	CBP Panic										
	Value	Name																
	0	QP Panic																
1	CBP Panic																	



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		Programming Notes If it is set to 0, in panic mode, the macroblock QP is maxed out, setting to requested QP + QP_max_pos_mod. If it is set to 1, for an intra macroblock, AC CBPs are set to zero (note that DC CBPs are not modified). For inter macroblocks, AC and DC CBPs are forced to zero.														
21	MB Type Direct Conversion Disable Exists If: //B-Slice For all Macroblock type conversions in different slices, refer to Section "Macroblock Type Conversion Rules" in the same volume. <table><tr><th>Value</th><th colspan="3">Name</th></tr><tr><td>0</td><td colspan="3">Enable direct mode conversion</td></tr><tr><td>1</td><td colspan="3">Disable direct mode conversion</td></tr></table> Programming Notes This field is zero for all other slices other than B-Slice.				Value	Name			0	Enable direct mode conversion			1	Disable direct mode conversion		
Value	Name															
0	Enable direct mode conversion															
1	Disable direct mode conversion															
20	MB Type Skip Conversion Disable Exists If: //P-Slice or B-Slice For all Macroblock type conversions in different slices, refer to Section "Macroblock Type Conversion Rules" in the same volume. <table><tr><th>Value</th><th colspan="3">Name</th></tr><tr><td>0</td><td colspan="3">Enable skip type conversion</td></tr><tr><td>1</td><td colspan="3">Disable skip type conversion</td></tr></table> Programming Notes This field is zero for all other slices other than P_Slice or B-Slice. \				Value	Name			0	Enable skip type conversion			1	Disable skip type conversion		
Value	Name															
0	Enable skip type conversion															
1	Disable skip type conversion															
19	Is Last Slice It is used by the zero filling in the Minimum Frame Size test. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>1</td><td></td><td>Current slice is the last slice of a picture</td></tr><tr><td>0</td><td></td><td>Current slice is NOT the last slice of a picture</td></tr></table>				Value	Name	Description	1		Current slice is the last slice of a picture	0		Current slice is NOT the last slice of a picture			
Value	Name	Description														
1		Current slice is the last slice of a picture														
0		Current slice is NOT the last slice of a picture														
18	Reserved															
17	Header Insertion Present in Bitstream <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td></td><td>No header insertion into the output bitstream buffer, in front of the current slice encoded bits.</td></tr><tr><td>1</td><td></td><td>Header insertion into the output bitstream buffer is present, and is in front of</td></tr></table>				Value	Name	Description	0		No header insertion into the output bitstream buffer, in front of the current slice encoded bits.	1		Header insertion into the output bitstream buffer is present, and is in front of			
Value	Name	Description														
0		No header insertion into the output bitstream buffer, in front of the current slice encoded bits.														
1		Header insertion into the output bitstream buffer is present, and is in front of														



MFX_AVC_SLICE_STATE			
7			the current slice encoded bits.
	16	SliceData Insertion Present in Bitstream	
		Value	Name Description
		0	No Slice Data insertion into the output bitstream buffer
		1	Slice Data insertion into the output bitstream buffer is present.
	15	Tail Insertion Present in bitstream	
		Value	Name Description
		0	No tail insertion into the output bitstream buffer, after the current slice encoded bits
		1	Tail insertion into the output bitstream buffer is present, and is after the current slice encoded bits.
	14	Reserved	
		Format:	MBZ
	13	EmulationByteSliceInsertEnable	
		To have PAK outputting SODB or EBSP to the output bitstream buffer	
		Value	Name Description
		0	outputting RBSP
		1	outputting EBSP
	12	CabacZeroWordInsertionEnable	
		To pad the end of a SliceLayer RBSP to meet the encoded size requirement.	
		Value	Name Description
		0	No Cabac_Zero_Word Insertion
		1	Allow internal Cabac_Zero_Word generation and append to the end of RBSP (effectively can be used as an indicator for last slice of a picture, if the assumption is only the last slice of a picture needs to insert CABAC_ZERO_WORDS.
	11:8	Reserved	
		Format:	MBZ
	7:4	Slice ID [3:0]	
		To identify the output data (coding information record) returned for rate control from PAK to ENC and VPP.	
	3:2	Reserved	
		Format:	MBZ
	1:0	Stream ID [1:0]	
		To identify the output data (coding information record) returned for rate control from PAK to ENC and VPP.	
7	31:29	Reserved	



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Encoder Only		Format:	MBZ	
	28:0	Indirect PAK-BSE Data Start Address (Write)		
		Exists If:	//AVC Encode Mode	
		This field specifies the memory starting address (offset) to write out the compressed bitstream data from the BSE processing. This pointer is relative to the MFC Indirect PAK-BSE Object Base Address. It is a byte-aligned address for the AVC bitstream data in both CABAC/CAVLC Modes. For Write, there is no need to have a data length field. It is assumed the global memory bound check specified in the IND_OBJ_BASE_ADDRESS command (Indirect PAK-BSE Object Access Upper Bound) will take care of any illegal write access.		
		Value	Name	
	0 - 512MB			
8 Encoder Only	31:24	Magnitude of QP Max Negative Modifier		
		Format:	U8	
		This field specifies the lower limit of the QP modifier.		
		Value	Name	
		0-51		
	23:16	Magnitude of QP Max Positive Modifier		
		Format:	U8	
		This field specifies the upper limit of the QP modifier.		
		Value	Name	
		0 - 15		
	15:12	Shrink Param - Shrink Resistance		
		Format:	U4	
		This field specifies the additional points added each time decreased correction is invoked.		
		Value	Name	
		0 - 15		
	11:8	Shrink Param - Shrink Init		
		Format:	U4	
		This field specifies the initial points required to trip decreased control.		
		Value	Name	
		0 - 15		
	7:4	Grow Param - Grow Resistance		
		Format:	U4	
		This field specifies the additional points added each time increased correction is invoked.		
		Value	Name	
		0 - 15		

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9 Encoder Only	3:0	Grow Param - Grow Init	
		Format:	U4
		This field specifies the initial points required to trip increased control.	
		Value	Name
		0 - 15	
	31	RoundInterEnable	
		Format:	Enable
		When this bit is not set, RoundInter defaults to 2 to match SNB.	
	30:28	RoundInter	
		Format:	U3
		Rounding precision for Inter quantized coefficients	
		Value	Name
		000b	+1/16 [Default]
		001b	+2/16
		010b	+3/16
		011b	+4/16
		100b	+5/16
		101b	+6/16
		110b	+7/16
		111b	+8/16
	27	RoundIntraEnable	
		Format:	Enable
		When this bit is not set, RoundIntra defaults to 4 to match SNB.	
	26:24	RoundIntra	
		Format:	U3
		Rounding precision for Intra quantized coefficients	
		Value	Name
		000b	+1/16 [Default]
		001b	+2/16
		010b	+3/16
		011b	+4/16
		100b	+5/16
		101b	+6/16
		110b	+7/16
		111b	+8/16
	23:20	Correct 6	



MFX_AVC_SLICE_STATE												
		<table><tr><td>Format:</td><td>U4</td></tr><tr><td colspan="2">This field specifies the points used in the lowermost RC region when sum_act <= sum_min.</td></tr><tr><td>Value</td><td>Name</td></tr><tr><td>0 - 15</td><td></td></tr></table>	Format:	U4	This field specifies the points used in the lowermost RC region when sum_act <= sum_min.		Value	Name	0 - 15			
	Format:	U4										
	This field specifies the points used in the lowermost RC region when sum_act <= sum_min.											
	Value	Name										
	0 - 15											
	19:16	<table><tr><td colspan="2">Correct 5</td></tr><tr><td>Format:</td><td>U4</td></tr><tr><td colspan="2">This field specifies the points used in the fifth RC region when sum_act > sum_min but <= lower_midpt.</td></tr><tr><td>Value</td><td>Name</td></tr><tr><td>0 - 15</td><td></td></tr></table>	Correct 5		Format:	U4	This field specifies the points used in the fifth RC region when sum_act > sum_min but <= lower_midpt.		Value	Name	0 - 15	
	Correct 5											
	Format:	U4										
	This field specifies the points used in the fifth RC region when sum_act > sum_min but <= lower_midpt.											
	Value	Name										
	0 - 15											
	15:12	<table><tr><td colspan="2">Correct 4</td></tr><tr><td>Format:</td><td>U4</td></tr><tr><td colspan="2">This field specifies the points used in the fourth RC region when sum_act > lower_midpt but <= sum_target.</td></tr><tr><td>Value</td><td>Name</td></tr><tr><td>0 - 15</td><td></td></tr></table>	Correct 4		Format:	U4	This field specifies the points used in the fourth RC region when sum_act > lower_midpt but <= sum_target.		Value	Name	0 - 15	
	Correct 4											
	Format:	U4										
	This field specifies the points used in the fourth RC region when sum_act > lower_midpt but <= sum_target.											
	Value	Name										
	0 - 15											
	11:8	<table><tr><td colspan="2">Correct 3</td></tr><tr><td>Format:</td><td>U4</td></tr><tr><td colspan="2">This field specifies the points used in the third RC region when sum_act > sum_target but <= upper_midpt.</td></tr><tr><td>Value</td><td>Name</td></tr><tr><td>0 - 15</td><td></td></tr></table>	Correct 3		Format:	U4	This field specifies the points used in the third RC region when sum_act > sum_target but <= upper_midpt.		Value	Name	0 - 15	
	Correct 3											
	Format:	U4										
This field specifies the points used in the third RC region when sum_act > sum_target but <= upper_midpt.												
Value	Name											
0 - 15												
7:4	<table><tr><td colspan="2">Correct 2</td></tr><tr><td>Format:</td><td>U4</td></tr><tr><td colspan="2">This field specifies the points used in the second RC region when sum_act > upper_midpt but <= sum_max.</td></tr><tr><td>Value</td><td>Name</td></tr><tr><td>0 - 15</td><td></td></tr></table>	Correct 2		Format:	U4	This field specifies the points used in the second RC region when sum_act > upper_midpt but <= sum_max.		Value	Name	0 - 15		
Correct 2												
Format:	U4											
This field specifies the points used in the second RC region when sum_act > upper_midpt but <= sum_max.												
Value	Name											
0 - 15												
3:0	<table><tr><td colspan="2">Correct 1</td></tr><tr><td>Format:</td><td>U4</td></tr><tr><td colspan="2">This field specifies the points used in the topmost RC region when sum_act > sum_max.</td></tr><tr><td>Value</td><td>Name</td></tr><tr><td>0 - 15</td><td></td></tr></table>	Correct 1		Format:	U4	This field specifies the points used in the topmost RC region when sum_act > sum_max.		Value	Name	0 - 15		
Correct 1												
Format:	U4											
This field specifies the points used in the topmost RC region when sum_act > sum_max.												
Value	Name											
0 - 15												
10 Encoder Only	31:28	ClampValues - CV7										
	27:24	CV6										
	23:20	CV5										
	19:16	CV4										

**MFX_AVC_SLICE_STATE**

15:12	CV3							
11:8	CV2							
7:4	CV1							
3:0	CV0 - Clamp Value 0							
	Format:	U4						
	If the magnitude of coefficients at locations assigned with CV0 (mapping shown below) exceeds $2^{CV0}-1$, they are replaced with $2^{CV0}-1$. For coefficients at locations marked as 'none', no clamping is performed. The following mappings are only applied to luma and chroma blocks\subblocks containing AC coefficients (blocks\subblocks with only DC coeffs will not be clamped).							
	For 4x4 frame block, each coefficient is mapped to one of the eight CV values as following:							
	none	CV7	CV5	CV4				
	CV7	CV6	CV4	CV3				
	CV5	CV4	CV2	CV1				
	CV4	CV3	CV1	CV0				
	For 8x8 frame block, each coefficient is mapped to one of the eight CV values as following:							
	none	none	CV7	CV6	CV5	CV4	CV3	CV3
	none	CV7	CV6	CV5	CV4	CV3	CV3	CV2
	CV7	CV6	CV5	CV4	CV3	CV3	CV2	CV2
	CV6	CV5	CV4	CV3	CV3	CV2	CV2	CV1
	CV5	CV4	CV3	CV3	CV2	CV2	CV1	CV1
	CV4	CV3	CV3	CV2	CV2	CV1	CV1	CV0
	CV3	CV3	CV2	CV2	CV1	CV1	CV0	CV0
	CV3	CV2	CV2	CV1	CV1	CV0	CV0	CV0
	For 4x4 field block, each coefficient is mapped to one of the eight CV values as following:							
	none	CV6	CV3	CV1				
	CV7	CV6	CV3	CV1				
	CV5	CV4	CV2	CV0				
	CV5	CV4	CV2	CV0				
	For 8x8 field block, each coefficient is mapped to one of the eight CV values as following:							
	none	none	CV6	CV5	CV4	CV3	CV2	CV1
	none	CV7	CV6	CV5	CV4	CV3	CV2	CV1
	CV7	CV6	CV5	CV4	CV3	CV3	CV2	CV1
	CV7	CV6	CV5	CV4	CV3	CV2	CV2	CV1
	CV6	CV5	CV4	CV4	CV3	CV2	CV1	CV0
	CV6	CV5	CV4	CV3	CV2	CV2	CV1	CV0
	CV5	CV5	CV4	CV3	CV2	CV1	CV1	CV0



MFX_AVC_SLICE_STATE									
		CV5	CV5	CV4	CV3	CV2	CV1	CV1	CV0
		Value						Name	
		0 - 15							



MFx_BSP_BUF_BASE_ADDR_STATE

MFX_BSP_BUF_BASE_ADDR_STATE			
Source:		VideoCS	
Length Bias:		2	
This frame-level state command is used to specify all the buffer base addresses needed for the operation of the AVC Bit Stream Processing Units (for decoder, it is BSD Unit; for encoder, it is BSE Unit) For both encoder and decoder, currently it is assumed that all codec standards can share the same BSP_BUF_BASE_STATE. The simplicity of this command is the result of moving all the direct MV related processing into the ENC Subsystem. Since all implicit weight calculations and directMV calculations are done in ENC and all picture buffer management are done in the Host, there is no need to provide POC (POC List - FieldOrderCntList, CurrPic POC - CurrFieldOrderCnt) information to PAK. For decoder, all the direct mode information are sent in a separate slice-level command (AVC_DIRECTMODE_STATE command). In addition, in Encoder, the row stores for CABAC encoding and MB Parameters Construction (MPC) are combined into one single row store. The row stores specified in this command do not combine with those specified in the MFC_PIPE_BUF_ADDR_STATE command for hardware simplification reason.			
DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	3h PARALLEL_VIDEO_PIPE
		Format:	OpCode
	28:27	Pipeline	
		Default Value:	2h Pipeline
		Format:	OpCode
	26:24	Media Command Opcode	
		Default Value:	0h MFX_COMMON_STATE
		Format:	OpCode
	23:21	SubOpcode A	
		Default Value:	0h
		Format:	OpCode
	20:16	SubOpcode B	
		Default Value:	4h
Format:		OpCode	
15:12	Reserved		
	Format:	MBZ	
11:0	DWord Length		
	Default Value:	8h Excludes DWord (0,1)	
	Format:	=n Total Length - 2	
1	31:6	BSD/MPC Row Store Scratch Buffer Base Address - Read/Write	



MFX_BSP_BUF_BASE_ADDR_STATE

		This field provides the base address of the scratch buffer used by BSD (decoder) and MPC (encoder) unit to store MB information of the previous row for coding each macroblock in the current row. It is a private buffer used by the BSD (decoder) and MPC (encoder) hardware only. Its content is not accessible by software. ThisRow Store buffer must be 64-byte cacheline aligned. Hardware uses the horizontal address of the current macroblock to address this Row Store. For AVC BSD, 2 cacheline (CL) per MB when in MBAFF mode (row of MB pair); 1 CL per MB for non-MBAFF. So, to support 256 MBs per row (4K screen resolution), 2 * 256 * 64 bytes = 32,768 bytes are required. Cacheline alignment should be followed. For AVC MPC, 1 cachline for non-MBAFF, 2 cachelines for MBAFF per MB. For VC1, the BSD row store is 512-bit (one cacheline) per MB, times the number of MBs per picture MB row.											
		Programming Notes This is one of the four RowStore Scratch Buffers which can programmed to use the internal Media Storage (total size 640 CacheLine). When Deblocking Filter Row Store Scratch Buffer Cache Select is programmed to "1", this will be stored inside MFX Media Internal Storage. Driver then needs to program this Base Address between 0 to 639, indicating starting cacheline address location for this buffer. Driver needs to make sure the whole buffer fits into Media Internal Storage. <i>(Notes: 1 cachelines per MB for non-mbaff; 2 cachelines per MB pair for mbaff, and the buffer needs to have enough space for 1 MB (pair) row).</i>											
	5:0	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>		Format:	MBZ								
	Format:	MBZ											
2	31:16	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table> Reserved for 64-bit address extension.		Format:	MBZ								
	Format:	MBZ											
	15:0	BSD/MPC Row Store Scratch Buffer Base Address - Read/Write [47:32] Description This field is for the upper range of BSD/MPC Row Store Scratch Buffer Base Address. This field is used for 48-bit addressing.											
		3	31:15	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>		Format:	MBZ						
Format:			MBZ										
14:13	BSD/MPC Row Store Scratch Buffer - Tiled Resource Mode <table><tr><td>Format:</td><td>U2</td></tr></table> For Media Surfaces: This field specifies the tiled resource mode. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>TRMODE_NONE</td><td>No tiled resource</td></tr><tr><td>1h</td><td>TRMODE_TILEYF</td><td>4KB tiled resources</td></tr></table>		Format:	U2	Value	Name	Description	0h	TRMODE_NONE	No tiled resource	1h	TRMODE_TILEYF	4KB tiled resources
	Format:	U2											
	Value	Name	Description										
	0h	TRMODE_NONE	No tiled resource										
1h	TRMODE_TILEYF	4KB tiled resources											

**MFx_BSP_BUF_BASE_ADDR_STATE**

		2h	TRMODE_TILEYS	64KB tiled resources
		3h	Reserved	
	12	BSD/MPC Row Store Scratch Buffer Cache Select This field controls if Intra Row Store is going to store inside Media Internal Storage or to LLC.		
		Value	Name	Description
		0		Buffer going to LLC
		1		Buffer going to Internal Media Storage
	11	Reserved		
		Format:		MBZ
	10:9	Reserved		
		Format:		MBZ
	8:7	BSD/MPC Row Store Scratch Buffer - Arbitration Priority Control		
		Format:		U2
	6:1	This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.		
		Value	Name	
		00b	Highest priority	
		01b	Second highest priority	
		10b	Third highest priority	
		11b	Lowest priority	
		BSD/MPC Row Store Scratch Buffer - Index to Memory Object Control State (MOCS) Tables		
		Format:		U6
	0	The index to define the L3 and system cache memory properties. The details of the controls are further defined in L3 and Page walker (memory interface) control registers.		
		The field is defined to populate 64 different surface controls to be used concurrently. Related control registers can be updated during runtime.		
		Reserved		
		Reserved		
4	31:6	MPR Row Store Scratch Buffer Base Address - Read/Write (Decoder Only) This field provides the base address of the scratch buffer used by decoder's MPR unit to store MB information of the previous row for decoding each macroblock in the current row. It is a private buffer used by the MPR hardware only. Its content is not accessible by software.		
		Programming Notes The MPR Row Store buffer must be 64-byte cacheline aligned. Hardware uses the horizontal address of each macroblock to address the MPR Row Store. Except ILDB Control Data, all other operations does not cross slice boundary. This field is specified in frame-level.2 cacheline (CL) per MB when in MBAFF mode (row of MB pair); 1 CL per MB for non-MBAFF, So, to support 256 MBs per row (4K screen resolution), 2 * 256 * 64 bytes = 32,768 bytes are required. Cacheline alignment should be followed. This field is only valid for AVC decoder mode		



MFX_BSP_BUF_BASE_ADDR_STATE

		This is one of the four RowStore Scratch Buffers which can programmed to use the internal Media Storage (total size 640 CacheLine). When Deblocking Filter Row Store Scratch Buffer Cache Select is programmed to "1", this will be cache inside MFX Media Internal Storage. Driver then needs to program this Base Address between 0 to 639, indicating starting cachelines address location for this buffer. Driver needs to make sure the whole buffer fits into Media Internal Storage <i>(Notes: 1 cachelines per MB for non-mbaff; 2 cachelines per MB pair for mbaff, and the buffer needs to have enough space for 1 MB (pair) row).</i>															
	5:0	Reserved															
		Format:	MBZ														
5	31:16	Reserved															
		Format:	MBZ														
	Reserved for 64-bit address extension.																
	15:0	MPR Row Store Scratch Buffer Base Address - Read/Write [47:32] This field is for the upper range of MPR Row Store Scratch Buffer Base Address. This field is used for 48-bit addressing.															
6	31:15	Reserved															
		Format:	MBZ														
	14:13	MPR Row Store Scratch Buffer - Tiled Resource Mode															
		Format:	U2														
	For Media Surfaces: This field specifies the tiled resource mode.																
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>TRMODE_NONE</td><td>No tiled resource</td></tr><tr><td>1h</td><td>TRMODE_TILEYF</td><td>4KB tiled resources</td></tr><tr><td>2h</td><td>TRMODE_TILEYS</td><td>64KB tiled resources</td></tr><tr><td>3h</td><td>Reserved</td><td></td></tr></table>	Value	Name	Description	0h	TRMODE_NONE	No tiled resource	1h	TRMODE_TILEYF	4KB tiled resources	2h	TRMODE_TILEYS	64KB tiled resources	3h	Reserved	
	Value	Name	Description														
	0h	TRMODE_NONE	No tiled resource														
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	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td></td><td>Buffer going to LLC</td></tr><tr><td>1</td><td></td><td>Buffer going to Internal Media Storage</td></tr></table>	Value	Name	Description	0		Buffer going to LLC	1		Buffer going to Internal Media Storage							
Value	Name	Description															
0		Buffer going to LLC															
1		Buffer going to Internal Media Storage															
11	Reserved																
	Format:	MBZ															
10:9	Reserved																
	Format:	MBZ															
8:7	MPR Row Store Scratch Buffer - Arbitration Priority Control																
	Format:	U2															



MFX_BSP_BUF_BASE_ADDR_STATE																	
		This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.															
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>00b</td><td>Highest priority</td></tr><tr><td>01b</td><td>Second highest priority</td></tr><tr><td>10b</td><td>Third highest priority</td></tr><tr><td>11b</td><td>Lowest priority</td></tr></table>	Value	Name	00b	Highest priority	01b	Second highest priority	10b	Third highest priority	11b	Lowest priority					
		Value	Name														
		00b	Highest priority														
		01b	Second highest priority														
		10b	Third highest priority														
11b	Lowest priority																
6:1	MPR Row Store Scratch Buffer - Index to Memory Object Control State (MOCS) Tables																
<table><tr><td>Format:</td><td>U6</td></tr></table>		Format:	U6														
Format:	U6																
The index to define the L3 and system cache memory properties. The details of the controls are further defined in L3 and Page walker (memory interface) control registers. The field is defined to populate 64 different surface controls to be used concurrently. Related control registers can be updated during runtime.																	
0	Reserved																
7	31:6	Bitplane Read Buffer Base Address It must be cacheline aligned (i.e. 64 bytes address boundary), so lower bit 0 to 5 are used for controlling information.(In Cantiga, this field must be dword aligned.)Bitplane buffer is a linear buffer. In VC1 Long format, it is written by an application. In VC1 Short Format, it is written and read by H/W only.For VC1 intel Long Format : it is a read-only bufferFor VC1 DXVA2 Short Format : it is a write and a read bufferThis field is only valid for VC1 decoder mode.															
	5:0	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ													
	Format:	MBZ															
8	31:16	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table> Reserved for 64-bit address extension.	Format:	MBZ													
Format:	MBZ																
	15:0	Bitplane Read Buffer Base Address - Read/Write [47:32] This field is for the upper range of Bitplane Read Buffer Base Address. This field is used for 48-bit addressing.															
	9	31:15	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ												
Format:	MBZ																
	14:13	Bitplane Read Buffer - Tiled Resource Mode															
		<table><tr><td>Format:</td><td>U2</td></tr></table>	Format:	U2													
		Format:	U2														
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		Value	Name	Description													
0h	TRMODE_NONE	No tiled resource															
1h	TRMODE_TILEYF	4KB tiled resources															
2h	TRMODE_TILEYS	64KB tiled resources															
3h	Reserved																



MFX_BSP_BUF_BASE_ADDR_STATE																
	12:11	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ												
	Format:	MBZ														
	10:9	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ												
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	8:7	Bitplane Read Buffer - Arbitration Priority Control <table><tr><td>Format:</td><td>U2</td></tr><tr><td colspan="2">This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.</td></tr><tr><td>Value</td><td>Name</td></tr><tr><td>00b</td><td>Highest priority</td></tr><tr><td>01b</td><td>Second highest priority</td></tr><tr><td>10b</td><td>Third highest priority</td></tr><tr><td>11b</td><td>Lowest priority</td></tr></table>	Format:	U2	This field controls the priority of arbitration used in the GAC/GAM pipeline for this surface.		Value	Name	00b	Highest priority	01b	Second highest priority	10b	Third highest priority	11b	Lowest priority
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Format:	U6															
0	Reserved															



MI_ATOMIC

MI_ATOMIC											
Source:	BSpec										
Length Bias:	2										
Description											
MI_ATOMIC is used to carry atomic operation on data in graphics memory. Atomic operations are supported on data granularity of 4B, 8B and 16B. The atomic operation leads to a read-modify-write operation on the data in graphics memory with the option of returning value. The data in graphics memory is modified by doing arithmetic and logical operation with the inline/indirect data provided with the MI_ATOMIC command. Inline/Indirect provided in the command can be one or two operands based on the atomic operation. Ex: Atomic-Compare operation needs two operands while Atomic-Add operation needs single operand and Atomic-increment requires no operand. Refer "Atomics" sub-section under "L3 Cache and URB" section for detailed atomic operations supported. Atomic operations can be enabled to return value by setting "Return Data Control" field in the command, return data is stored to CS_GPR registers. CS_GPR4/5 registers are updated with memory Return Data based on the "Data Size". Each GPR register is qword in size and occupies two MMIO registers. Note: Any references to CS_GPR registers in the command should be understood as the CS_GPR registers belonging to the corresponding engines *CS_GPR registers. <table><tr><th>Engine Name</th><th>Corresponding GPR Registers</th></tr><tr><td>RCS</td><td>CS_GPR</td></tr><tr><td>BCS</td><td>BCS_GPR</td></tr><tr><td>VCS</td><td>VCS_GPR</td></tr><tr><td>VECS</td><td>VECS_GPR</td></tr></table> Indirect Source Operands: Operand1 is sourced from [CS_GPR1, CS_GPR0] Operand2 is sourced from [CS_GPR3, CS_GPR2] Read return Data is stored in [CS_GPR_5, CS_GPR4] When "Data Size" is DWORD lower dword of CS_GPR4 (Qword) is updated with the dword data returned from memory. When "Data Size" is QWORD only CS_GPR4 (Qword) is updated with the qword data returned from memory. When the data size is OCTWORD CS_GPR4/5 are updated with the OCTWORD data returned from memory. CS_GPR4 is loaded with lower qword returned from memory and CS_GPR5 is loaded with upper qword returned from memory.		Engine Name	Corresponding GPR Registers	RCS	CS_GPR	BCS	BCS_GPR	VCS	VCS_GPR	VECS	VECS_GPR
Engine Name	Corresponding GPR Registers										
RCS	CS_GPR										
BCS	BCS_GPR										
VCS	VCS_GPR										
VECS	VECS_GPR										
Programming Notes	Source										
- When Inline Data mode is not set, Dwords 3..10 must not be included as part of the command. Dword Length field in the header must be programmed accordingly. - When Inline Data Mode is set, Dwords3..10 must be included based on the Data Size field of the header. Both Operand-1 and Operand-2 dwords must be programmed based on the Data Size field. Operand-2 must be programmed to 0x0 if the atomic operation doesn't require it. Dword Length field in the											



MI_ATOMIC

header must be programmed accordingly.

Engines must be IDLE prior to command stream parsing MI_ATOMIC command. MI_FLUSH_DW prior to the MI_ATOMIC command would ensure the engine is IDLE prior to the atomic operation.

BlitterCS, VideoCS, VideoEnhancementCS

Workaround

Workaround: SW must ensure to program a PIPECONTROL command with CS Stall bit set prior to programming MI_ATOMIC command.

DWord	Bit	Description	
0	31:29	Command Type	
		Default Value:	0h MI_COMMAND
		Format:	OpCode
	28:23	MI Command Opcode	
		Default Value:	2Fh MI_ATOMIC
		Format:	OpCode
	22	Memory Type	
		This bit will be ignored and treated as if clear when executing from a non-privileged batch buffer. It is allowed for this bit to be clear when executing this command from a privileged (secure) batch buffer. This bit must be 1 if the Per Process GTT Enable bit is clear.	
		Value	Name
		0h	Per Process Graphics Address
		1h	Global Graphics Address This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.
	21	Reserved	
		Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
		Format:	MBZ
	21	Post-Sync Operation	
		Source:	RenderCS
		Value	Name
		0h	No Post Sync Operation Command is executed as usual.
		1h	Post Sync Operation MI_ATOMIC command is executed as a pipelined PIPE_CONTROL flush command with Atomics operation as post sync operation. Flush completion only guarantees the workload prior to this command is pushed till Windower unit and completion of any



MI_ATOMIC

outstanding flushes issued prior to this command.

When this bit set following restrictions apply to atomic operation:

- Non-Compare atomic operations are supported on data granularity of 4B and 8B. DW3 is the lower dword of the operand and DW4 is the upper dword of the operand for the atomic operation.
- Compare atomic operations are supported on data granularity of 4B. DW3 is Operand-0 and DW4 is Operand-1 for the atomic operation.
- Atomic operations to GGTT/PPGTT memory surface are supported.
- Only Inline data mode for atomic operand is supported, no support for indirect data mode.
- No support for Return Data Control functionality.
- No support for atomic operations on data granularity of 16B.
- No support for compare atomic operations on data granularity of 8B.

Programming Notes

Any desired pipeline flush operation can be achieved by programming PIPE_CONTROL command prior to this command.

When this bit is set Command Streamer sends a flush down the pipe and the atomic operation is saved as post sync operation. Command streamer goes on executing the following commands. Atomic operation saved as post sync operation is executed at some point later on completion of corresponding flush issued.

When this bit is set atomic semaphore signal operation will be out of order with rest of the MI commands programmed in the ring buffer or batch buffer, it will be in order with respect to the post sync operations resulting due to PIPE_CONTROL command.

Workaround

PIPECONTROL command with "Command Streamer Stall Enable" must be programmed prior to programming MI_ATOMIC command with Post-Sync Operation set in GPGPU mode of operation (i.e when PIPELINE_SELECT command is set to GPGPU mode of operation).

20:19

Data Size

This field indicates the size of the operand in dword/qword/octword on which atomic operation will be performed. Data size must match with the Atomic Opcode. Operation Data size could be 4B, 8B or 16B

Value	Name	Description
0h	DWORD	Operand size used by Atomic Operation is DWORD.
1h	QWORD	Operand Size used by Atomic Operation is QWORD.



MI_ATOMIC				
		2h	OCTWORD	Operand Size used by Atomic Operation is OCTWORD.
		3h	RESERVED	
	18	Inline Data This bit when set indicates the source operands are provided in line within the command. When reset the source operands are in CS_GPR registers.		
		Programming Notes CS_GPR registers must be programmed with appropriate values before issuing MI_ATOMIC command with this field reset.		
	17	CS STALL This bit when set command stream waits for completion of this command before executing the next command.		
		Programming Notes Render Command Streamer Only: CS will not guarantee atomic operation to be complete upon setting this bit along with Post Sync Operation set. When Post Sync Operation is set, this bit has no significance.		Source
				RenderCS
		Workaround Workaround: When CS STALL bit is set, Return Data Control must also be set in MI_ATOMIC command.		
	16	Return Data Control Source: RenderCS, BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS		
		Description When Return Data Control is set the read return feature will be enabled during the atomic operation. Data is stored in CS_GPR5/4 registers unconditionally on completion of the atomic operation. On data return CS_GPR5/4 Registers are updated based on the "Data Size" field. When "Data Size" is DWORD lower dword of CS_GPR4 (Qword) is updated with the dword data returned from memory. When "Data Size" is QWORD only CS_GPR4 (Qword) is updated with the qword data returned from memory. When the data size is OCTWORD CS_GPR4/5 are updated with the OCTWORD data returned from memory. CS_GPR4 is loaded with lower qword returned from memory and CS_GPR5 is loaded with upper qword returned from memory.		
		Workaround Workaround: When Return Data Control bit is set, CS STALL must also be set in MI_ATOMIC command.		
	15:8	ATOMIC OPCODE This field selects the kind of atomic operation to be performed. Refer "Atomics" sub-section of "L3 Cache and URB" section of the B-spec for atomic opcode encoding and operation.		
	7:0	DWord Length Format:		=n



MI_ATOMIC											
		Total Length - 2. Excludes DWord (0,1). <table><tr><th>Value</th><th>Name</th><th>Exists If</th></tr><tr><td>1h</td><td>Inline Data 0 [Default]</td><td>([Inline Data]==0)</td></tr><tr><td>9h</td><td>Inline Data 1</td><td>([Inline Data]==1)</td></tr></table>	Value	Name	Exists If	1h	Inline Data 0 [Default]	([Inline Data]==0)	9h	Inline Data 1	([Inline Data]==1)
Value	Name	Exists If									
1h	Inline Data 0 [Default]	([Inline Data]==0)									
9h	Inline Data 1	([Inline Data]==1)									
1	31:2	Memory Address <table><tr><td>Format:</td><td>GraphicsAddress[31:2]</td></tr></table> This field contains the graphics memory address of the data on which atomic operation has to be performed. Atomic operation can be performed on data granularity of 4B, 8B or 16B and hence the Address has to be correspondingly aligned to 4B,8B or 16B respectively.	Format:	GraphicsAddress[31:2]							
	Format:	GraphicsAddress[31:2]									
1:0	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ								
Format:	MBZ										
2	31:16	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ							
	Format:	MBZ									
15:0	Memory Address High This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space.										
3	31:0	Operand1 Data Dword 0 <table><tr><td>Format:</td><td>U32</td></tr></table> Dword0 of Operand1 when Inline Data mode is set.	Format:	U32							
		Format:	U32								
4	31:0	Operand2 Data Dword 0 <table><tr><td>Format:</td><td>U32</td></tr></table> Dword0 of Operand2 when Inline Data mode is set.	Format:	U32							
		Format:	U32								
5	31:0	Operand1 Data Dword 1 <table><tr><td>Format:</td><td>U32</td></tr></table> Dword1 of Operand1 when Inline Data mode is set.	Format:	U32							
		Format:	U32								
6	31:0	Operand2 Data Dword 1 <table><tr><td>Format:</td><td>U32</td></tr></table> Dword1 of Operand2 when Inline Data mode is set.	Format:	U32							
		Format:	U32								
7	31:0	Operand1 Data Dword 2 <table><tr><td>Format:</td><td>U32</td></tr></table> Dword2 of Operand1 when Inline Data mode is set.	Format:	U32							
		Format:	U32								
8	31:0	Operand2 Data Dword 2 <table><tr><td>Format:</td><td>U32</td></tr></table> Dword2 of Operand2 when Inline Data mode is set.	Format:	U32							
		Format:	U32								
9	31:0	Operand1 Data Dword 3 <table><tr><td>Format:</td><td>U32</td></tr></table> Dword3 of Operand1 when Inline Data mode is set.	Format:	U32							
		Format:	U32								



MI_ATOMIC		
10	31:0	Operand2 Data Dword 3
		Format: U32
		Dword3 of Operand2 when Inline Data mode is set.



MI_SEMAPHORE_WAIT

MI_SEMAPHORE_WAIT		
Source:	CommandStreamer	
Length Bias:	2	
Description		
This command supports memory based Semaphore WAIT. Memory based semaphores will be used for synchronization between the Producer and the Consumer contexts. Producer and Consumer Contexts could be running on different engines or on the same engine inside GT. Running on the same engine is only possible when execlists are enabled. Producer Context implements a Signal and Consumer context implements a Wait. Command Streamer on parsing this command fetches data from the Semaphore Address mentioned in this command and compares it with the inline Semaphore Data Dword. • If comparison passes, the command streamer moves to the next command. • When execlists are enabled, if comparison fails Command streamer switches out the context. Context switch can be inhibited by setting "Inhibit Synchronous Context Switch" in CTEXT_SR_CTL register. • In ring buffer mode of scheduling or Execlist with "Inhibit Synchronous context Switch", if comparison fails, Command Streamer evaluates the Compare Operation based on the Wait Mode until the compare operation is true or Wait is canceled by SW. • Exec-List Scheduling: CS generates semaphore wait interrupt to the scheduler when MI_SEMAPHORE_WAIT command is un-successful and when "Inhibit Synchronous Context Switch" is set. Scheduler can use this interrupt to preempt the context waiting on semaphore wait. • Ring Buffer Scheduling: CS generates semaphore wait interrupt to the scheduler when MI_SEMAPHORE_WAIT command is un-successful. MI_SEMPHORE_SIGNAL and MI_SEMAPHORE_WAIT together replace the MI_SEMAPHORE_MBOX command. MI_SEMAPHORE_WAIT command also supports register based Semaphore WAIT. Command Streamer on parsing this command fetches data from the MMIO offset mentioned in this command and compares it with the inline Semaphore Data Dword. This functionality is supported when "Register Poll" bit is set in the command header. In register poll mode of operation "Wait Mode" supported is always Poll mode and no Signal mode is supported. • If comparison passes, the command streamer moves to the next command. • Unlike in Memory based semaphore, there is no context switch or preemption supported in Register Poll mode of operation. Semaphore wait interrupt is not generated by default on wait un-successful in "Register Poll" mode. • Register Poll mode of Semaphore Wait command operation is privileged and will not be supported from PPGTT batch buffers. • HW will not trigger Render DOP CG on semaphore wait unsuccessful in register poll mode of operation.		
DWord	Bit	Description
0	31:29	Command Type
		Default Value: 0h MI_COMMAND



MI_SEMAPHORE_WAIT

MI_SEMAPHORE_WAIT			
		Format:	OpCode
28:23	MI Command Opcode		
	Default Value:	1Ch MI_SEMAPHORE_WAIT	
	Format:	OpCode	
22	Memory Type		
	This bit will be ignored and treated as if clear when executing from a non-privileged batch buffer. It is allowed for this bit to be clear when executing this command from a privileged (secure) batch buffer. This bit <i>must</i> be 1 if the Per Process GTT Enable bit is clear.		
	Value	Name	Description
	0h	Per Process Graphics Address	
	1h	Global Graphics Address	This command will use the global GTT to translate the Address and this command must be executing from a privileged (secure) batch buffer.
21:18	Reserved		
	Format:	MBZ	
17	Reserved		
	Format:	MBZ	
16	Register Poll Mode		
	This field control the semaphore wait behavior of polling from memory vs MMIO register.		
	Value	Name	Description
	1h	Register Poll [Default]	In this mode HW periodically reads the semaphore data from MMIO register instead of memory for comparison until the condition is satisfied. Periodicity will be mentioned in a SEMA_WAIT_POLL register. When operating in register poll mode, DW2 "Semaphore Address" (bits 22:2) carries the register MMIO offset to be polled. In register poll mode "Memory Type" field of this command are ignored by HW.
	0h	Memory Poll	In this mode HW will functional as in regular mode and checks for semaphore data in memory.
Programming Notes			
In register poll mode of operation of MI_SEMAPHORE_WAIT command, context switch and preemption are not supported on wait un-successful. "Wait Mode" must be always set to "Polling Mode" when Register Poll Mode is enabled.			
15	Wait Mode		
	This bit specifies the WAIT behavior when the semaphore comparison fails and before the context is switched out.		
	Value	Name	Description



MI_SEMAPHORE_WAIT

MI_SEMAPHORE_WAIT					
		1h	Polling Mode	In this mode HW periodically reads the semaphore data from memory for comparison until it is context switched out. Periodicity will be mentioned in a SEMA_WAIT_POLL register.	
		0h	Signal Mode	In this mode HW will reacquire the semaphore data from memory on receiving SIGNAL with the same Context ID. In ring buffer mode of scheduling Context ID associated with SIGNAL is ignored and always treated as a match.	
		Programming Notes			
		Wait Mode must be always set to Polling Mode when Register Poll Mode is enabled.			
14:12	Compare Operation				
	This field specifies the operation that will be executed to create the result that will either allow the context to continue or wait.				
	SAD = Semaphore Address Data SDD = Semaphore Data Dword				
	Value	Name	Description		
	0h	SAD_GREATER_THAN_SDD	If Indirect fetched data is greater than inline data then continue.		
	1h	SAD_GREATER_THAN_OR_EQUAL_SDD	If Indirect fetched data is greater than or equal to inline data then continue.		
	2h	SAD_LESS_THAN_SDD	If Indirect fetched data is less than inline data then continue.		
	3h	SAD_LESS_THAN_OR_EQUAL_SDD	If Indirect fetched data is less than or equal to inline data then continue.		
	4h	SAD_EQUAL_SDD	If Indirect fetched data is equal to inline data then continue.		
	5h	SAD_NOT_EQUAL_SDD	If Indirect fetched data is not equal to inline data then continue.		
	6h	Reserved			
	7h	Reserved			
	11:8	Reserved			
		Format:		MBZ	
7:0	DWord Length				
	Format:		=n Total Length - 2		
	Value	Name			
2h	Excludes DWord (0,1) [Default]				
1	31:0	Semaphore Data Dword			



MI_SEMAPHORE_WAIT			
2..3		Format:	U32
		This Data dword is supplied by software to control execution of the command buffer. This value is used as part of the comparison to result in waiting or continuing in the command parser if enabled.	
	63:2	Semaphore Address	
		Format:	GraphicsAddress63-2
		Register Poll Mode: In Register Poll mode of operation, Bits 22:2 (Bits 63:23 are reserved MBZ, HW enforced) specify the MMIO offset of the register for the semaphore. Non Register Poll Mode: This field is the Graphics Memory Address of the 32-bit value for the semaphore. GraphicsAddress [63:48] are ignored by the HW and assumed to be in correct canonical form.	
	1:0	Reserved	
		Format:	MBZ



PIPE_CONTROL

PIPE_CONTROL		
Source: RenderCS		
Length Bias: 2		
The PIPE_CONTROL command is used to effect the synchronization described above.		
DWord	Bit	Description
0	31:29	Command Type
		Default Value: 3h GFXPIPE
		Format: OpCode
	28:27	Command SubType
		Default Value: 3h GFXPIPE_3D
		Format: OpCode
	26:24	3D Command Opcode
		Default Value: 2h PIPE_CONTROL
		Format: OpCode
	23:16	3D Command Sub Opcode
		Default Value: 0h PIPE_CONTROL
		Format: OpCode
	15:10	Reserved
		Format: MBZ
	9	Reserved
	8	Reserved
	7:0	DWord Length
		Default Value: 4h DWORD_COUNT_n
		Format: =n
	Total Length - 2. Excludes DWord (0,1).	
1	31	Reserved
		Format: MBZ
	30	Reserved
		Format: MBZ
	29	Reserved
		Format: MBZ
	28	Reserved
		Format: MBZ
	27	Reserved



PIPE_CONTROL

PIPE_CONTROL			
26	Flush LLC		
	Format:		Enable
	If enabled, at the end of the current pipe-control the last level cache is cleared of all the cachelines which have been determined as being part of the Frame Buffer.		
	Programming Notes		
	SW must always program Post-Sync Operation to "Write Immediate Data" when Flush LLC is set.		
25	Reserved		
	Format:		MBZ
24	Destination Address Type		
	Defines address space of Destination Address		
	Value	Name	Description
	0h	PPGTT	Use PPGTT address space for DW write
	1h	GGTT	Use GGTT address space for DW write
	Programming Notes		
Ignored if ""No Write" is selected in Operation.			
23	LRI Post Sync Operation		
	Value	Name	Description
	0h	No LRI Operation	No LRI operation occurs as a result of this instruction. The Post-Sync Operation field is valid and may be used to specify an operation.
	1h	MMIO Write Immediate Data	Write the DWord contained in Immediate Data Low (DW3) to the MMIO offset specifed in the Address field.
	Programming Notes		
	This bit caues a post sync operation with an LRI (Load Register Immediate) operation. If this bit is set then the Post-Sync Operation field must be cleared.		
22	Reserved		
21	Store Data Index		
	Format:		U1
	Description		
Ring Buffer Mode Scheduling: This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is actually an index into the global hardware status page. This bit only applies to the Global HW status page. If this field is 1, the Destination Address Type in this command must be set to 1 (GGTT).			
Execlist Mode Scheduling: This field is valid only if the post-sync operation is not 0. If this bit is set, the store data address is index into the global hardware status page when destination address type in the command is set to 1 (GGTT). The store data address is index into the per-process hardware status page when destination address type in the command is set to 0 (PPGTT).			



PIPE_CONTROL		
20	Command Streamer Stall Enable	
	Format:	U1
	If ENABLED, the sync operation will not occur until all previous flush operations pending a completion of those previous flushes will complete, including the flush produced from this command. This enables the command to act similar to the legacy MI_FLUSH command.	
	Programming Notes	
	A PIPE_CONTROL with Command Streamer Stall Enable set must be sent prior to enabling tessellation or a geometry shader.	
19	Reserved	
18	TLB Invalidate	
	Format:	U1
	If ENABLED, all TLBs belonging to Render Engine will be invalidated once the flush operation is complete. Note that if the flush TLB invalidation mode is clear, a TLB invalidate will occur irrespective of this bit setting	
	If ENABLED, PIPE_CONTROL command will flush the in flight data written out by render engine to Global Observation point on flush done. Also Requires stall bit ([20] of DW1) set.	
	Programming Notes	
	If ENABLED, all TLBs belonging to Render Engine will be invalidated once the flush operation is complete. Note that if the flush TLB invalidation mode is clear, a TLB invalidate will occur irrespective of this bit setting.	
	Post Sync Operation or CS stall must be set to ensure a TLB invalidate occurs. Otherwise no cycle will occur to the TLB cache to invalidate.	
17	Reserved	
	Format:	MBZ
16	Generic Media State Clear	
	Format:	Disable
	If set, all generic media state context information will be invalidated. Any state invalidated will not be saved as part of the render engine context image. The state only only become valid once it is parsed by the command streamer.	
	Workaround	
	Workaround: PIPECONTROL command with "Command Streamer Stall Enable" must be programmed prior to programming a PIPECONTROL command with "Media State Clear" set in GPGPU mode of operation (i.e when PIPELINE_SELECT command is set to GPGPU mode of operation).	
15:14	Post Sync Operation	
	Description	
	This field specifies an optional action to be taken upon completion of the synchronization operation.	



PIPE_CONTROL

This field must be cleared if the LRI Post-Sync Operation bit is set.

Value	Name	Description
0h	No Write	No write occurs as a result of this instruction. This can be used to implement a "trap" operation, etc.
1h	Write Immediate Data	Write the QWord containing Immediate Data Low, High DWs to the Destination Address
2h	Write PS Depth Count	Write the 64-bit PS_DEPTH_COUNT register to the Destination Address
3h	Write Timestamp	Write the 64-bit TIMESTAMP register (i.e. "Reported Timestamp Count" 0x2358 for render pipe) to the Destination Address.

Programming Notes

If executed in non-secure batch buffer, the address given will be in a PPGTT address space. If in a secure ring or batch, address given will be in GGTT space

Workaround

Workaround: PIPECONTROL command with "Command Streamer Stall Enable" must be programmed prior to programming a PIPECONTROL command with Post Sync Op in GPGPU mode of operation (i.e when PIPELINE_SELECT command is set to GPGPU mode of operation).

13 Depth Stall Enable

Format:	Enable

This bit must be set when obtaining a "visible pixel" count to preclude the possible inclusion in the PS_DEPTH_COUNT value written to memory of some fraction of pixels from objects initiated after the PIPE_CONTROL command.

Value	Name	Description
0h	Disable	3D pipeline will not stall subsequent primitives at the Depth Test stage.
1h	Enable	3D pipeline will stall any subsequent primitives at the Depth Test stage until the Sync and Post-Sync operations complete.

Programming Notes

This bit must be DISABLED for operations other than writing PS_DEPTH_COUNT.

This bit will have no effect (besides preventing write cache flush) if set in a PIPE_CONTROL command issued to the Media pipe.

12 Render Target Cache Flush Enable

Format:	Enable

Setting this bit will force Render Cache to be flushed to memory prior to this synchronization point completing. This bit must be set for all write fence sync operations to assure that results from operations initiated prior to this command are visible in memory once software observes this synchronization.

**PIPE_CONTROL**

PIPE_CONTROL												
	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable Flush</td><td>Render Target Cache is NOT flushed.</td></tr><tr><td>1h</td><td>Enable Flush</td><td>Render Target Cache is flushed.</td></tr></table>	Value	Name	Description	0h	Disable Flush	Render Target Cache is NOT flushed.	1h	Enable Flush	Render Target Cache is flushed.		
Value	Name	Description										
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Format:	Enable											
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8	<table><tr><th colspan="2">Notify Enable</th></tr><tr><td>Format:</td><td>Enable</td></tr><tr><td colspan="2">If ENABLED, a Sync Completion Interrupt will be generated (if enabled by the MI Interrupt Control registers) once the sync operation is complete. See Interrupt Control Registers in Memory Interface Registers for details.</td></tr></table>		Notify Enable		Format:	Enable	If ENABLED, a Sync Completion Interrupt will be generated (if enabled by the MI Interrupt Control registers) once the sync operation is complete. See Interrupt Control Registers in Memory Interface Registers for details.					
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7	<table><tr><th colspan="2">Pipe Control Flush Enable</th></tr></table>		Pipe Control Flush Enable									
Pipe Control Flush Enable												



PIPE_CONTROL

		Format:	Enable
		Hardware on parsing PIPECONTROL command with Pipe Control Flush Enable set will wait for all the outstanding post sync operations corresponding to previously executed PIPECONTROL commands are complete before making forward progress.	
6	Reserved		
5	DC Flush Enable		
		Format:	Enable
		Setting this bit enables flushing of the L3\$ portions that caches DC writes.	
		Programming Notes	
		DC Flush (L3 Flush) by default doesn't result in flushing/invalidating the IA Coherent lines from L3\$, however this can be achieved by setting control bit "Pipe line flush Coherent lines" in "L3SQCREG4" register.	
4	VF Cache Invalidation Enable		
		Format:	Enable
		Setting this bit is independent of any other bit in this packet. This bit controls the invalidation of VF address based cache at the top of the pipe i.e. at the parsing time.	
		Programming Notes	
		If the VF Cache Invalidation Enable is set to a 1 in a PIPE_CONTROL, a separate Null PIPE_CONTROL, all bitfields sets to 0, with the VF Cache Invalidation Enable;set to 0 needs to be sent prior to the PIPE_CONTROL with VF Cache Invalidation Enable set to a 1.	
		As the VF, VFR data caches do not support a full address tag, SW shall invalidate the VF, VFR cache before a draw call that uses modified VERTEX_BUFFER state. Failure to do so may result in erroneous hits in the cache.	
		Workaround	
		Workaround When VF Cache Invalidate is set "Post Sync Operation" must be enabled to "Write Immediate Data" or "Write PS Depth Count" or "Write Timestamp".	
3	Constant Cache Invalidation Enable		
		Format:	Enable
		Setting this bit is independent of any other bit in this packet. This bit controls the invalidation of the constant cache at the top of the pipe i.e. at the parsing time.	
2	State Cache Invalidation Enable		
		Format:	Enable
		Setting this bit is independent of any other bit in this packet. This bit controls the invalidation of the L1 and L2 state caches at the top of the pipe i.e. at the parsing time.	
1	Stall At Pixel Scoreboard		
		Format:	Enable
		Defines the behavior of PIPE_CONTROL command at the pixel scoreboard.	

**PIPE_CONTROL**

PIPE_CONTROL											
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Disable</td><td>Stall at the pixel scoreboard is disabled.</td></tr><tr><td>1h</td><td>Enable</td><td>Stall at the pixel scoreboard is enabled.</td></tr></table>	Value	Name	Description	0h	Disable	Stall at the pixel scoreboard is disabled.	1h	Enable	Stall at the pixel scoreboard is enabled.
		Value	Name	Description							
		0h	Disable	Stall at the pixel scoreboard is disabled.							
		1h	Enable	Stall at the pixel scoreboard is enabled.							
		Programming Notes									
	This bit must be DISABLED for End-of-pipe (Read) fences, PS_DEPTH_COUNT or TIMESTAMP queries. This bit is ignored if Depth Stall Enable is set. Further the render cache is not flushed even if Write Cache Flush Enable bit is set.										
	0	Depth Cache Flush Enable									
	<table><tr><td>Format:</td><td>Enable</td></tr></table>		Format:	Enable							
	Format:	Enable									
Setting this bit enables flushing (i.e. writing back the dirty lines to memory and invalidating the tags) of depth related caches. This bit applies to HiZ cache, Stencil cache and depth cache.											
<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Flush Disabled</td><td>Depth relates caches (HiZ, Stencil and Depth) are NOT flushed.</td></tr><tr><td>1h</td><td>Flush Enabled</td><td>Depth relates caches (HiZ, Stencil and Depth) are flushed.</td></tr></table>		Value	Name	Description	0h	Flush Disabled	Depth relates caches (HiZ, Stencil and Depth) are NOT flushed.	1h	Flush Enabled	Depth relates caches (HiZ, Stencil and Depth) are flushed.	
Value	Name	Description									
0h	Flush Disabled	Depth relates caches (HiZ, Stencil and Depth) are NOT flushed.									
1h	Flush Enabled	Depth relates caches (HiZ, Stencil and Depth) are flushed.									
Programming Notes											
Ideally depth caches need to be flushed only when depth is required to be coherent in memory for later use as a texture, source or honoring CPU lock. This bit must be DISABLED for End-of-pipe (Read) fences, PS_DEPTH_COUNT or TIMESTAMP queries.											
2	31:2	Address									
		<table><tr><td>Format:</td><td>GraphicsAddress[31:2]U32</td></tr></table>	Format:	GraphicsAddress[31:2]U32							
	Format:	GraphicsAddress[31:2]U32									
If Post Sync Operation is set to 1h ([DevIVB+]: LRI Post-Sync Operation must be clear): Bits 31:3 specify the QW address of where the Immediate Data following this DW in the packet to be stored. Bit 2 MBZ Ignored if "No Write" is the selected in Post-Sync Operation [DevIVB+]: If LRI Post-Sync Operation is set: Bits 22:2 (Bits 31:23 are reserved MBZ) specify the MMIO offset destination for the data in the Immediate Data Low (DW3) field. Only DW writes are valid.											
	1:0	Reserved									
<table><tr><td>Format:</td><td>MBZ</td></tr></table>			Format:	MBZ							
Format:	MBZ										
3	31:0	Address High									
		<table><tr><td>Format:</td><td>GraphicsAddress[63:32]U32</td></tr></table>	Format:	GraphicsAddress[63:32]U32							
		Format:	GraphicsAddress[63:32]U32								
This field specifies the 4GB aligned base address of gfx 4GB virtual address space within the host's 64-bit virtual address space. This field is valid only if the post-sync operation is not 0 and the LRI Post-Sync Operation is clear.											
4..5	63:0	Immediate Data									
		<table><tr><td>Format:</td><td>U64</td></tr></table>	Format:	U64							
		Format:	U64								
This field specifies the QWord value to be written to the targeted location. Only valid when Post-Sync Operation is 1h (Write Immediate Data) or LRI Post-Sync Operation is set. Ignored if Post-Sync Operation is "No write", "Write PS_DEPTH_COUNT" or "Write TIMESTAMP".											



Split Send Message

sends - Split Send Message	
Source:	Eulsa
Length Bias:	4
Description	
The sends instruction performs data communication between a thread and external function units, including shared functions (Sampler, Data Port Read, Data Port Write, URB, and Message Gateway) and some fixed functions (e.g. Thread Spawner, who also have an unique Shared Function ID). The sends instruction adds an entry to the EU's message request queue. The request message is stored in a block of contiguous GRF registers. The response message, if present, will be returned to a block of contiguous GRF registers. The return GRF writes may be in any order depending on the external function units. <src0> and <src1> are the lead GRF registers for the first and second block of the request respectively. <dest> is the lead GRF register for response. The message descriptor field <desc> contains the Message Length (the number of consecutive GRF registers corresponding to src0) and the Response Length (the number of consecutive GRF registers). It also contains the header present bit, and the function control signals. The extend message descriptor field <ex_desc> contains the target function ID, the Extended Message Length (the number of consecutive GRF registers corresponding to src1) and the extended function control signals. WrEn is forwarded to the target function in the message sideband. The sends instruction is the only way to terminate a thread. When the EOT (End of Thread) bit of <ex_desc> is set, it indicates the end of thread to the EU, the Thread Dispatcher and, in most cases, the parent fixed function. Message descriptor field <desc> can be a 32-bit immediate, imm32, or a 32-bit scalar register, <reg32a>. GEN restricts that the 32-bit scalar register <reg32a> must be the leading dword of the address register. It should be in the form of a0.0<0;1,0>:ud. When <desc> is a register operand, only the lower 31 bits of <reg32a> are used. Extended Message descriptor field <ex_desc> can be a 32-bit immediate, imm32 only. The bits3:0 of the <ex_desc> specifies the SFID for the message. The EOT field always comes from bit127 of the instruction word, which is the bit5 of <ex_desc>. A thread must terminate with a sends instruction with EOT turned on. The bits9:6 of <ex_desc> specify the extended message length and bits31:16 specify the 16bit extended function control. Interpretation of the extended function control signals is subject to the target external function. <src0> is a 256-bit aligned GRF register. It serves as the leading GRF register of the request. <src1> is a 256-bit aligned GRF register or a null register. It serves as the leading GRF register for the second block of the request when it is not a null register. It is required that the second block of GRFs does not overlap with the first block. If it is a null register the Extended Message Length must be 0. The sum of Message Length and Extended Message Length must not be greater than 15 on SKL. The source dependency control, {NoSrcDepSet} is used to control the setting of source dependency for both the sources. <dest> serves for two purposes: to provide the leading GRF register location for the response message if present, and to provide parameters to form the channel enable sideband signals. <dest> signals whether there is a response to the message request. It can be either a null register, a direct-addressed GRF register or a register-indirect GRF register. Otherwise, hardware behavior is undefined. If <dest> is null, there is no response to the request. Meanwhile, the Response Length field in <desc> must be 0. Certain types of message requests, such as memory write (store) through the Data Port, do not want	



sends - Split Send Message

response data from the function unit. If so, the posted destination operand can be null.

If <dest> is a GRF register, the register number is forwarded to the shared function. In this case, the target function unit must send one or more response message phases back to the requesting thread. The number of response message phases must match the Response Length field in <desc>, which of course cannot be zero. For some cases, it could be an empty return message. An empty return message is defined as a single phase message with all channel enables turned off.

The destination type field is always valid and is used to generate the WrEn. This is true even if <dest> is a null register (this is an exception for null as for most cases these fields are ignored by hardware).

The address immediates for indirect sources and destination must be oword aligned.

The 16-bit channel enables of the message sideband are formed based on the WrEn. Interpretation of the channel enable sideband signals is subject to the target external function. In general for a 'sends' instruction with return messages, they are used as the destination dword write mask for the GRF registers starting at <dest>. For a message that has multiple return phases, the same set of channel enable signals applies to all the return phases.

NoDDClr and NoDDChk must not be used for send instruction.

Send a message stored in GRF locations starting at <src0> followed by <src1> to a shared function identified by <ex_desc> along with control from <desc> and <ex_desc> with a GRF writeback location at <dest>.

Format:

[(pred)] sends (exec_size) <dest> <src0> <src1> <ex_desc> <desc>

Restriction

Restriction : Software must obey the following rules in signaling the end of thread using the sends instruction: The posted destination operand must be null. No acknowledgement is allowed for the sends instruction that signifies the end of thread. This is to avoid deadlock as the EU is expecting to free up the terminated thread's resource. A thread must terminate with a sends instruction with message to a shared function on the output message bus; therefore, it cannot terminate with a sends instruction with message to the following shared functions: Sampler unit, NULL function For example, a thread may terminate with a URB write message or a render cache write message. A root thread originated from the media (generic) pipeline must terminate with a sends instruction with message to the Thread Spawner unit. A child thread should also terminate with a sends to TS. Please refer to the Media Chapter for more detailed description. The sends instruction can not update accumulator registers. Saturate is not supported for sends instruction. ThreadCtrl encodings Switch is not supported for sends instruction. The sends with EOT should use register space R112-R127 for <src>. This is to enable loading of a new thread into the same slot while the message with EOT for current thread is pending dispatch. Any instruction updating the ARF must use a {Switch} if the ARF is not used before EOT.</src>

Restriction : The source dependency control, {NoSrcDepSet}, must not be set for the send instruction preceding a send instruction with EOT.

Syntax

[(pred)] sends (exec_size) reg greg greg imm32 imm32 [(pred)] sends (exec_size) reg greg greg imm32 reg32a

Pseudocode

Evaluate(WrEn); <MsgChEnable> = WrEn; <SourceReg0> = <src0>.RegNum; <SourceReg1>



sends - Split Send Message

```
= <src1>.RegNum; MessageEnqueue(<MsgChEnable>, <ResponseReg>, <SourceReg0>,
<SourceReg1>, <ex_desc>, <dest>);
```

Predication	Conditional Modifier	Saturation	Source Modifier
Y	N	N	N

DWord	Bit	Description
0..3	127:96	Message Format: EU_INSTRUCTION_OPERAND_SEND_MSG
	95:80	ExDesc[31:16] Format: ExtMsgDescpt[31:16]
	79	Source 0 Addressing Mode Format: AddrMode
	78	Reserved Exists If: ([Source 0 Addressing Mode]='Direct') Format: MBZ
	78	Source 0 Address Immediate Sign [9] Exists If: ([Source 0 Addressing Mode]='Indirect') Format: S9[9]
	77	SelReg32Desc
	76:73	Source 0 Address Subregister Number Exists If: ([Source 0 Addressing Mode]='Indirect')
	76:69	Source 0 Register Number Exists If: ([Source 0 Addressing Mode]='Direct')
	72:68	Source 0 Address Immediate [8:4] Exists If: ([Source 0 Addressing Mode]='Indirect') Format: S9[8:4]
	68	Source 0 Subregister Number Exists If: ([Source 0 Addressing Mode]='Direct')
	67:64	ExDesc[9:6] Format: ExtMsgDescpt[9:6]
	63	Destination Addressing Mode Format: AddrMode
	62	Destination Address Immediate Sign [9] Exists If: ([Destination Addressing Mode]='Indirect') Format: S9[9]



sends - Split Send Message

	62	Reserved	
		Exists If:	(([Destination Addressing Mode] == 'Direct')
		Format:	MBZ
	61	Reserved	
		Format:	MBZ
	60:57	Destination Address Subregister Number	
		Exists If:	(([Destination Addressing Mode] == 'Indirect')
	60:53	Destination Register Number	
		Exists If:	(([Destination Addressing Mode] == 'Direct')
	56:52	Destination Address Immediate [8:4]	
		Exists If:	(([Destination Addressing Mode] == 'Indirect')
		Format:	S9[8:4]
	52	Destination Subregister Number [4]	
		Exists If:	(([Destination Addressing Mode] == 'Direct')
	51:44	Source 1 Register Number	
	43:41	Reserved	
		Format:	MBZ
	40:37	Destination Type	
	36	Source 1 Register File	
		Format:	RegFile[0]
	35	Destination Register File	
		Format:	RegFile[0]
	34	MaskCtrl	
	33:32	Flag Register Number/Subregister Number	
	31:28	Controls B	
		Format:	EU_INSTRUCTION_CONTROLS_B
	27:24	Shared Function ID (SFID)	
		Format:	SFID
	23:8	Controls A	
		Format:	EU_INSTRUCTION_CONTROLS_A
	7	Reserved	
		Format:	MBZ
	6:0	Opcode	
		Format:	EU_OPCODE



Intel® Open Source HD Graphics

Programmer's Reference Manual

For the 2016 Intel Atom™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Apollo Lake" Platform (Broxton Graphics)

Volume 2b: Command Reference: Registers

May 2017, Revision 1.0



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Arbiter Control Register

GARBCNTLREG - Arbiter Control Register					
Register Space:		MMIO: 0/2/0			
Source:		BSpec			
Default Value:		0x29124100			
Size (in bits):		32			
Address:		0B004h			
DWord	Bit	Description			
0	31	Reserved			
	30	Disables hashing function <table><tr><td>Access:</td><td>R/W</td></tr></table> Disables hashing function to generate bank_id[1:0] for L3\$ bank accessing, and forces the use of address[7:6] for bank_id[1:0]. 0: (default) Hash function enabled to generate L3\$ bank IDs. 1: L3\$ address[7:6] used as L3\$ bank IDs. Incf_csr_l3bankidhashdis. (This bit needs to set corresponding bit lpfcon_csr_l3bankidhashdis in LPFC.)	Access:	R/W	
		Access:	R/W		
		29:28	Arbitration priority order between RCC and MSC <table><tr><td>Default Value:</td><td>10b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Arbitration priority order between RCC and MSC. 00b/11b: Invalid; default setting used. 10b: Default setting; RCC MSC (i.e., MSC has higher priority). 01b: RCC MSC (i.e., RCC has higher priority). Incf_csr_rcc_msc_pri[1:0].	Default Value:	10b
Default Value:	10b				
Access:	R/W				
27:22	Arbitration priority order between RCZ, STC, and HIZ <table><tr><td>Default Value:</td><td>100100b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Arbitration priority order between RCZ, STC, and HIZ. 100100b: Default setting; RCZ STC HIZ. (i.e., RCZ has lowest priority; HIZ has highest priority). 100001b: RCZ ; HIZ ; STC. 011000b: STC ; RCZ ; HIZ. 010010b: STC ; HIZ ; RCZ. 001001b: HIZ ; RCZ ; STC. 000110b: HIZ ; STC ; RCZ. Note: Others settings are invalid, and result in use of default. Incf_csr_rcz_stc_hiz_pri[5:0].	Default Value:	100100b	Access:	R/W
Default Value:	100100b				
Access:	R/W				

**GARBCNTLREG - Arbiter Control Register**

	21:19	Write data port arbitration priority between Z client writes and L3\$ evictions	
		Default Value:	010b
		Access:	R/W
		Z Max Write Request Limit Count (GFXC_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (both Slice 0 and 1). Minimum count value must be = 1. Incf_csr_wdpagapz[2:0].	
	18:16	Write data port arbitration priority between C client writes and Z/L3\$ writes/evictions	
		Default Value:	010b
		Access:	R/W
		C Max Request Limit Count (GFXZ_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (both Slice 0 and 1). Minimum count value must be = 1. Incf_csr_wdpagapc[2:0].	
	15	Reserved	
		Access:	RO
	14:12	L3 Max Write Request Limit Count	
		Default Value:	100b
		Access:	R/W
		L3 Max Write Request Limit Count (GFXL3_MRLC). This is the MAX number of Allowed Requests Count - These counters keep track of the accepted requests from each engine. Requests are counted, regardless of kind of cycle (Miss/Hit/Present). Minimum count value must be = 1. Incf_csr_wdpagapl3[2:0].	
	11:9	Reserved	
		Access:	RO
	8	GAPs_fixarb_en	
		Default Value:	1b
		Access:	R/W
		Incf_csr_gaps_fixarb_en.	
	7	Reserved1	
		Access:	RO
	6:0	Reserved	
		Access:	RO



ASL Storage

ASLS_0_2_0_PCI - ASL Storage			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	000FCh		
This is a software scratch register. The exact bit register usage must be worked out in common between System BIOS and driver software. For each device, the ASL control method requires two bits for DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for DGS (enable/disable requested), and two bits for DCS (enabled now/disabled now, connected or not).			
DWord	Bit	Description	
0	31:0	Device Switching Storage	
		Default Value:	0000000000000000000000000000000b
		Access:	R/W
		Software controlled usage to support device switching.	



ATS Capability

ATS_CAP_0_2_0_PCI - ATS Capability			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000020		
Size (in bits):	16		
Address:	00204h		
ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ATS specification.			
DWord	Bit	Description	
0	15:6	RESERVED	
		Access:	RO
		Reserved	
		Value	Name
		000b	[Default]
	5	Page Aligned Request	
		Default Value:	1b
		Access:	RO
		Hardwired to 1, the Untranslated Address is always aligned to a 4096 byte boundary. Processor Graphics reports value of 1b indicating all VT-d and SVM translations are page-aligned.	
	4:0	Invalidate Queue Depth	
		Default Value:	00000b
		Access:	RO
The number of Invalidate Requests that the endpoint can accept before putting back pressure on the upstream connection. Hardwired to 0h, the function can accept 32 Invalidate Requests.			



ATS Control

ATS_CTRL_0_2_0_PCI - ATS Control		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	16	
Address:	00206h	
DWord	Bit	Description
0	15	ATS Enable
		Default Value:
		0b
		Access:
		R/W
		When Set, the function is enabled to cache translations. Processor graphics ignores this field, as GT uses GTLB as IOTLB and only pretends to software that it has a Device-TLB. Software is expected to Set this field before configuring extended context-entry for Device2 with Page Request Enable field Set. For compatibility, this field is implemented as RW as software can read it to determine ATS enable status.
	14:5	RESERVED
		Default Value:
		000b
		Access:
		RO
		Reserved
	4:0	Smallest Translation Unit
		Default Value:
		00000b
		Access:
		R/W
		This value indicates to the Endpoint the minimum number of 4096-byte blocks that is indicated in a Translation Completion or Invalidate Request. This is a power of 2 multiple and the number of blocks is 2^{STU} . A value of 0 indicates one block and value 1F indicates 2^{31} blocks. For IGD this must be programmed to 0h for 4KB as smallest translation unit.



ATS Extended Capability Header

ATS_EXTCAP_0_2_0_PCI - ATS Extended Capability Header			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x3001000F		
Size (in bits):	32		
Address:	00200h		
ATS Capability reports support for Device-TLBs on Device-2, compliant to PCI Express ats specification.			
DWord	Bit	Description	
0	31:20	Next Capability Offset	
		Default Value:	001100000000b
		Access:	RO
		This is a hardwired pointer to the next item in the capabilities list. Value 300h in this field provides the offset for Page-Request Capability.	
	19:16	Version	
		Default Value:	0001b
		Access:	RO
		Hardwired to capability version 1.	
	15:0	Capability ID	
		Default Value:	0000000000001111b
		Access:	RO
		Hardwired to the ATS Extended Capability ID	



Base Data of Stolen Memory

BDSM_0_0_0_PCI - Base Data of Stolen Memory			
Register Space:	PCI: 0/0/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	000B0h		
This register contains the base address of graphics data stolen DRAM memory.			
DWord	Bit	Description	
0	31:20	Graphics Base of Stolen Memory	
		Default Value:	000000000000b
		Access:	R/W Lock
		This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI device 0 offset 50 bits 15:8) from TOLUD (PCI Device 0 offset BC bits 31:20).	
	19:1	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	0	Lock	
		Default Value:	0b
		Access:	R/W Key Lock
This bit will lock all writeable settings in this register, including itself.			



Base of GTT Stolen Memory

BGSM_0_0_0_PCI - Base of GTT Stolen Memory			
Register Space:		PCI: 0/0/0	
Source:		BSpec	
Default Value:		0x00000000	
Size (in bits):		32	
Address:		000B4h	
This register contains the base address of stolen DRAM memory for the GTT.			
DWord	Bit	Description	
0	31:20	Graphics Base of GTT Stolen Memory	
		Default Value:	000000000000b
		Access:	R/W Lock
		This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 50 bits 7:6) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).	
	19:1	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	0	Lock	
		Default Value:	0b
		Access:	R/W Key Lock
This bit will lock all writeable settings in this register, including itself.			



Batch Buffer Per Context Pointer

BB_PER_CTX_PTR - Batch Buffer Per Context Pointer	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
This register is used to program the batch buffer address to be executed between context restore and execution of ring/execution list if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within the Per Context Batch Buffer.	
Programming Notes	Source
BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be programmed for these command streamers.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
Render CS: Per Context Batch Buffer execution must not look at the MI_RS_CONTROL or Wait For Event status that are restored for the corresponding context. Ex: A context with MI_RS_CONTROL status with RS disabled doesn't stop Render CS from triggering Resource Streamer to execute Per Context Batch Buffer when "RS Enabled Batch Buffer Per Context" is set.	RenderCS
RenderCS: The following commands are not supported within a Per Context Batch Buffer:	RenderCS
Command Name	
MI_WAIT_FOR_EVENT	
MI_ARB_CHECK	
MI_RS_CONTROL	
MI_REPORT_HEAD	
MI_URB_ATOMIC_ALLOC	
MI_SUSPEND_FLUSH	
MI_TOPOLOGY_FILTER	
MI_RS_CONTEXT	
MI_SET_CONTEXT	
MI_URB_CLEAR	
MI_SEMAPHORE_WAIT (Memory Poll Mode).Note: MI_SEMAPHORE_WAIT in register poll mode is supported.	
MI_SEMAPHORE_SIGNAL	

**BB_PER_CTX_PTR - Batch Buffer Per Context Pointer**

MI_BATCH_BUFFER_START	
MI_CONDITIONAL_BATCH_BUFFER_END	
MEDIA_OBJECT_WALKER	
GPGPU_WALKER	
3DPRIMITIVE	
3DSTATE_BINDING_TABLE_POINTERS_VS	
3DSTATE_BINDING_TABLE_POINTERS_HS	
3DSTATE_BINDING_TABLE_POINTERS_DS	
3DSTATE_BINDING_TABLE_POINTERS_GS	
3DSTATE_BINDING_TABLE_POINTERS_PS	
3DSTATE_GATHER_CONSTANT_VS	
3DSTATE_GATHER_CONSTANT_GS	
3DSTATE_GATHER_CONSTANT_HS	
3DSTATE_GATHER_CONSTANT_DS	
3DSTATE_GATHER_CONSTANT_PS	
3DSTATE_DX9_CONSTANTF_VS	
3DSTATE_DX9_CONSTANTF_HS	
3DSTATE_DX9_CONSTANTF_DS	
3DSTATE_DX9_CONSTANTF_GS	
3DSTATE_DX9_CONSTANTF_PS	
3DSTATE_DX9_CONSTANTI_VS	
3DSTATE_DX9_CONSTANTI_HS	
3DSTATE_DX9_CONSTANTI_DS	
3DSTATE_DX9_CONSTANTI_GS	
3DSTATE_DX9_CONSTANTI_PS	
3DSTATE_DX9_CONSTANTB_VS	
3DSTATE_DX9_CONSTANTB_HS	
3DSTATE_DX9_CONSTANTB_DS	
3DSTATE_DX9_CONSTANTB_GS	
3DSTATE_DX9_CONSTANTB_PS	
3DSTATE_DX9_LOCAL_VALID_VS	
3DSTATE_DX9_LOCAL_VALID_DS	
3DSTATE_DX9_LOCAL_VALID_HS	
3DSTATE_DX9_LOCAL_VALID_GS	
3DSTATE_DX9_LOCAL_VALID_PS	



BB_PER_CTX_PTR - Batch Buffer Per Context Pointer

3DSTATE_DX9_GENERATE_ACTIVE_VS	
3DSTATE_DX9_GENERATE_ACTIVE_HS	
3DSTATE_DX9_GENERATE_ACTIVE_DS	
3DSTATE_DX9_GENERATE_ACTIVE_GS	
3DSTATE_DX9_GENERATE_ACTIVE_PS	
3DSTATE_BINDING_TABLE_EDIT_VS	
3DSTATE_BINDING_TABLE_EDIT_GS	
3DSTATE_BINDING_TABLE_EDIT_HS	
3DSTATE_BINDING_TABLE_EDIT_DS	
3DSTATE_BINDING_TABLE_EDIT_PS	
3DSTATE_CONSTANT_VS	
3DSTATE_CONSTANT_GS	
3DSTATE_CONSTANT_PS	
3DSTATE_CONSTANT_HS	
3DSTATE_CONSTANT_DS	
PIPECONTROL	

Workaround	Source
Workaround: [Render CS Only][Execlist Mode of Scheduling] SW must ensure arbitration is switched off while context restore is in progress for any given context. This is achieved by disabling arbitration by programming MI_ARB_ON_OFF to "Arbitration Disable" in RCS_INDIRECT_CTX buffer and by enabling back the arbitration by programming MI_ARB_ON_OFF to "Arbitration Enable" as the last command prior to MI_BATCH_END in the BB_PER_CTX_PTR buffer of every context submitted. Note that RCS_INDIRECT_CTX_OFFSET could be set to default value or any other legitimate value as per the programming notes of the register definition. Arbitration disable by programming MI_ARB_ON_OFF (Arbitration Disabled) in RCS_INDIRECT_CTX buffer. Arbitration enabled by programming MI_ARB_ON_OFF (Arbitration Enabled) as the last command prior to MI_BATCH_BUFFER_END in BB_PER_CTX_PTR buffer. Additional Note: This WA need not be applied when it is guaranteed for no preemption to occur during execution of GPGPU workload. Preemption of GPGPU workload can be avoided by Bracketing the GPGPU workload with MI_ARB_ON_OFF (Arbitration Disable) and MI_ARB_ON_OFF (Arbitration Enable) command. MI_ARB_ON_OFF is a privileged command and can only be programmed in ring buffer or in privileged batch buffer (batch buffer in GGTT memory). Pending execlist submitted must not trigger preemption of the ongoing GPGPU workload due to following reasons First context of the pending execlist submitted is not the same as the ongoing GPGPU context. Force restore bit set for the submitted pending execlist.	
Workaround:On BXT "RS enabled Batch Buffer Per Context" can be programmed with MI_SEMAPHORE_WAIT command in register poll mode. Resource streamer stops executing the "RS enabled Batch Buffer Per Context" on encountering MI_SEMAPHORE_WAIT command. SW must ensure all the commands meant to be executed by Resource Streamer from "RS enabled Batch Buffer Per Context" must be programmed prior to programming the MI_SEMAPHORE_WAIT	RenderCS

**BB_PER_CTX_PTR - Batch Buffer Per Context Pointer**

command.			
DWord	Bit	Description	
0	31:12	Batch Buffer Per Context Address	
		Format:	U20
	Pointer to the Context in memory to be executed as a batch.		
	11:3	Reserved	
		Format:	MBZ
	2	Reserved	
	1	RS Enabled Batch Buffer Per Context	
		Format:	U1
		If set, the command stream will enable the RS to parse commands.	
		Programming Notes	
This must be set when programming the resource streamer pool commands (3DSTATE_BINDING_TABLE_POOL_ALLOC, 3DSTATE_GATHER_POOL_ALLOC, and 3DSTATE_DX9_CONSTANT_BUFFER_POOL_ALLOC) in order for the pool alloc fields to be valid in both the render engine and resource streamer.			
0	Batch Buffer Per Context Valid		
	Format:	U1	
If set, the command stream will execute the context from the Batch Buffer Per Context Address prior to the execution of actual submitted workloads.			



BLC_PWM_CTL

BLC_PWM_CTL								
Register Space:	MMIO: 0/2/0							
Source:	BSpec							
Default Value:	0x00000000							
Access:	R/W							
Size (in bits):	32							
Address:	C8250h-C8253h							
Name:	Backlight 1 PWM Control							
ShortName:	BLC_PWM_CTL_1							
Power:	PG0							
Reset:	soft							
Address:	C8350h-C8353h							
Name:	Backlight 2 PWM Control							
ShortName:	BLC_PWM_CTL_2							
Power:	PG0							
Reset:	soft							
DWord	Bit	Description						
0	31	PWM Enable This bit enables the PWM. A disabled PWM will drive 0, which can be inverted to 1 with the polarity control.						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Disable</td></tr><tr><td>1b</td><td>Enable</td></tr></table>	Value	Name	0b	Disable	1b	Enable
		Value	Name					
		0b	Disable					
	1b	Enable						
	30	Reserved Format: MBZ						
	29	PWM Polarity This field controls the polarity of the PWM signal.						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Active High</td></tr><tr><td>1b</td><td>Active Low</td></tr></table>	Value	Name	0b	Active High	1b	Active Low
		Value	Name					
		0b	Active High					
	1b	Active Low						
28:0	Reserved Format: MBZ							



BLC_PWM_DUTY

BLC_PWM_DUTY				
Register Space:	MMIO: 0/2/0			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	C8258h-C825Bh			
Name:	Backlight 1 PWM Duty Cycle			
ShortName:	BLC_PWM_DUTY_1			
Power:	PG0			
Reset:	soft			
Address:	C8358h-C835Bh			
Name:	Backlight 2 PWM Duty Cycle			
ShortName:	BLC_PWM_DUTY_2			
Power:	PG0			
Reset:	soft			
DWord	Bit	Description		
0	31:0	Duty Cycle This field controls the active portion of the backlight PWM duty cycle. The value should be programmed to (BLC_PWM_FREQ Frequency * desired duty cycle percentage / 100). A value of zero will give a 0% active duty cycle. A value equal to BLC_PWM_FREQ Frequency will give a 100% active duty cycle. When written, the new value will take affect at the end of the current PWM cycle. <table><tr><th>Restriction</th></tr><tr><td>Restriction: This should never be larger than BLC_PWM_FREQ Frequency.</td></tr></table>	Restriction	Restriction: This should never be larger than BLC_PWM_FREQ Frequency.
Restriction				
Restriction: This should never be larger than BLC_PWM_FREQ Frequency.				



BLC_PWM_FREQ

BLC_PWM_FREQ		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	C8254h-C8257h	
Name:	Backlight 1 PWM Frequency	
ShortName:	BLC_PWM_FREQ_1	
Power:	PG0	
Reset:	soft	
Address:	C8354h-C8357h	
Name:	Backlight 2 PWM Frequency	
ShortName:	BLC_PWM_FREQ_2	
Power:	PG0	
Reset:	soft	
DWord	Bit	Description
0	31:0	Frequency This field controls the backlight PWM frequency. The value should be programmed to (PWM clock frequency / desired PWM frequency). The Backlight page gives the PWM clock frequency.



Blitter MOCS Register0

BLT_MOCS_0 - Blitter MOCS Register0			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000030	
Size (in bits):		32	
Address:		0CC00h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_0 - Blitter MOCS Register0

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register1

BLT_MOCS_1 - Blitter MOCS Register1			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000034		
Size (in bits):	32		
Address:	0CC04h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_1 - Blitter MOCS Register1

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register2

BLT_MOCS_2 - Blitter MOCS Register2			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000038	
Size (in bits):		32	
Address:		0CC08h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_2 - Blitter MOCS Register2

BLT_MOCS_2 - Blitter MOCS Register2			
	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
1:0	LLC/eDRAM cacheability control		
	Default Value:	00b	
	Access:	R/W	
	Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)		



Blitter MOCS Register3

BLT_MOCS_3 - Blitter MOCS Register3			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000031	
Size (in bits):		32	
Address:		0CC0Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_3 - Blitter MOCS Register3

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	01b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register4

BLT_MOCS_4 - Blitter MOCS Register4			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0CC10h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_4 - Blitter MOCS Register4

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register5

BLT_MOCS_5 - Blitter MOCS Register5			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CC14h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_5 - Blitter MOCS Register5

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register6

BLT_MOCS_6 - Blitter MOCS Register6			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CC18h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_6 - Blitter MOCS Register6

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register7

LT_MOCS_7 - Blitter MOCS Register7			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CC1Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



LT_MOCS_7 - Blitter MOCS Register7

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register8

BLT_MOCS_8 - Blitter MOCS Register8			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000037	
Size (in bits):		32	
Address:		0CC20h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_8 - Blitter MOCS Register8

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register9

BLT_MOCS_9 - Blitter MOCS Register9			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CC24h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_9 - Blitter MOCS Register9

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register10

BLT_MOCS_10 - Blitter MOCS Register10			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0CC28h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_10 - Blitter MOCS Register10

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register11

BLT_MOCS_11 - Blitter MOCS Register11			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0CC2Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_11 - Blitter MOCS Register11

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register12

BLT_MOCS_12 - Blitter MOCS Register12			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CC30h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_12 - Blitter MOCS Register12

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register13

BLT_MOCS_13 - Blitter MOCS Register13			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000033		
Size (in bits):	32		
Address:	0CC34h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_13 - Blitter MOCS Register13

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register14

BLT_MOCS_14 - Blitter MOCS Register14			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0CC38h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_14 - Blitter MOCS Register14

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register15

BLT_MOCS_15 - Blitter MOCS Register15			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003B		
Size (in bits):	32		
Address:	0CC3Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_15 - Blitter MOCS Register15

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register16

BLT_MOCS_16 - Blitter MOCS Register16			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000030		
Size (in bits):	32		
Address:	0CC40h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_16 - Blitter MOCS Register16

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register17

BLT_MOCS_17 - Blitter MOCS Register17			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000034		
Size (in bits):	32		
Address:	0CC44h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_17 - Blitter MOCS Register17

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register18

BLT_MOCS_18 - Blitter MOCS Register18			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000038		
Size (in bits):	32		
Address:	0CC48h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_18 - Blitter MOCS Register18

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register19

BLT_MOCS_19 - Blitter MOCS Register19			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000031		
Size (in bits):	32		
Address:	0CC4Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_19 - Blitter MOCS Register19

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	01b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register20

BLT_MOCS_20 - Blitter MOCS Register20			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0CC50h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_20 - Blitter MOCS Register20

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register21

BLT_MOCS_21 - Blitter MOCS Register21			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0CC54h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_21 - Blitter MOCS Register21

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register22

BLT_MOCS_22 - Blitter MOCS Register22			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CC58h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_22 - Blitter MOCS Register22

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register23

BLT_MOCS_23 - Blitter MOCS Register23			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CC5Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_23 - Blitter MOCS Register23

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register24

BLT_MOCS_24 - Blitter MOCS Register24			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0CC60h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_24 - Blitter MOCS Register24

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register25

BLT_MOCS_25 - Blitter MOCS Register25			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003B		
Size (in bits):	32		
Address:	0CC64h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_25 - Blitter MOCS Register25

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register26

BLT_MOCS_26 - Blitter MOCS Register26			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0CC68h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_26 - Blitter MOCS Register26

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register27

BLT_MOCS_27 - Blitter MOCS Register27			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CC6Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_27 - Blitter MOCS Register27

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register28

BLT_MOCS_28 - Blitter MOCS Register28			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CC70h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_28 - Blitter MOCS Register28

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register29

BLT_MOCS_29 - Blitter MOCS Register29			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000033		
Size (in bits):	32		
Address:	0CC74h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_29 - Blitter MOCS Register29

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register30

BLT_MOCS_30 - Blitter MOCS Register30			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000037	
Size (in bits):		32	
Address:		0CC78h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_30 - Blitter MOCS Register30

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register31

BLT_MOCS_31 - Blitter MOCS Register31			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003B		
Size (in bits):	32		
Address:	0CC7Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_31 - Blitter MOCS Register31

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register32

BLT_MOCS_32 - Blitter MOCS Register32			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000030	
Size (in bits):		32	
Address:		0CC80h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_32 - Blitter MOCS Register32

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register33

BLT_MOCS_33 - Blitter MOCS Register33			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000034		
Size (in bits):	32		
Address:	0CC84h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_33 - Blitter MOCS Register33

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register34

BLT_MOCS_34 - Blitter MOCS Register34			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000038	
Size (in bits):		32	
Address:		0CC88h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_34 - Blitter MOCS Register34

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register35

BLT_MOCS_35 - Blitter MOCS Register35			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000031		
Size (in bits):	32		
Address:	0CC8Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_35 - Blitter MOCS Register35

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	01b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register36

BLT_MOCS_36 - Blitter MOCS Register36			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0CC90h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_36 - Blitter MOCS Register36

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register37

BLT_MOCS_37 - Blitter MOCS Register37			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0CC94h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_37 - Blitter MOCS Register37

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register38

BLT_MOCS_38 - Blitter MOCS Register38			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0CC98h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_38 - Blitter MOCS Register38

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register39

BLT_MOCS_39 - Blitter MOCS Register39			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CC9Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_39 - Blitter MOCS Register39

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register40

BLT_MOCS_40 - Blitter MOCS Register40			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0CCA0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_40 - Blitter MOCS Register40

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register41

BLT_MOCS_41 - Blitter MOCS Register41			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CCA4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_41 - Blitter MOCS Register41

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register42

BLT_MOCS_42 - Blitter MOCS Register42			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0CCA8h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_42 - Blitter MOCS Register42

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register43

BLT_MOCS_43 - Blitter MOCS Register43			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CCACH	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_43 - Blitter MOCS Register43

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register44

BLT_MOCS_44 - Blitter MOCS Register44			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CCB0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_44 - Blitter MOCS Register44

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register45

BLT_MOCS_45 - Blitter MOCS Register45			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000033		
Size (in bits):	32		
Address:	0CCB4h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_45 - Blitter MOCS Register45

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register46

BLT_MOCS_46 - Blitter MOCS Register46			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0CCB8h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_46 - Blitter MOCS Register46

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register47

BLT_MOCS_47 - Blitter MOCS Register47			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003B		
Size (in bits):	32		
Address:	0CCBCh		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_47 - Blitter MOCS Register47

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register48

BLT_MOCS_48 - Blitter MOCS Register48			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000030		
Size (in bits):	32		
Address:	0CCC0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_48 - Blitter MOCS Register48

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register49

BLT_MOCS_49 - Blitter MOCS Register49			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000034		
Size (in bits):	32		
Address:	0CCC4h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_49 - Blitter MOCS Register49

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register50

BLT_MOCS_50 - Blitter MOCS Register50			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000038	
Size (in bits):		32	
Address:		0CCC8h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_50 - Blitter MOCS Register50

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register51

BLT_MOCS_51 - Blitter MOCS Register51			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000031	
Size (in bits):		32	
Address:		0CCCCCh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_51 - Blitter MOCS Register51

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	01b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register52

BLT_MOCS_52 - Blitter MOCS Register52			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0CCD0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_52 - Blitter MOCS Register52

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register53

BLT_MOCS_53 - Blitter MOCS Register53			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0CCD4h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_53 - Blitter MOCS Register53

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register54

BLT_MOCS_54 - Blitter MOCS Register54			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0CCD8h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_54 - Blitter MOCS Register54

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register55

BLT_MOCS_55 - Blitter MOCS Register55			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000033		
Size (in bits):	32		
Address:	0CCDCh		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_55 - Blitter MOCS Register55

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register56

BLT_MOCS_56 - Blitter MOCS Register56			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0CCE0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_56 - Blitter MOCS Register56

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register57

BLT_MOCS_57 - Blitter MOCS Register57			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CCE4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_57 - Blitter MOCS Register57

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register58

BLT_MOCS_58 - Blitter MOCS Register58			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0CCE8h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_58 - Blitter MOCS Register58

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register59

BLT_MOCS_59 - Blitter MOCS Register59			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CCECh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_59 - Blitter MOCS Register59

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register60

BLT_MOCS_60 - Blitter MOCS Register60			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CCF0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_60 - Blitter MOCS Register60

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register61

BLT_MOCS_61 - Blitter MOCS Register61			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CCF4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_61 - Blitter MOCS Register61

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register62

BLT_MOCS_62 - Blitter MOCS Register62			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0CCF8h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_62 - Blitter MOCS Register62

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Blitter MOCS Register63

BLT_MOCS_63 - Blitter MOCS Register63			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CCFCh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



BLT_MOCS_63 - Blitter MOCS Register63

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Built In Self Test

BIST_0_2_0_PCI - Built In Self Test			
Register Space:		PCI: 0/2/0	
Source:		BSpec	
Default Value:		0x00000000	
Size (in bits):		8	
Address:		0000Fh	
This register is used for control and status of Built In Self Test (BIST).			
DWord	Bit	Description	
0	7	BIST Supported	
		Default Value:	0b
		Access:	RO
		BIST is not supported. This bit is hardwired to 0.	
	6:0	Reserved	
		Default Value:	0000000b
		Access:	RO
		Reserved	



Cache Line Size

CLS_0_2_0_PCI - Cache Line Size		
Register Space: PCI: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 8		
Address: 0000Ch		
DWord	Bit	Description
0	7:0	Cache Line Size Value
		Default Value: 00000000b
		Access: R/W
		This field is implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no effect on any PCI Express device behavior.



Capabilities Control

CAPCTRL0_0_2_0_PCI - Capabilities Control		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x0000010C	
Size (in bits):	16	
Address:	00042h	
DWord	Bit	Description
0	15:12	Reserved
		Default Value: 0000000b
		Access: RO
		Reserved
	11:8	CAPID Version
		Default Value: 0001b
		Access: RO
		This field is hardwired to the value 1h to identify the first revision of the CAPID register definition.
	7:0	CAPID Length
		Default Value: 00001100b
		Access: RO
		This field is hardwired to the value 0Ch to indicate the structure length (12 bytes).



Capabilities Pointer

CAPPOINT_0_2_0_PCI - Capabilities Pointer			
Register Space: PCI: 0/2/0			
Source: BSpec			
Default Value: 0x00000040			
Size (in bits): 8			
Address: 00034h			
This register points to a linked list of capabilities implemented by this device.			
DWord	Bit	Description	
0	7:0	Capabilities Pointer Value	
		Default Value:	01000000b
		Access:	RO
		This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the CAPID0 register at offset 40h.	



Capability Identifier

CAPID0_0_2_0_PCI - Capability Identifier		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00007009	
Size (in bits):	16	
Address:	00040h	
DWord	Bit	Description
0	15:8	Next Capability Pointer
		Default Value: 01110000b
		Access: RO
		This field is hardwired to point to the next PCI Capability structure, the PCIe Capabilities structure at 70h.
	7:0	Capability Identifier
		Default Value: 00001001b
		Access: RO
		This field is hardwired to the value 09h to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.



CDCLK_CTL

CDCLK_CTL				
Register Space:	MMIO: 0/2/0			
Source:	BSpec			
Default Value:	0x000002A1			
Access:	R/W			
Size (in bits):	32			
Address:	46000h-46003h			
Name:	CD Clock Control			
ShortName:	CDCLK_CTL			
Power:	PG0			
Reset:	global			
This register is not reset by the device 2 FLR.				
Restriction				
Restriction : These fields should only be changed as part of the Display Sequences for Changing CD Clock Frequency.				
DWord	Bit	Description		
0	31:24	Reserved		
		Format: MBZ		
	23:22	DE CD2X Divider Select		
		Access: Double Buffered		
		Double Buffer Update Point: Pipe off or start of vertical blank		
		This field selects how the DE PLL CD2X clock output is divided before driving the display CD2X clock.		
		This field is double buffered to align with the pipe from DE CD2X Pipe Select. It will update at the start of vertical blank of the selected pipe, or immediately if the selected pipe is disabled or no pipe is selected.		
		Value	Name	Description
		00b	Divide by 1	If DE PLL output is 1248 MHz: CD2X 1248 MHz, CD 624 MHz. If DE PLL output is 1152 MHz: CD2X 1152 MHz, CD 576 MHz. DE PLL CD2X output must be configured to 1152 MHz or 1248 MHz when using this divider.
		01b	Divide by 1.5	CD2X 768 MHz, CD 384 MHz DE PLL CD2X output must be configured to 1152 MHz when using this divider.
10b	Divide by 2	CD2X 576 MHz, CD 288 MHz DE PLL CD2X output must be configured to 1152 MHz when using this divider.		



CDCLK_CTL			
		11b	Divide by 4 CD2X 288 MHz, CD 144 MHz DE PLL CD2X output must be configured to 1152 MHz when using this divider.
		Restriction Restriction : DE CD2X Divider Select must not be changed while more than one pipe is enabled. When one pipe is enabled, the DE CD2X Pipe Select must be set to that pipe before changing DE CD2X Divider Select.	
	21:20	DE CD2X Pipe Select This field selects the pipe enable and vertical blank to be used for double buffering the DE CD2X Divider Select and SSA Precharge Enable.	
		Value	Name Description
		00b	Pipe A
		01b	Pipe B
		10b	Pipe C
		11b	None Double buffer enable is tied to 1 so that writes to the DE CD2X Divider Select and SSA Precharge Enable will take effect immediately.
	19	Reserved	
	18	Reserved	
	17	Reserved	
		Format:	MBZ
	16	SSA Precharge Enable	
		Access:	Double Buffered
		Double Buffer Update Point:	Pipe off or start of vertical blank
		This field enables the Low Speed Small Signal Array Pre-charge. This field is double buffered to align with the pipe from DE CD2X Pipe Select. It will update at the start of vertical blank of the selected pipe, or immediately if the selected pipe is disabled or no pipe is selected.	
		Value	Name
		0b	Disable
		1b	Enable
		Restriction	



CDCLK_CTL		
		Restriction : This field must be disabled when CD clock frequency is < 500 MHz and enabled when CD clock frequency is >= 500 MHz. This field must not be changed while more than one pipe is enabled. When one pipe is enabled, the DE CD2X Pipe Select must be set to that pipe before changing DE CD2X Divider Select.
15:11	Reserved	
	Format:	MBZ
10:0	CD Frequency Decimal	
	Format:	U10.1
	This field selects the decimal value of the frequency for CD clock, which is used to generate divided down clocks for some display engine timers. This value is represented in a 10.1 format with 10 integer bits and 1 fractional bit. Program this field to select the pre-defined value that matches the CD frequency chosen by the DE PLL and CD2X Divider. If no value is defined, program this field with the CD frequency, rounded to the closest 0.5, then minus one.	
	Value	Name
	00 1000 1111 0b	144 MHz CD
	01 0001 1111 0b	288 MHz CD
	01 0111 1111 0b	384 MHz CD
	10 0011 1111 0b	576 MHz CD
	10 0110 1111 0b	624 MHz CD
	01 0101 0000 1b	337.5 MHz CD [Default]



Class Code

CC_0_2_0_PCI - Class Code			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00030000		
Size (in bits):	24		
Address:	00009h		
This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.			
DWord	Bit	Description	
0	23:16	Base Class Code	
		Default Value:	00000011b
		Access:	RO Variant
		This is an 8-bit value that indicates the base class code. When MGGC0[VAMEN] is 0 this code has the value 03h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this code has the value 04h, indicating a Multimedia Device.	
	15:8	Sub-Class Code	
		Default Value:	00000000b
		Access:	RO Variant
		When MGGC0[VAMEN] is 0 this value will be determined based on Device 0 GGC register, GMS and IVD fields. 00h: VGA compatible 80h: Non VGA (GMS = "00h" or IVD = "1b") When MGGC0[VAMEN] is 1, this value is 80h, indicating other multimedia device.	
	7:0	Programming Interface	
		Default Value:	00000000b
		Access:	RO
		When MGGC0[VAMEN] is 0 this value is 00h, indicating a Display Controller. When MGGC0[VAMEN] is 1 this value is 00h, indicating a NOP.	



Configuration Register1 for RPMunit

CONFIG1 - Configuration Register1 for RPMunit					
Register Space:		MMIO: 0/2/0			
Default Value:		0x0000001E			
Size (in bits):		32			
Address:		00D04h			
Lock bit LOCK applies to all RW/L fields in this register. Lock is overridden during context restore.					
DWord	Bit	Description			
0	31	Lock for RW/L Fields in this Register			
		<table><tr><td>Access:</td><td>R/W Lock</td></tr></table> 0 = Bits of CONFIG0 register are R/W. 1 = All bits of CONFIG0 register are RO (including this lock bit). Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). Lock is reset on a restore after context is captured.	Access:	R/W Lock	
	Access:	R/W Lock			
	30:9	Placeholder Bits BF			
		<table><tr><td>Access:</td><td>R/W Lock</td></tr></table> Placeholder bits for implementation or ECO loops.	Access:	R/W Lock	
Access:	R/W Lock				
8:0	RCP L3 FREQ DETECT				
	<table><tr><td>Default Value:</td><td>000011110b</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> This is control signal needed from clock unit that can be set at 1 when 2X clock frequency is less than or equal to 1GHz. It needs to be at 0 when 2X clock frequency is >1GHz. Without this circuit changes, the GT L3 cache will not be functional at lower frequency due to Vcc is less than Vccmin of 0.9V for the array. default value: low2xthresh=0x01Eh corresponding to a 1x frequency of 500Mhz.	Default Value:	000011110b	Access:	R/W Lock
Default Value:	000011110b				
Access:	R/W Lock				



DC_STATE_EN

DC_STATE_EN			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	45504h-45507h		
Name:	Display C State Enable		
ShortName:	DC_STATE_EN		
Power:	PG0		
Reset:	global		
DWord	Bit	Description	
0	31:10	Reserved	
	9	In CSR Flow	
		Value	Name
		0b	Not In CSR
		1b	In CSR
		Restriction	
		Restriction : This field is used for hardware communication. Software must not change this field.	
	8	Block Outbound Traffic	
		Access is read/write, but hardware can also clear the value based on the PM Request.	
		Value	Name
		0b	Do Not Block
		1b	Block
		Restriction	
	Restriction : This field is used for hardware communication. Software must not change this field.		
7:5	Reserved		



DC_STATE_EN									
4	Mask Poke This field masks the poke signal that would otherwise be generated by a write to the DC_STATE_SEL register.								
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Unmask</td></tr><tr><td>1b</td><td>Mask</td></tr></table>	Value	Name	0b	Unmask	1b	Mask		
	Value	Name							
	0b	Unmask							
	1b	Mask							
<table><tr><th>Restriction</th></tr><tr><td>Restriction : This field is used for hardware communication. Software must not change this field.</td></tr></table>	Restriction	Restriction : This field is used for hardware communication. Software must not change this field.							
Restriction									
Restriction : This field is used for hardware communication. Software must not change this field.									
3	DC9 Allow This field indicates software allows Display C9. When allowed, the PCU can save the display PCI Config context and power down display								
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Do not allow</td></tr><tr><td>1b</td><td>Allow</td></tr></table>	Value	Name	0b	Do not allow	1b	Allow		
	Value	Name							
	0b	Do not allow							
1b	Allow								
2	Reserved								
1:0	Dynamic DC State Enable This field enables hardware to dynamically enter and exit Display C states.								
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>00b</td><td>Disable</td></tr><tr><td>01b</td><td>Enable up to DC5</td></tr><tr><td>10b</td><td>Enable up to DC6</td></tr></table>	Value	Name	00b	Disable	01b	Enable up to DC5	10b	Enable up to DC6
	Value	Name							
	00b	Disable							
	01b	Enable up to DC5							
	10b	Enable up to DC6							
<table><tr><th>Restriction</th></tr><tr><td>Restriction : The Display CSR code must be loaded before this field is enabled.</td></tr></table>	Restriction	Restriction : The Display CSR code must be loaded before this field is enabled.							
Restriction									
Restriction : The Display CSR code must be loaded before this field is enabled.									



DDI_BUF_CTL

DDI_BUF_CTL		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	64000h-64003h	
Name:	DDI A Buffer Control	
ShortName:	DDI_BUF_CTL_A	
Power:	PG1	
Reset:	soft	
Address:	64100h-64103h	
Name:	DDI B Buffer Control	
ShortName:	DDI_BUF_CTL_B	
Power:	PG1	
Reset:	soft	
Address:	64200h-64203h	
Name:	DDI C Buffer Control	
ShortName:	DDI_BUF_CTL_C	
Power:	PG1	
Reset:	soft	
Address:	64300h-64303h	
Name:	DDI D Buffer Control	
ShortName:	DDI_BUF_CTL_D	
Power:	PG1	
Reset:	soft	
Address:	64400h-64403h	
Name:	DDI E Buffer Control	
ShortName:	DDI_BUF_CTL_E	
Power:	PG1	
Reset:	soft	
Do not read or write the register when the associated power well is disabled.		
DWord	Bit	Description
0	31	DDI Buffer Enable This bit enables the DDI buffer.



DDI_BUF_CTL														
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Disable</td></tr><tr><td>1b</td><td>Enable</td></tr></table>	Value	Name	0b	Disable	1b	Enable							
Value	Name													
0b	Disable													
1b	Enable													
30	Reserved													
	Format:	MBZ												
29:28	Reserved													
27:24	DP Vswing Emp Sel													
	<table><tr><th colspan="3">Description</th></tr><tr><td colspan="3">This field is ignored on Broxton. Voltage swing and emphasis programming is done through the PHY registers.</td></tr><tr><td colspan="3">These bits are used to select the voltage swing and emphasis for DisplayPort.</td></tr><tr><td colspan="3">This field is ignored for HDMI and DVI. The values programmed in DDI_BUF_TRANS determine the voltage swing and emphasis for each selection.</td></tr></table>		Description			This field is ignored on Broxton. Voltage swing and emphasis programming is done through the PHY registers.			These bits are used to select the voltage swing and emphasis for DisplayPort.			This field is ignored for HDMI and DVI. The values programmed in DDI_BUF_TRANS determine the voltage swing and emphasis for each selection.		
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These bits are used to select the voltage swing and emphasis for DisplayPort.														
This field is ignored for HDMI and DVI. The values programmed in DDI_BUF_TRANS determine the voltage swing and emphasis for each selection.														
	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0000b-1000b</td><td>Select 0 - Select 8</td><td>Select from buffer translations 0 through 8. Valid with all DDIs.</td></tr><tr><td>1001b</td><td>Select 9</td><td>Select buffer translation 9. Valid only with DDIA and DDIE.</td></tr></table>	Value	Name	Description	0000b-1000b	Select 0 - Select 8	Select from buffer translations 0 through 8. Valid with all DDIs.	1001b	Select 9	Select buffer translation 9. Valid only with DDIA and DDIE.				
Value	Name	Description												
0000b-1000b	Select 0 - Select 8	Select from buffer translations 0 through 8. Valid with all DDIs.												
1001b	Select 9	Select buffer translation 9. Valid only with DDIA and DDIE.												
23:17	Reserved													
	Format:	MBZ												
16	Port Reversal													
	This field enables lane reversal within the port. Lane reversal swaps the data on the lanes as they are output from the port.													
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Not reversed</td></tr><tr><td>1b</td><td>Reversed</td></tr></table>	Value	Name	0b	Not reversed	1b	Reversed							
Value	Name													
0b	Not reversed													
1b	Reversed													
	<table><tr><th>Programming Notes</th></tr><tr><td>DDI B, C, D, and F reversal always swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2. If DDIA Lane Capability Control selects DDIA x2, then DDI A reversal swaps the two lanes, so lane 0 is swapped with lane 1. If DDIA Lane Capability Control selects DDIA x4, then DDI A reversal swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2.</td></tr></table>		Programming Notes	DDI B, C, D, and F reversal always swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2. If DDIA Lane Capability Control selects DDIA x2, then DDI A reversal swaps the two lanes, so lane 0 is swapped with lane 1. If DDIA Lane Capability Control selects DDIA x4, then DDI A reversal swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2.										
Programming Notes														
DDI B, C, D, and F reversal always swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2. If DDIA Lane Capability Control selects DDIA x2, then DDI A reversal swaps the two lanes, so lane 0 is swapped with lane 1. If DDIA Lane Capability Control selects DDIA x4, then DDI A reversal swaps the four lanes, so lane 0 is swapped with lane 3, and lane 1 is swapped with lane 2.														
	<table><tr><th>Restriction</th></tr><tr><td>Restriction : This field must not be changed while the DDI is enabled. DDI E does not support reversal.</td></tr></table>		Restriction	Restriction : This field must not be changed while the DDI is enabled. DDI E does not support reversal.										
Restriction														
Restriction : This field must not be changed while the DDI is enabled. DDI E does not support reversal.														



DDI_BUF_CTL			
	15:8	Reserved	
		Format:	MBZ
	7	DDI Idle Status	
		Access:	RO
		This bit indicates when the DDI buffer is idle.	
		Value	Name
		0b	Buffer Not Idle
		1b	Buffer Idle
		Restriction	
		Restriction : On BXT this status can be incorrect. Follow the fixed delay in the mode set sequence instead of using this field.	
	6:5	Reserved	
		Format:	MBZ
	4	DDIA Lane Capability Control	
		This bit selects how lanes are shared between DDI A and DDI E.	
		This field is only used in the DDI A instance of this register.	
		See the DDI A and DDI E lane mapping table in the Introduction section.	
		Value	Name
		0b	DDIA x2
		1b	DDIA x4
		Restriction	
	3:1	DP Port Width Selection	
		Description	
		This bit selects the number of lanes to be enabled on the DDI link for DisplayPort.	
		Value	Name
		000b	x1
		001b	x2
		011b	x4
		Others	Reserved
		Programming Notes	



DDI_BUF_CTL									
		DDI E only supports x1 and x2 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x2, otherwise DDI E is not supported. DDI A (EDP) supports x1, x2, and x4 when DDI_BUF_CTL_A DDIA Lane Capability Control is set to DDIA x4, otherwise DDI A only supports x1 and x2.							
		Restriction							
		Restriction : When in DisplayPort mode the value selected here must match the value selected in TRANS_DDI_FUNC_CTL attached to this DDI.							
	0	Restriction : This field must not be changed while the DDI is enabled.							
		Init Display Detected							
		Access: RO							
		Description							
		Strap indicating whether a display was detected on this port during initialization. It signifies the level of the port detect pin at boot. This bit is only informative. It does not prevent this port from being enabled in hardware. This field only indicates the DDIA detection. Detection for other ports is read from SFUSE_STRAP.							
		There are no port presence straps on Broxton. Software should use alternate means to determine port presence.							
		<table> <tr> <th>Value</th><th>Name</th><th>Description</th></tr> <tr> <td>0b</td><td>Not Detected</td><td>Digital display not detected during initialization</td></tr> <tr> <td>1b</td><td>Detected</td><td>Digital display detected during initialization</td></tr> </table>	Value	Name	Description	0b	Not Detected	Digital display not detected during initialization	1b
Value	Name	Description							
0b	Not Detected	Digital display not detected during initialization							
1b	Detected	Digital display detected during initialization							



DE_PIPE_INTERRUPT

DE_PIPE_INTERRUPT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44400h-4440Fh	
Name:	Display Engine Pipe A Interrupts	
ShortName:	DE_PIPE_INTERRUPT_A	
Power:	PG1	
Reset:	soft	
Address:	44410h-4441Fh	
Name:	Display Engine Pipe B Interrupts	
ShortName:	DE_PIPE_INTERRUPT_B	
Power:	PG2	
Reset:	soft	
Address:	44420h-4442Fh	
Name:	Display Engine Pipe C Interrupts	
ShortName:	DE_PIPE_INTERRUPT_C	
Power:	PG2	
Reset:	soft	
Description		
This table indicates which events are mapped to each bit of the Display Engine Pipe Interrupt registers. The IER enabled Display Engine Pipe Interrupt IIR (sticky) bits are ORed together to generate the DE_Pipe Interrupts Pending bit in the Master Interrupt Control register. There is one full set of Display Engine Pipe interrupts per display pipes A/B/C. The STEREO3D_EVENT_MASK selects between left eye and right eye reporting of vertical blank, vertical sync, and scanline events in stereo 3D modes.		
0x44400 = ISR A, 0x44410 = ISR B, 0x44420 = ISR C 0x44404 = IMR A, 0x44414 = IMR B, 0x44424 = IMR C 0x44408 = IIR A, 0x44418 = IIR B, 0x44428 = IIR C 0x4440C = IER A, 0x4441C = IER B, 0x4442C = IER C		
DWord	Bit	Description
0	31	Underrun The ISR is an active high pulse when there is an underrun on the transcoder attached to this pipe.
	30	Unused_Int_30 These interrupts are currently unused.



DE_PIPE_INTERRUPT

DE_PIPE_INTERRUPT				
	29	Reserved		
	28	Reserved		
	27:20	Unused_Int_27_20 These interrupts are currently unused.		
	19	Reserved		
	18	Reserved		
	17	Reserved		
	16	Reserved		
	15:13	Unused_Int_15_13 These interrupts are currently unused.		
	12	DPST_Histogram_event The ISR is an active high pulse on the DPST Histogram event on this pipe.		
	11	Cursor_GTT_Fault_Status The ISR is an active high pulse when a GTT fault is detected for the cursor on this pipe.		
	10	Plane4_GTT_Fault_Status <table><tr><th>Description</th></tr><tr><td>The ISR is an active high pulse when a GTT fault is detected for plane 4 on this pipe. Not all pipes a have plane 4.</td></tr></table>	Description	The ISR is an active high pulse when a GTT fault is detected for plane 4 on this pipe. Not all pipes a have plane 4.
	Description			
	The ISR is an active high pulse when a GTT fault is detected for plane 4 on this pipe. Not all pipes a have plane 4.			
	9	Plane3_GTT_Fault_Status <table><tr><th>Description</th></tr><tr><td>The ISR is an active high pulse when a GTT fault is detected for plane 3 on this pipe. Not all pipes a have plane 3.</td></tr></table>	Description	The ISR is an active high pulse when a GTT fault is detected for plane 3 on this pipe. Not all pipes a have plane 3.
	Description			
	The ISR is an active high pulse when a GTT fault is detected for plane 3 on this pipe. Not all pipes a have plane 3.			
8	Plane2_GTT_Fault_Status The ISR is an active high pulse when a GTT fault is detected for plane 2 on this pipe.			
7	Plane1_GTT_Fault_Status The ISR is an active high pulse when a GTT fault is detected for plane 1 on this pipe.			
6	Plane4_Flip_Done <table><tr><th>Description</th></tr><tr><td>The ISR is an active high pulse when the flip is done for plane 4 on this pipe. Not all pipes have a plane 4.</td></tr></table>	Description	The ISR is an active high pulse when the flip is done for plane 4 on this pipe. Not all pipes have a plane 4.	
Description				
The ISR is an active high pulse when the flip is done for plane 4 on this pipe. Not all pipes have a plane 4.				
5	Plane3_Flip_Done <table><tr><th>Description</th></tr><tr><td>The ISR is an active high pulse when the flip is done for plane 3 on this pipe. Not all pipes have a plane 3.</td></tr></table>	Description	The ISR is an active high pulse when the flip is done for plane 3 on this pipe. Not all pipes have a plane 3.	
Description				
The ISR is an active high pulse when the flip is done for plane 3 on this pipe. Not all pipes have a plane 3.				
4	Plane2_Flip_Done The ISR is an active high pulse when the flip is done for plane 2 on this pipe.			



DE_PIPE_INTERRUPT		
	3	Plane1_Flip_Done The ISR is an active high pulse when the flip is done for plane 1 on this pipe.
	2	Scan_Line_Event The ISR is an active high pulse on the scan line event of the transcoder attached to this pipe.
		Restriction
		Restriction : Not supported with MIPI DSI.
	1	Vsync The ISR is an active high level for the duration of the vertical sync of the transcoder attached to this pipe.
Restriction		
Restriction : Not supported with MIPI DSI.		
0	Vblank The ISR is an active high level for the duration of the vertical blank of the transcoder attached to this pipe.	



DE_PLL_CTL

DE_PLL_CTL			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000064		
Access:	R/W		
Size (in bits):	32		
Address:	6D000h-6D003h		
Name:	DE PLL Control		
ShortName:	DE_PLL_CTL		
Power:	PG0		
Reset:	global		
The register is used to control the frequency of the outputs from the DE PLL. The DE_PLL_ENABLE register controls the PLL enable.			
Restriction			
Restriction : The fields must not be changed while the PLL is enabled.			
DWord	Bit	Description	
0	31:25	Reserved	
		Format: MBZ	
	24:18	Output Ratio	
		Set the output clock ratio.	
		Restriction	
	Restriction : Display software must not change this field.		
	17:16	PVD Ratio	
		Set the post VCO divider ratio.	
		Value	Name
		00b	1
		01b	2
		10b	4
11b		8	
Restriction			
Restriction : Display software must not change this field.			
15:14	Ref Ratio		
	Set the refclk ratio.		
	Value	Name	
00b	Ref		



DE_PLL_CTL			
		01b	Ref/2
		10b	Ref/4
		11b	Ref/8
		Restriction	
		Restriction : Display software must not change this field.	
	13	Force On Force the PLL on.	
		Value	Name
		0b	No Force
		1b	Force On
		Restriction	
		Restriction : Display software must not change this field.	
	12	Force Off Force the PLL off.	
		Value	Name
		0b	No Force
		1b	Force Off
		Restriction	
		Restriction : Display software must not change this field.	
	11:10	Freq Sel C Frequency Select for DSI C clock	
		Value	Name
		00b	16X
		Non DSI	
		Restriction	
		Restriction : Display software must not change this field.	
	9:8	Freq Sel A Frequency Select for DSI A clock	
		Value	Name
		00b	16X
		Non DSI	
		Restriction	
		Restriction : Display software must not change this field.	



DE_PLL_CTL				
	7:0	PLL Ratio		
		Value	Name	Description
		3Ch	60	DE PLL 1152 MHz before post divider
		41h	65	DE PLL 1248 MHz before post divider
		21h	33	DE PLL 633.6 MHz before post divider
		64h	100 [Default]	
		Others	Reserved	



DE_PLL_ENABLE

DE_PLL_ENABLE								
Register Space:	MMIO: 0/2/0							
Source:	BSpec							
Default Value:	0x00000000							
Access:	R/W							
Size (in bits):	32							
Address:	46070h-46073h							
Name:	DE PLL Enable							
ShortName:	DE_PLL_ENABLE							
Power:	Always on							
Reset:	soft							
DWord	Bit	Description						
0	31	PLL Enable This field enables or disables the DE PLL.						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Disable</td></tr><tr><td>1b</td><td>Enable</td></tr></table>	Value	Name	0b	Disable	1b	Enable
		Value	Name					
		0b	Disable					
	1b	Enable						
	30	PLL Lock						
		Access:	RO					
		This fields indicates the status of the DE PLL Lock.						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Not locked or not enabled</td></tr><tr><td>1b</td><td>Locked</td></tr></table>	Value	Name	0b	Not locked or not enabled	1b	Locked
		Value	Name					
		0b	Not locked or not enabled					
	1b	Locked						
	29:0	Reserved						
Format:		MBZ						



DE Misc Interrupt Definition

DE Misc Interrupt Definition			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	44460h-4446Fh		
Name:	Display Engine Miscellaneous Interrupts		
ShortName:	DE_MISC_INTERRUPT		
Power:	PG0		
Reset:	soft		
This table indicates which events are mapped to each bit of the Display Engine Miscellaneous Interrupt registers. 0x44460 = ISR 0x44464 = IMR 0x44468 = IIR 0x4446C = IER			
DWord	Bit	Description	
0	31	Poison The ISR is an active high pulse on receiving the poison response to a memory transaction.	
	30	ECC_Double_Error The ISR is an active high level while any of the ECC Double Error status bits are set.	
	29	Invalid_GTT_page_table_entry The ISR is an active high pulse on receiving the iMPH invalid GTT page table entry indication.	
	28	Invalid_page_table_entry_data	Description
			The ISR is an active high pulse on receiving the iMPH invalid page table entry data indication.
			This interrupt is not supported.
	27	GSE The ISR is an active high pulse on the GSE system level event.	
	26	Camera Interrupt Event This interrupt is not supported.	
	25	Reserved	
	24	Reserved	
	23	WD0_Interrupts_Combined The ISR is an active high level while any of the WD0_IIR bits are set.	
22	SVM Device Mode PRQ Event The ISR is an active high pulse on receiving the iMPH SVM Device Mode PRQ event indication. This event indicates that a GT advanced context encountered a recoverable page fault.		



DE Misc Interrupt Definition

DE Misc Interrupt Definition				
	21	SVM Device Mode VTD Fault The ISR is an active high pulse on receiving the iMPH SVM Device Mode VT-d fault indication. This event indicates GT encountered a non-recoverable translation fault.		
	20	SVM Device Mode Wait Descriptor Completion The ISR is an active high pulse on receiving the iMPH SVM Device Mode Wait Descriptor Completion indication. This event indicates that IMPH completed Invalidation Wait Descriptor.		
	19	SRD_Interrupts_Combined The ISR is an active high level while any of the SRD_IIR bits are set.		
	18	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ
	Format:	MBZ		
	17:16	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ
	Format:	MBZ		
	15	GTC_Interrupts_Combined The ISR is an active high level while any of the GTC_IIR bits are set.		
	14:9	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ
	Format:	MBZ		
	8	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ
	Format:	MBZ		
7:4	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ	
Format:	MBZ			
3:1	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ	
Format:	MBZ			
0	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ	
Format:	MBZ			



DE Port Interrupt Definition

DE Port Interrupt Definition		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	44440h-4444Fh	
Name:	Display Engine Port Interrupts	
ShortName:	DE_PORT_INTERRUPT	
Power:	PG0	
Reset:	soft	
This table indicates which events are mapped to each bit of the Display Engine Port Interrupt registers. 0x44440 = ISR 0x44444 = IMR 0x44448 = IIR 0x4444C = IER		
DWord	Bit	Description
0	31	MIPI C The ISR is an active high level indicating an interrupt is set in MIPIC_INTR_STAT_REG or MIPIC_INTR_STAT_REG_1.
	30	MIPI A The ISR is an active high level indicating an interrupt is set in MIPIA_INTR_STAT_REG or MIPIA_INTR_STAT_REG_1.
	29	Reserved
	28	Reserved
	27	AUX Channel D The ISR is an active high pulse on the AUX DDI D done event. This event will not occur for SRD AUX done.
	26	AUX Channel C The ISR is an active high pulse on the AUX DDI C done event. This event will not occur for SRD AUX done.
	25	AUX Channel B The ISR is an active high pulse on the AUX DDI B done event. This event will not occur for SRD AUX done.
	24	MIPI C TE The ISR is an active high level indicating a TE interrupt is set in MIPIC_STATUS.
	23	MIPI A TE The ISR is an active high level indicating a TE interrupt is set in MIPIA_STATUS.
22:12	Reserved	



DE Port Interrupt Definition

	11:10	Reserved
	9:8	Reserved
	7:6	Reserved
	5	DDI C Hotplug The ISR gives the live state of the DDI HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled. This field is unused in projects that have a PCH.
	4	DDI B Hotplug The ISR gives the live state of the DDI HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled. This field is unused in projects that have a PCH.
	3	DDI A Hotplug The ISR gives the live state of the DDI HPD pin when the HPD input is enabled. The IIR is set if a short or long pulse is detected when HPD input is enabled. This field is unused in projects that have a PCH.
	2	Reserved
	1	GMBus The ISR is an active high pulse when any of the unmasked events in GMBUS4 Interrupt Mask register occur. This field is only used on projects that have GMBUS integrated into the north display. Projects that have GMBUS in the south display have the GMBUS interrupt in the south display interrupts.
	0	AUX_Channel_A The ISR is an active high pulse on the AUX DDI A done event. This event will not occur for SRD AUX done.



Device 0 Capabilities A

CAPID0_A_0_0_0_PCI - Device 0 Capabilities A		
Register Space: PCI: 0/0/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 000E4h		
DWord	Bit	Description
0	31	Display HD Audio Disable
		Default Value: 0b
		Access: R/W Key Firmware Only
		Unused - Bit field not relevant for the current project
	30	PEG12 Disable
		Default Value: 0b
		Access: R/W Key Firmware Only
		Unused - Bit field not relevant for the current project
	29	PEG11 Disable
		Default Value: 0b
		Access: R/W Key Firmware Only
		Unused - Bit field not relevant for the current project
	28	PEG10 Disable
		Default Value: 0b
		Access: R/W Key Firmware Only
		Unused - Bit field not relevant for the current project
	27	PCI Express Link Width Upconfig Disable
		Default Value: 0b
		Access: R/W Firmware Only
		Unused - Bit field not relevant for the current project
	26	DMI Width
		Default Value: 0b
		Access: R/W Firmware Only
		Unused - Bit field not relevant for the current project
	25	ECC Disable
		Default Value: 0b
		Access: R/W Firmware Only
		Unused - Bit field not relevant for the current project



CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

	24	Force DRAM ECC Enabled	Default Value:	0b
			Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project		
	23	VTd Disable	Default Value:	0b
			Access:	R/W Firmware Only
		0: Enable VTd 1: Disable VTd		
	22	DMI Gen 2 Disable	Default Value:	0b
			Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project		
	21	PEG Gen 2 Disable	Default Value:	0b
			Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project		
	20:19	DDR Size	Default Value:	00b
			Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project		
	18	Bclk overclocking disable	Default Value:	0b
			Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project		
	17	Disable 1N Mode	Default Value:	0b
			Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project		
	16	Full ULT Fuse Read Disable	Default Value:	0b
			Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project		
	15	Camarillo Device Disable	Default Value:	0b
			Access:	R/W Firmware Only
		0: DPTF (Camarillo) associated memory spaces are accessible. 1: DPTF (Camarillo) associated memory and IO spaces are disabled. DEVEN_0_0_0_PCI field for		



CAPID0_A_0_0_0_PCI - Device 0 Capabilities A

	DPTF can not be set.	
14	2 DIMMS per Channel Disable	
	Default Value:	0b
	Access:	R/W Firmware Only
	Unused - Bit field not relevant for the current project	
13	X2APIC Enabled	
	Default Value:	0b
	Access:	R/W Firmware Only
	Unused - Bit field not relevant for the current project	
12	Performance Dual Channel Disable	
	Default Value:	0b
	Access:	R/W Firmware Only
	Unused - Bit field not relevant for the current project	
11	Internal Graphics Disable	
	Default Value:	0b
	Access:	R/W Key Firmware Only
	0b: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1b: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control. Device 2 is disabled and hidden.	
10	Reserved	
9:8	Capability Device ID	
	Default Value:	00b
	Access:	R/W Firmware Only
7:4	Compatibility Rev ID	
	Default Value:	0000b
	Access:	R/W Firmware Only
	Unused - Bit field not relevant for the current project	
3	DDR Overclocking	
	Default Value:	0b
	Access:	R/W Firmware Only
	Unused - Bit field not relevant for the current project	

**CAPID0_A_0_0_0_PCI - Device 0 Capabilities A**

	2	IA Overclocking Enabled by DSKU	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	1	DDR Write VRef Enable	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	0	DDR3L Enable	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	



Device 0 Capabilities B

CAPID0_B_0_0_0_PCI - Device 0 Capabilities B			
Register Space:	PCI: 0/0/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	000E8h		
DWord	Bit	Description	
0	31	Reserved_31	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	30	IA Overclocking DSKU Control Disable	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	29	IA Overclocking Enable	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	28	SMT Capability	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
27:25	Cache Size Capability		
	Default Value:	000b	
	Access:	R/W Firmware Only	
	Unused - Bit field not relevant for the current project		
24	SVMDIS		
	Access:	R/W Firmware Only	
	Value	Name	
	0b	SVM mode enabled [Default]	
	1b	SVM mode disabled	
23:21	DDR3 Maximum Frequency Capability with 100 Memory		
	Access:	R/W Firmware Only	
	Unused - Bit field not relevant for the current project		

**CAPID0_B_0_0_0_PCI - Device 0 Capabilities B**

	20	Gen3 Disable Fuse for PCIe PEG Controllers	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	19	Package Type	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	18	Additive Graphics Enabled	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	17	Additive Graphics Capable	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	16	Primary PEG Port x16 Disable	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	15:12	Reserved_15_12	
		Default Value:	0000b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	11	Reserved	
	10:8	Reserved_10_8	
		Default Value:	000b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	7	Reserved	
	6:4	DDR3 Maximum Frequency Capability	
		Default Value:	000b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	



CAPID0_B_0_0_0_PCI - Device 0 Capabilities B

	3	Reserved_3	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	2	DDR4 DSKU Enable	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	1	Dual PEG Force x1 when VGA Enabled	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	
	0	Single PEG Force x1 when VGA Enabled	
		Default Value:	0b
		Access:	R/W Firmware Only
		Unused - Bit field not relevant for the current project	



Device 2 Control

DEV2CTL_0_2_0_PCI - Device 2 Control			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	00058h		
This register implements a control bit to disable and hide the IOBAR register in systems that do not require legacy IOBAR access to Gfx MMIO registers.			
DWord	Bit	Description	
0	7:1	Reserved	
		Default Value:	0000000b
		Access:	RO
		Reserved	
	0	Reserved	



Device Capabilities

DEVICECAP_0_2_0_PCI - Device Capabilities			
Register Space:		PCI: 0/2/0	
Source:		BSpec	
Default Value:		0x10008000	
Size (in bits):		32	
Address:		00074h	
PCI Express Device Capabilities			
DWord	Bit	Description	
0	31:29	Reserved	
		Default Value:	000b
		Access:	RO
		Reserved	
	28	Functional Level Reset Capability	
		Default Value:	1b
		Access:	RO
		Hardwired to 1b to indicate the Function supports the optional Function Level Reset mechanism.	
	27:26	Captured Slot Power Limit Scale	
		Default Value:	00b
		Access:	RO
		Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00b	
	25:18	Captured Slot Power Limit Value	
		Default Value:	00000000h
		Access:	RO
		Not applicable for a Root Complex Integrated Endpoint with no Link or Slot. Hardwired to 00h	
	17:16	Reserved	
		Default Value:	00b
		Access:	RO
		Reserved	
	15	Role-Based Error Reporting	
		Default Value:	1b
		Access:	RO

**DEVICECAP_0_2_0_PCI - Device Capabilities**

		When Set, this bit indicates that the Function implements the functionality originally defined in the Error Reporting ECN for PCI Express Base Specification, Revision 1.0a, and later incorporated into PCI Express Base Specification, Revision 1.1. Hardwired to 1b as this bit must be Set by all Functions conforming to the ECN, PCI Express Base Specification, Revision 1.1, or subsequent PCI Express Base Specification revisions.	
14:12	RESERVED		
	Default Value:		000b
	Access:		RO
	Reserved		
11:9	Endpoint L1 Acceptable Latency		
	Default Value:		000b
	Access:		RO
	This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L1 state to the L0 state. This does not apply to the integrated graphics device, so it is hardwired to 000b (Maximum of 1 us).		
8:6	Endpoint L0s Acceptable Latency		
	Default Value:		000b
	Access:		RO
	This field indicates the acceptable total latency that an Endpoint can withstand due to the transition from the L0s state to the L0 state. This does not apply to the integrated graphics device, so it is hardwired to 000b (Maximum of 64 ns).		
5	Extended Tag Field Supported		
	Default Value:		0b
	Access:		RO
	This bit indicates the maximum supported size of the Tag field as a Requester. This does not apply to the integrated graphics device, so it is hardwired to 0b (5-bit Tag field supported).		
4:3	Phantom Functions Supported		
	Default Value:		00b
	Access:		RO
	This field indicates the support for use of unclaimed Function Numbers to extend the number of outstanding transactions for PCIe devices. This does not apply to the integrated graphics device, so it is hardwired to 00b to indicate no Function Number bits are used for Phantom Functions.		



DEVICECAP_0_2_0_PCI - Device Capabilities			
	2:0	Max Payload Size Supported	
		Default Value:	000b
		Access:	RO
		This field indicates the maximum payload size that the Function can support for TLPs. Hardwired to 000b to represents 128 bytes, the minimum allowed value.	



Device Enable

DEVEN_0_0_0_PCI - Device Enable			
Register Space:		PCI: 0/0/0	
Source:		BSpec	
Default Value:		0x000000BF	
Size (in bits):		32	
Address:		00054h	
Allows for enabling/disabling of PCI devices and functions that are within the CPU package.			
DWord	Bit	Description	
0	31:15	RESERVED	
		Default Value:	000b
		Access:	RO
	14	Chap Enable	
		Default Value:	0b
		Access:	R/W
		Unused - Bit field not relevant for the current project	
	13	Device 6 Enable	
		Default Value:	0b
		Access:	R/W
		Unused - Bit field not relevant for the current project	
	12:11	RESERVED	
		Default Value:	000b
		Access:	RO
	10	Device 5 Enable	
		Default Value:	0b
		Access:	R/W Lock
		Unused - Bit field not relevant for the current project	
	9:8	RESERVED	
		Default Value:	000b
		Access:	RO
	7	Device 4 Enable	
		Default Value:	1b
		Access:	R/W Lock
		Unused - Bit field not relevant for the current project	



DEVEN_0_0_0_PCI - Device Enable

	6	RESERVED	
		Default Value:	000b
		Access:	RO
	5	Device 3 enable for Display HD Audio	
		Default Value:	1b
		Access:	R/W Lock
	4	Internal Graphics Engine	
		Default Value:	1b
		Access:	R/W Lock
		0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled.	
	3	PEG10 Enable	
		Default Value:	1b
		Access:	R/W Lock
	2	Unused - Bit field not relevant for the current project	
		PEG11 Enable	
		Default Value:	1b
		Access:	R/W Lock
	1	Unused - Bit field not relevant for the current project	
		PEG12 Enable	
		Default Value:	1b
	0	Access:	R/W Lock
		Host Bridge	
		Default Value:	1b
		Access:	RO



Device Identification

DID2_0_2_0_PCI - Device Identification			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000A84		
Size (in bits):	16		
Address:	00002h		
This register combined with the Vendor Identification register uniquely identifies any PCI device.			
DWord	Bit	Description	
0	15:7	Device Identification Number MSB	
		Default Value:	000010101b
		Access:	RO Variant Firmware Only
		This is the upper part of a 16 bit value assigned to the device.	
	6:2	Device Identification Number STRAPS	
		Default Value:	00001b
		Access:	RO Variant
		These are bits 6:2 of the 16 bit value, updated from straps.	
	1:0	Device Identification Number SKU	
		Default Value:	00b
		Access:	RO Variant
		This is the lower part of a 16 bit value assigned to the device.	



DFSM

DFSM				
Register Space:	MMIO: 0/2/0			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	51000h-51003h			
Name:	Display Fuse			
ShortName:	DFSM			
Power:	PG0			
Reset:	global			
This register contains fuse and strap settings for display. This register is not reset by FLR.				
DWord	Bit	Description		
0	31	Internal Graphics Disable This bit indicates whether internal graphics capability is disabled.		
		Value	Name	Description
		0b	Enable	Internal Graphics Enabled
		1b	Disable	Internal Graphics Disabled
		30	Internal Display Disable This bit indicates whether the display pipe A (first pipe) capability is disabled.	
	Value		Name	Description
	0b		Enable	Pipe A Capability Enabled
	1b		Disable	Pipe A Capability Disabled
	29		Reserved	
	28	Display PipeC Disable This bit indicates whether the display pipe C (third pipe) capability is disabled.		
		Value	Name	Description
		0b	Enable	Pipe C Capability Enabled
		1b	Disable	Pipe C Capability Disabled
		27	Display PM Disable This bit indicates whether the display power management FBC and DPST capabilities are disabled.	
	Value		Name	Description
	0b		Enable	PM Capability Enabled
	1b		Disable	PM Capability Disabled

**DFSM**

	26	Display eDP Disable	
		Description	
		This bit indicates whether the display embedded DisplayPort eDP DDIA capability is disabled.	
		Value	Name
		0b	Enable
		1b	Disable
	25	Reserved	
	24:23	Display CDCLK Limit	
		This field indicates the maximum allowed CD clock frequency.	
		Value	Name
		00b	675 MHz
		01b	540 MHz
		10b	450 MHz
		11b	337.5 MHz
		Programming Notes	
		This field is unused on BXT. Any CD clock frequency limitation must be done in software.	
		Restriction	
		Restriction : Display software should not select any frequency higher than the maximum that is allowed. If software incorrectly selects a higher frequency, display hardware will internally override the selection to the lowest frequency.	
	22	Display Spare	
	21	Spare 21	
		This bit indicates whether the display pipe B (second pipe) capability is disabled.	
		Value	Name
		0b	Pipe B Capability Enabled
		1b	Pipe B Capability Disabled
	20	Display WD Disable	
		This bit indicates whether the display WD capability is disabled.	
		Value	Name
		0b	Enable
		1b	Disable
	19	Spare 19	
	18	Spare 18	
	17	Spare 17	



DFSM				
		Description		
		Device ID bit 1		
	16	Spare 16		
		Description		
		Device ID bit 0		
	15	Spare 15		
	14	Spare 14		
	13	Spare 13		
	12	Spare 12		
	11	Spare 11		
	10	Spare 10		
	9	Spare 9		
	8	Spare 8		
	7	Spare 7		
		Description		
		This field indicates whether the DSC feature is disabled.		
		Value	Name	
		0b	DSC Capability Enabled	
		1b	DSC Capability Disabled	
	6	Display RSB Enable		
		This bit indicates whether the remote screen blanking feature is enabled in the display engine.		
		Value	Name	Description
		0b	Disable	RSB Capability Disabled
		1b	Enable	RSB Capability Enabled
	5	Spare 5		
	4	Spare 4		
	3	Spare 3		
	2	Spare 2		
1	Reserved			
0	Display Audio Codec Disable			
	This bit indicates whether the display audio codec capability is disabled.			
	Value	Name	Description	
	0b	Enable	Audio Codec Capability Enabled	
	1b	Disable	Audio Codec Capability Disabled	



DISPLAY_DEADLINE_CONTROL

DISPLAY_DEADLINE_CONTROL - DISPLAY_DEADLINE_CONTROL		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 10102Ch		
Deadline latency override control		
DWord	Bit	Description
0	31:11	Reserved
		Default Value: 0000000h
		Access: R/W
	10:1	Reserved
		Latency_Override_Offset
		Default Value: 000h
	0	Access: R/W
		When enable, provides a fixed latency offset override for display VC1 requests. For example, value of 0 would sent every VC1 request with the current global time value .. effectively making every VC1 request access "urgent".
		Latency_Override_Enable
		Default Value: 0b
		Access: R/W
		0 (default) : Hardware determined deadlines. 1 : Latency override enabled. Deadline latency offsets are no longer hardware determined. Instead, deadline latency offsets are taken from the "latency_override_offset" bits



DMA Protected Range

DPR_0_0_0_PCI - DMA Protected Range			
Register Space:	PCI: 0/0/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address: 0005Ch			
DMA protected range register.			
DWord	Bit	Description	
0	31:20	Top of DPR	
		Default Value:	000000000000b
		Access:	RO Variant Firmware Only
		Top address + 1 of DPR. This is the base of TSEG. Bits 19:0 of the BASE reported here are 0x0_0000.	
	19:12	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	11:4	DPRSIZE	
		Default Value:	00000000b
		Access:	R/W Lock
		This is the size of memory, in MB, that will be protected from DMA accesses. A value of 0x00 in this field means no additional memory is protected. The maximum amount of memory that will be protected is 255MB. The amount of memory reported in this field will be protected from all DMA accesses, including translated CPU accesses and graphics. The top of the protected range is the BASE of TSEG -1. Note: If TSEG is not enabled, then the top of this range becomes the base of stolen graphics, or ME stolen space or TOLUD, whichever would have been the location of TSEG, assuming it had been enabled. The DPR range works independently of any other range, including the NoDMA.TABLE protection or the PMRC checks in VTd, and is done post any VTd translation or LT NoDMA lookup. Therefore incomming cycles are checked against this range after the VTd translation and faulted if they hit this protected range, even if they passed the VTd translation or were clean in the NoDMA lookup. All the memory checks are OR'ed with respect to NOT being allowed to go to memory. So if either PMRC, DPR, NoDMA table lookup, NoDMA.TABLE.PROTECT OR a VTd translation disallows the cycle, then the cycle is not allowed to go to memory. Or in other words, all of the above checks must pass before a cycle is allowed to DRAM.	



DPR_0_0_0_PCI - DMA Protected Range		
	3	RESERVED
		Default Value: 000b
		Access: RO
		Reserved
	2	EPM
		Default Value: 0b
		Access: R/W Lock
		This field controls DMA accesses to the DMA Protected Range (DPR) region. 0: DPR is disabled. 1: DPR is enabled. All DMA requests accessing DPR region are blocked. Dev 0 HW reports the status of DPR enable/disabled through the PRS field in this register.
	1	Protected Range Status
		Default Value: 0b
		Access: RO Variant Firmware Only
		This field indicated the status of DPR. 0: DPR protection disabled. 1: DPR protection enabled.
	0	Lock
		Default Value: 0b
		Access: R/W Key Lock
		All bits which may be updated by SW in this register are locked down when this bit is set.



DPFC_CONTROL_SA

DPFC_CTL_SA - DPFC_CONTROL_SA			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000000	
Size (in bits):		32	
Address:		100100h	
This register contains control bits related to Display Frame Buffer Compression Host Invalidation in System Agent.			
DWord	Bit	Description	
0	31:30	Reserved	
		Default Value:	00b
		Access:	R/W
		Reserved	
	29	CPUFNCEN	
		Default Value:	0b
		Access:	R/W
		0: Display Buffer is not in a CPU fence. No modifications are allowed from CPU to the Display Buffer. 1: Display Buffer exists in a CPU fence.	
	28:5	Reserved	
		Default Value:	000000h
		Access:	R/W
		Reserved	
	4:0	CPUFNCNUM	
		Default Value:	00h
		Access:	R/W
		This field specifies the CPU visible FENCE number corresponding to the placement of the uncompressed frame buffer.	



DPFC_CPU_FENCE_OFFSET

DPFC_CFO - DPFC_CPU_FENCE_OFFSET			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	100104h		
This register contains control bits related to Display Frame Buffer Compression Host Invalidation in System Agent.			
DWord	Bit	Description	
0	31:22	Reserved	
		Default Value:	000h
		Access:	R/W
		Reserved	
	21:0	YFNCDISP	
		Default Value:	000000h
		Access:	R/W
		Y offset from the CPU fence to the Display Buffer base	



DSC_CRC_CTL

DSC_CRC_CTL			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000000			
Access: R/W			
Size (in bits): 32			
Address: 6B284h-6B287h			
Name: DSC_CRC_CTL_A			
ShortName: DSC_CRC_CTL_A			
Power: PG1			
Reset: soft			
Address: 6BA84h-6BA87h			
Name: DSC_CRC_CTL_C			
ShortName: DSC_CRC_CTL_C			
Power: PG1			
Reset: soft			
DWord	Bit	Description	
0	31	Enable CRC	
		Access: R/W	
		Enables the CRC calculations. The CRC will give a done indication and a new result at the end of each frame.	
		Value	Name
		0b	Disable
		1b	Enable
	30	CRC Done	
		Access: R/WC	
		This bit is set on the rising edge of the CRC done indication. This is a sticky bit, cleared by writing 1b to it.	
		Value	Name
		0b	Not Done
		1b	Done
	29	CRC Change	
		Access: R/WC	
This bit is set if the CRC result value changes from the previous value. This is a sticky bit, cleared by writing 1b to it.			



DSC_CRC_CTL			
		Value	Name
		0b	No Change
		1b	Change
	28:0	Reserved	
		Format:	MBZ



DSC_CRC_RES

DSC_CRC_RES		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Address:	6B288h-6B28Bh	
Name:	DSC_CRC_RES_A	
ShortName:	DSC_CRC_RES_A	
Power:	PG1	
Reset:	soft	
Address:	6BA88h-6BA8Bh	
Name:	DSC_CRC_RES_C	
ShortName:	DSC_CRC_RES_C	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:0	CRC Result Value This field contains the CRC result at the end of a CRC frame. The CRC done bit indicates when the result is valid.



DSC_PICTURE_PARAMETER_SET_0

DSC_PICTURE_PARAMETER_SET_0				
Register Space:		MMIO: 0/2/0		
Source:		BSpec		
Default Value:		0x00000000		
Access:		R/W		
Size (in bits):		32		
Address:		6B200h-6B203h		
Name:		DSCA_PICTURE_PARAMETER_SET_0		
ShortName:		DSCA_PICTURE_PARAMETER_SET_0		
Power:		PG1		
Reset:		soft		
Address:		6BA00h-6BA03h		
Name:		DSCC_PICTURE_PARAMETER_SET_0		
ShortName:		DSCC_PICTURE_PARAMETER_SET_0		
Power:		PG1		
Reset:		soft		
DWord	Bit	Description		
0	31:20	Reserved		
		Format:	MBZ	
	19	vbr_enable		
		Access:	R/W	
		Value	Name	Description
		0b	disable [Default]	"0" padding bits are stuffed at the end of a slice to ensure that the total number of bits within the slice is equal to the slice bit budget.
		1b	Enable	Bit stuffing is bypassed
	18	enable_422		
		Access:	R/W	
		Value	Name	Description
		0b	444 [Default]	Input uses 4:4:4 sampling
		1b	422	Input uses 4:2:2 sampling
	17	convert_rgb		
Access:		R/W		
Indicates whether DSC color space conversion is active.				



DSC_PICTURE_PARAMETER_SET_0			
		Value	Name
		0b	YCbCr
		1b	convert_rgb
	16	block_pred_enable	
		Access:	
		R/W	
		Value	Name
		0b	disable
	15:12	linebuf_depth	
		Access:	
		R/W	
		Contains the line buffer bit depth used to generate the bitstream. If a component's bit depth (after color space conversion) is greater than this value, the line storage rounds the reconstructed values to this number of bits.	
		0x8 = 8 bits	
	11:8	bits_per_component	
		Access:	
		R/W	
		Indicates the number of bits per component for the original pixels of the encoded picture.	
		0x8 = 8bpc	
	7:4	dsc_version_minor	
		Access:	
		R/W	
		Contains the major version of DSC.	
		0x1 = Encoder implements DSC	
	3:0	dsc_version_major	
		Access:	
		R/W	
		Contains the major version of DSC.	
		0x1 = Encoder implements DSC	



DSC_PICTURE_PARAMETER_SET_1

DSC_PICTURE_PARAMETER_SET_1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B204h-6B207h	
Name:	DSCA_PICTURE_PARAMETER_SET_1	
ShortName:	DSCA_PICTURE_PARAMETER_SET_1	
Power:	PG1	
Reset:	soft	
Address:	6BA04h-6BA07h	
Name:	DSCC_PICTURE_PARAMETER_SET_1	
ShortName:	DSCC_PICTURE_PARAMETER_SET_1	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:10	RESERVED
		Format: MBZ
	9:0	bits_per_pixel
		Access: R/W



DSC_PICTURE_PARAMETER_SET_2

DSC_PICTURE_PARAMETER_SET_2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B208h-6B20Bh	
Name:	DSCA_PICTURE_PARAMETER_SET_2	
ShortName:	DSCA_PICTURE_PARAMETER_SET_2	
Power:	PG1	
Reset:	soft	
Address:	6BA08h-6BA0Bh	
Name:	DSCC_PICTURE_PARAMETER_SET_2	
ShortName:	DSCC_PICTURE_PARAMETER_SET_2	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	pic_width
		Access: R/W
	15:0	pic_height
		Access: R/W



DSC_PICTURE_PARAMETER_SET_3

DSC_PICTURE_PARAMETER_SET_3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B20Ch-6B20Fh	
Name:	DSCA_PICTURE_PARAMETER_SET_3	
ShortName:	DSCA_PICTURE_PARAMETER_SET_3	
Power:	PG1	
Reset:	soft	
Address:	6BA0Ch-6BA0Fh	
Name:	DSCC_PICTURE_PARAMETER_SET_3	
ShortName:	DSCC_PICTURE_PARAMETER_SET_3	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	slice_width Access: R/W This defines the width of the slice in number of pixels.
	15:0	slice_height Access: R/W This defines the height of the slice in number of pixels.



DSC_PICTURE_PARAMETER_SET_4

DSC_PICTURE_PARAMETER_SET_4		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B210h-6B213h	
Name:	DSCA_PICTURE_PARAMETER_SET_4	
ShortName:	DSCA_PICTURE_PARAMETER_SET_4	
Power:	PG1	
Reset:	soft	
Address:	6BA10h-6BA13h	
Name:	DSCC_PICTURE_PARAMETER_SET_4	
ShortName:	DSCC_PICTURE_PARAMETER_SET_4	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	initial_dec_delay
		Access: R/W
	15:10	RESERVED
		Format: MBZ
	9:0	initial_xmit_delay
		Access: R/W



DSC_PICTURE_PARAMETER_SET_5

DSC_PICTURE_PARAMETER_SET_5		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B214h-6B217h	
Name:	DSCA_PICTURE_PARAMETER_SET_5	
ShortName:	DSCA_PICTURE_PARAMETER_SET_5	
Power:	PG1	
Reset:	soft	
Address:	6BA14h-6BA17h	
Name:	DSCC_PICTURE_PARAMETER_SET_5	
ShortName:	DSCC_PICTURE_PARAMETER_SET_5	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:28	RESERVED
		Format: MBZ
	27:16	scale_decrement_interval
		Access: R/W
	15:0	scale_increment_interval
		Access: R/W



DSC_PICTURE_PARAMETER_SET_6

DSC_PICTURE_PARAMETER_SET_6		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B218h-6B21Bh	
Name:	DSCA_PICTURE_PARAMETER_SET_6	
ShortName:	DSCA_PICTURE_PARAMETER_SET_6	
Power:	PG1	
Reset:	soft	
Address:	6BA18h-6BA1Bh	
Name:	DSCC_PICTURE_PARAMETER_SET_6	
ShortName:	DSCC_PICTURE_PARAMETER_SET_6	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:29	RESERVED Format: MBZ
	28:24	flatness_max_qp Access: R/W
	23:21	RESERVED Format: MBZ
	20:16	flatness_min_qp Access: R/W
	15:13	RESERVED Format: MBZ
	12:8	first_line_bpg_offset Access: R/W
	7:6	RESERVED Format: MBZ
	5:0	initial_scale_value Access: R/W



DSC_PICTURE_PARAMETER_SET_7

DSC_PICTURE_PARAMETER_SET_7		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B21Ch-6B21Fh	
Name:	DSCA_PICTURE_PARAMETER_SET_7	
ShortName:	DSCA_PICTURE_PARAMETER_SET_7	
Power:	PG1	
Reset:	soft	
Address:	6BA1Ch-6BA1Fh	
Name:	DSCC_PICTURE_PARAMETER_SET_7	
ShortName:	DSCC_PICTURE_PARAMETER_SET_7	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	nfl_bpg_offset
		Access: R/W
	15:0	slice_bpg_offset
		Access: R/W



DSC_PICTURE_PARAMETER_SET_8

DSC_PICTURE_PARAMETER_SET_8		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B220h-6B223h	
Name:	DSCA_PICTURE_PARAMETER_SET_8	
ShortName:	DSCA_PICTURE_PARAMETER_SET_8	
Power:	PG1	
Reset:	soft	
Address:	6BA20h-6BA23h	
Name:	DSCC_PICTURE_PARAMETER_SET_8	
ShortName:	DSCC_PICTURE_PARAMETER_SET_8	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	initial_offset
		Access: R/W
	15:0	final_offset
		Access: R/W



DSC_PICTURE_PARAMETER_SET_9

DSC_PICTURE_PARAMETER_SET_9		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B224h-6B227h	
Name:	DSCA_PICTURE_PARAMETER_SET_9	
ShortName:	DSCA_PICTURE_PARAMETER_SET_9	
Power:	PG1	
Reset:	soft	
Address:	6BA24h-6BA27h	
Name:	DSCC_PICTURE_PARAMETER_SET_9	
ShortName:	DSCC_PICTURE_PARAMETER_SET_9	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:20	RESERVED
		Format: MBZ
	19:16	rc_edge_factor
		Access: R/W
	15:0	rc_model_Size
		Access: R/W



DSC_PICTURE_PARAMETER_SET_10

DSC_PICTURE_PARAMETER_SET_10		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B228h-6B22Bh	
Name:	DSCA_PICTURE_PARAMETER_SET_10	
ShortName:	DSCA_PICTURE_PARAMETER_SET_10	
Power:	PG1	
Reset:	soft	
Address:	6BA28h-6BA2Bh	
Name:	DSCC_PICTURE_PARAMETER_SET_10	
ShortName:	DSCC_PICTURE_PARAMETER_SET_10	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:24	RESERVED Format: MBZ
	23:20	rc_tgt_offset_lo Access: R/W
	19:16	rc_tgt_offset_hi Access: R/W
	15:13	RESERVED Format: MBZ
	12:8	rc_quant_incr_limit1 Access: R/W
	7:5	RESERVED Format: MBZ
	4:0	rc_quant_incr_limit0 Access: R/W



DSC_PICTURE_PARAMETER_SET_11

DSC_PICTURE_PARAMETER_SET_11		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B22Ch-6B22Fh	
Name:	DSCA_PICTURE_PARAMETER_SET_11	
ShortName:	DSCA_PICTURE_PARAMETER_SET_11	
Power:	PG1	
Reset:	soft	
Address:	6BA2Ch-6BA2Fh	
Name:	DSCC_PICTURE_PARAMETER_SET_11	
ShortName:	DSCC_PICTURE_PARAMETER_SET_11	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:0	RESERVED
		Format: MBZ



DSC_PICTURE_PARAMETER_SET_12

DSC_PICTURE_PARAMETER_SET_12		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B260h-6B263h	
Name:	DSCA_PICTURE_PARAMETER_SET_12	
ShortName:	DSCA_PICTURE_PARAMETER_SET_12	
Power:	PG1	
Reset:	soft	
Address:	6BA60h-6BA63h	
Name:	DSCC_PICTURE_PARAMETER_SET_12	
ShortName:	DSCC_PICTURE_PARAMETER_SET_12	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:0	RESERVED
		Format: MBZ



DSC_PICTURE_PARAMETER_SET_13

DSC_PICTURE_PARAMETER_SET_13		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B264h-6B267h	
Name:	DSCA_PICTURE_PARAMETER_SET_13	
ShortName:	DSCA_PICTURE_PARAMETER_SET_13	
Power:	PG1	
Reset:	soft	
Address:	6BA64h-6BA67h	
Name:	DSCC_PICTURE_PARAMETER_SET_13	
ShortName:	DSCC_PICTURE_PARAMETER_SET_13	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:0	RESERVED
		Format: MBZ



DSC_PICTURE_PARAMETER_SET_14

DSC_PICTURE_PARAMETER_SET_14		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B268h-6B26Bh	
Name:	DSCA_PICTURE_PARAMETER_SET_14	
ShortName:	DSCA_PICTURE_PARAMETER_SET_14	
Power:	PG1	
Reset:	soft	
Address:	6BA68h-6BA6Bh	
Name:	DSCC_PICTURE_PARAMETER_SET_14	
ShortName:	DSCC_PICTURE_PARAMETER_SET_14	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:0	RESERVED
		Format: MBZ



DSC_PICTURE_PARAMETER_SET_15

DSC_PICTURE_PARAMETER_SET_15		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B26Ch-6B26Fh	
Name:	DSCA_PICTURE_PARAMETER_SET_15	
ShortName:	DSCA_PICTURE_PARAMETER_SET_15	
Power:	PG1	
Reset:	soft	
Address:	6BA6Ch-6BA6Fh	
Name:	DSCC_PICTURE_PARAMETER_SET_15	
ShortName:	DSCC_PICTURE_PARAMETER_SET_15	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:0	RESERVED
		Format: MBZ



DSC_PICTURE_PARAMETER_SET_16

DSC_PICTURE_PARAMETER_SET_16		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B270h-6B273h	
Name:	DSCA_PICTURE_PARAMETER_SET_16	
ShortName:	DSCA_PICTURE_PARAMETER_SET_16	
Power:	PG1	
Reset:	soft	
Address:	6BA70h-6BA73h	
Name:	DSCC_PICTURE_PARAMETER_SET_16	
ShortName:	DSCC_PICTURE_PARAMETER_SET_16	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:20	slice_row_per_frame Access: R/W
	19	RESERVED Format: MBZ
	18:16	slice_per_line Access: R/W
	15:0	slice_chunk_size Access: R/W



DSC_RC_BUF_THRESH_0

DSC_RC_BUF_THRESH_0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	6B230h-6B237h	
Name:	DSCA_RC_BUF_THRESH_0	
ShortName:	DSCA_RC_BUF_THRESH_0	
Power:	PG1	
Reset:	soft	
Address:	6BA30h-6BA37h	
Name:	DSCC_RC_BUF_THRESH_0	
ShortName:	DSCC_RC_BUF_THRESH_0	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:24	rc_buf_thresh_3 Access: R/W
	23:16	rc_buf_thresh_2 Access: R/W
	15:8	rc_buf_thresh_1 Access: R/W
	7:0	rc_buf_thresh_0 Access: R/W
1	31:24	rc_buf_thresh_7 Access: R/W
	23:16	rc_buf_thresh_6 Access: R/W
	15:8	rc_buf_thresh_5 Access: R/W
	7:0	rc_buf_thresh_4 Access: R/W



DSC_RC_BUF_THRESH_1

DSC_RC_BUF_THRESH_1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	6B238h-6B23Fh	
Name:	DSCA_RC_BUF_THRESH_1	
ShortName:	DSCA_RC_BUF_THRESH_1	
Power:	PG1	
Reset:	soft	
Address:	6BA38h-6BA3Fh	
Name:	DSCC_RC_BUF_THRESH_1	
ShortName:	DSCC_RC_BUF_THRESH_1	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:24	rc_buf_thresh_11 Access: R/W
	23:16	rc_buf_thresh_10 Access: R/W
	15:8	rc_buf_thresh_9 Access: R/W
	7:0	rc_buf_thresh_8 Access: R/W
1	31:16	RESERVED Format: MBZ
	15:8	rc_buf_thresh_13 Access: R/W
	7:0	rc_buf_thresh_12 Access: R/W



DSC_RC_RANGE_PARAMETERS_0

DSC_RC_RANGE_PARAMETERS_0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	6B240h-6B247h	
Name:	DSCA_RC_RANGE_PARAMETERS_0	
ShortName:	DSCA_RC_RANGE_PARAMETERS_0	
Power:	PG1	
Reset:	soft	
Address:	6BA40h-6BA47h	
Name:	DSCC_RC_RANGE_PARAMETERS_0	
ShortName:	DSCC_RC_RANGE_PARAMETERS_0	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:26	rc_bpg_offset_1 Access: R/W
	25:21	rc_max_qp_1
	20:16	rc_min_qp_1
	15:10	rc_bpg_offset_0 Access: R/W
	9:5	rc_max_qp_0
	4:0	rc_min_qp_0
1	31:26	rc_bpg_offset_3 Access: R/W
	25:21	rc_max_qp_3
	20:16	rc_min_qp_3
	15:10	rc_bpg_offset_2 Access: R/W
	9:5	rc_max_qp_2
	4:0	rc_min_qp_2



DSC_RC_RANGE_PARAMETERS_1

DSC_RC_RANGE_PARAMETERS_1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	6B248h-6B24Fh	
Name:	DSCA_RC_RANGE_PARAMETERS_1	
ShortName:	DSCA_RC_RANGE_PARAMETERS_1	
Power:	PG1	
Reset:	soft	
Address:	6BA48h-6BA4Fh	
Name:	DSCC_RC_RANGE_PARAMETERS_1	
ShortName:	DSCC_RC_RANGE_PARAMETERS_1	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:26	rc_bpg_offset_5 Access: R/W
	25:21	rc_max_qp_5
	20:16	rc_min_qp_5
	15:10	rc_bpg_offset_4 Access: R/W
	9:5	rc_max_qp_4
	4:0	rc_min_qp_4
1	31:26	rc_bpg_offset_7 Access: R/W
	25:21	rc_max_qp_7
	20:16	rc_min_qp_7
	15:10	rc_bpg_offset_6 Access: R/W
	9:5	rc_max_qp_6
	4:0	rc_min_qp_6



DSC_RC_RANGE_PARAMETERS_2

DSC_RC_RANGE_PARAMETERS_2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	6B250h-6B257h	
Name:	DSCA_RC_RANGE_PARAMETERS_2	
ShortName:	DSCA_RC_RANGE_PARAMETERS_2	
Power:	PG1	
Reset:	soft	
Address:	6BA50h-6BA57h	
Name:	DSCC_RC_RANGE_PARAMETERS_2	
ShortName:	DSCC_RC_RANGE_PARAMETERS_2	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:26	rc_bpg_offset_9 Access: R/W
	25:21	rc_max_qp_9
	20:16	rc_min_qp_9
	15:10	rc_bpg_offset_8 Access: R/W
	9:5	rc_max_qp_8
	4:0	rc_min_qp_8
1	31:26	rc_bpg_offset_11 Access: R/W
	25:21	rc_max_qp_11
	20:16	rc_min_qp_11
	15:10	rc_bpg_offset_10 Access: R/W
	9:5	rc_max_qp_10
	4:0	rc_min_qp_10



DSC_RC_RANGE_PARAMETERS_3

DSC_RC_RANGE_PARAMETERS_3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Address:	6B258h-6B25Fh	
Name:	DSCA_RC_RANGE_PARAMETERS_3	
ShortName:	DSCA_RC_RANGE_PARAMETERS_3	
Power:	PG1	
Reset:	soft	
Address:	6BA58h-6BA5Fh	
Name:	DSCC_RC_RANGE_PARAMETERS_3	
ShortName:	DSCC_RC_RANGE_PARAMETERS_3	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:26	rc_bpg_offset_13 Access: R/W
	25:21	rc_max_qp_13
	20:16	rc_min_qp_13
	15:10	rc_bpg_offset_12 Access: R/W
	9:5	rc_max_qp_12
	4:0	rc_min_qp_12
1	31:26	Reserved
	25:21	Reserved
	20:16	Reserved
	15:10	rc_bpg_offset_14 Access: R/W
	9:5	rc_max_qp_14
	4:0	rc_min_qp_14



DSI_PHY_DW6

DSI_PHY_DW6			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000001		
Access:	R/W		
Size (in bits):	32		
Address:	160018h-16001Bh		
Name:	DSI_PHY_DW6		
ShortName:	DSI_PHY_DW6		
Power:	PG0		
Reset:	global		
DWord	Bit	Description	
0	31:23	Reserved	
		Format: MBZ	
	22	FORCE_HS_UPDATE Forced update mode for HS ; Does not wait for any device state	
	21	DSI_HS_RCOMP_UPDATE LNC clock lane update bit. When this bit is set RCOMP will update Clock lane with calibrated value when its data lane is in stop state. When it is clear it updates when clock lane itself in LP states	
	20:19	DSI_HS_TOGGLE_LIMIT_CREG_ENC HS state machine toggle limit. Number of times RCOMP state machine will toggle before exiting.	
		Value	Name
		00b	6 toggles
		01b	4 toggles
		10b	8 toggles
		11b	10 toggles
	18:16	DSI_HS_CALIB_LOOP_DELAY Delay after applying a new RCOMP value to the AFE, before sampling the count up/down input from the AFE. At the start of each RCOMP calibration cycle, the state machine waits for 8x this delay before starting to sample the count up/down signal.	
		Value	Name
0h		50-53ns	
1h		60ns	
2h		70-72s	
3h		80-83ns	



DSI_PHY_DW6			
		4h	90ns
		5h	100-102ns
		6h	125-128ns
		7h	159ns
	15:9	Reserved	
		Format:	MBZ
	8	HS_OVR_EN HS override enable	
	7:6	Reserved	
		Format:	MBZ
	5:1	HS_OVR_VALUE HS override values	
	0	HS_CALIB_EN Enable HS calibration	
		Value	Name
		1b	[Default]
		0b	



DSI_PLL_CTL

DSI_PLL_CTL				
Register Space:	MMIO: 0/2/0			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	161000h-161003h			
Name:	DSI PLL Control			
ShortName:	DSI_PLL_CTL			
Power:	PG0			
Reset:	global			
The register is used to control the frequency of the outputs from the MIPI DSI PLL. The DSI_PLL_ENABLE register controls the MIPI DSI PLL enable. The MIPI_CLOCK_CTL register controls additional dividers.				
Restriction				
Restriction : The fields must not be changed while the PLL is enabled.				
DWord	Bit	Description		
0	31:25	Reserved		
		Format: MBZ		
	24:18	Output Ratio		
		Set the output clock ratio.		
		Restriction		
	17:16	Restriction : Display software must not change this field.		
			PVD Ratio	
			Set the post VCO divider ratio.	
			Value	Name
			00b	1
			01b	2
			10b	4
11b			8	
Restriction				
Restriction : Display software must not change this field.				



DSI_PLL_CTL				
	15:14	Ref Ratio		
		Set the refclk ratio.		
		Value		Name
		00b		Ref
		01b		Ref/2
		10b		Ref/4
		11b		Ref/8
		Restriction		
		Restriction : Display software must not change this field.		
	13	Force On		
		Force the PLL on.		
		Value		Name
		0b		No Force
		1b		Force On
		Restriction		
		Restriction : Display software must not change this field.		
	12	Force Off		
		Force the PLL off.		
		Value		Name
		0b		No Force
		1b		Force Off
		Restriction		
		Restriction : Display software must not change this field.		
	11:10	Freq Sel C		
		Frequency Select for DSI C clock		
		Value	Name	Description
		00b	16X	Non DSI
		01b	8X	Divide 16X PLL output by 2
		10b	16X/3	Divide 16X PLL output by 3
		11b	4X	Divide 16X PLL output by 4
		Programming Notes		
		Restriction : This value must not be used when the PLL is enabled.		



DSI_PLL_CTL				
	9:8	Freq Sel A		
		Frequency Select for DSI A clock		
		Value	Name	Description
		00b	16X	Non DSI
		01b	8X	Divide 16X PLL output by 2
		10b	16X/3	Divide 16X PLL output by 3
		11b	4X	Divide 16X PLL output by 4
	7:0	PLL Ratio		
		Description		
		This field provides the feedback ratio for the PLL. Values from 34d (22h) to 125d (7Dh) are allowed.		



DSI_PLL_ENABLE

DSI_PLL_ENABLE			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	46080h-46083h		
Name:	DSI PLL Enable		
ShortName:	DSI_PLL_ENABLE		
Power:	Always on		
Reset:	soft		
DWord	Bit	Description	
0	31	PLL Enable	
		This field enables or disables the DSI PLL.	
		Value	Name
		0b	Disable
	30	1b	Enable
		PLL Lock	
		Access: RO	
		This fields indicates the status of the DSI PLL lock.	
		Value	Name
		0b	Not locked or not enabled
		1b	Locked
		29:0	Reserved
	Format:		MBZ



DSI_RCOMP_CFG1

DSI_RCOMP_CFG1			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000000	
Access:		R/W	
Size (in bits):		32	
Address:		16000Ch-16000Fh	
Name:		DSI_RCOMP_CFG1	
ShortName:		DSI_RCOMP_CFG1	
Power:		PG0	
Reset:		global	
DWord	Bit	Description	
0	31	mipA_dphy_defeature_en This field must be set to 0x1 when enabling MIPI port A.	
	30:28	mipA_lane_count This field specifies the number of lanes to be used for MIPI port A. This field is only used on BXT A0.	
		Value	Name
		000b	0 lanes
		001b	1 lane
		010b	2 lanes
		011b	3 lanes
		100b	4 lanes
	27	mipC_dphy_defeature_en This field must be set to 0x1 when enabling MIPI port C.	
	26:24	mipC_lane_count This field specifies the number of lanes to be used for MIPI port C. This field is only used on BXT A0.	
		Value	Name
		000b	0 lanes
		001b	1 lane
010b		2 lanes	
011b		3 lanes	
23:16	Reserved		
	Format:	MBZ	



DSI_RCOMP_CFG1		
	15:13	CZCLK_CLK_FREQ C
	12:11	RCOMP_CLK_FREQ
	10	Reserved Format: MBZ
	9:6	LP_P_RCOMP_OVR_SLEW
	5	Reserved Format: MBZ
	4:1	LP_N_RCOMP_OVR_SLEW
	0	LP_RCOMP_SLEW_OVR_EN



DSSM

DSSM		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	51004h-51007h	
Name:	Display Strap State	
ShortName:	DSSM	
Power:	PG0	
Reset:	global	
This register contains fuse and strap settings for display. This register is not reset by FLR.		
DWord	Bit	Description
0	31	Spare 31
	30	Spare 30
	29	Spare 29
	28	Spare 28
	27	Spare 27
	26	Spare 26
	25	Spare 25
	24	Spare 24
	23	Spare 23
	22	Spare 22
	21	Spare 21
	20	Spare 20
	19	Spare 19
	18	Spare 18
	17	Spare 17
	16	Spare 16
15	Spare 15	
14	Spare 14	
13	Spare 13	
12	Spare 12	
11	Spare 11	



DSSM			
	10	Spare 10	
	9	Spare 9	
	8	Spare 8	
	7	Spare 7	
	6	Spare 6	
	5	Spare 5	
	4	Spare 4	
	3	Spare 3	
	2	LCPLL Unavail	
		This bit specifies the availability of some LCPLL output frequencies.	
		Value	Name
		Description	
		0b	Available
		1b	Not available
		LCPLL available	
LCPLL not available			
1	Spare 1		
0	DisplayPort A Present		
	Description		
	This bit specifies whether the port was present during initalization. This strap state can also be read in the DDI_BUF_CTL_A 0x64000 register bit 0.		
	There are no port presence straps on Broxton. Software should use alternate means to determine port presence.		
	Value	Name	
	Description		
	0b	Not Present	
	1b	Present	
	Port not present		
	Port present		



EU PAIR 1 PFET control register with lock

PFETCTL - EU PAIR 1 PFET control register with lock		
Register Space:		MMIO: 0/2/0
Source:		BSpec
Default Value:		0x0003000A
Size (in bits):		32
Address:		24688h
DWord	Bit	Description
0	31	PFET Control Lock
		Access: R/W Lock 0 = Bits of EU PAIR 1 PFETCTL register are R/W 1 = All bits of EU PAIR 1 PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	Reserved
		Access: RO Reserved
	20	Power Well Status
	Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
19	Powergood timer error	
	Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
18:16	Delay from enabling secondary PFETs to power good.	
	Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns	



PFETCTL - EU PAIR 1 PFET control register with lock

PFETCTL - EU PAIR 1 PFET control register with lock						
		3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns <table><tr><th>Value</th><th>Name</th></tr><tr><td>011b</td><td>[Default]</td></tr></table>	Value	Name	011b	[Default]
Value	Name					
011b	[Default]					
15:13	Time period last primay pfet strobe to secondary pfet strobe <table><tr><td>Access:</td><td>R/W Lock</td></tr></table> Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)		Access:	R/W Lock		
Access:	R/W Lock					
12:10	Time period b/w two adjacent strobes <table><tr><td>Access:</td><td>R/W Lock</td></tr></table> Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)		Access:	R/W Lock		
Access:	R/W Lock					
9:7	FET setup margin from enable to strobe <table><tr><td>Access:</td><td>R/W Lock</td></tr></table> Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)		Access:	R/W Lock		
Access:	R/W Lock					
6:0	Number of flops to enable primary FETs <table><tr><td>Default Value:</td><td>0001010b</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed		Default Value:	0001010b	Access:	R/W Lock
Default Value:	0001010b					
Access:	R/W Lock					



EU PAIR 2 PGFET control register with lock

PFETCTL - EU PAIR 2 PGFET control register with lock		
Register Space:		MMIO: 0/2/0
Source:		BSpec
Default Value:		0x0003000A
Size (in bits):		32
Address:		24708h
DWord	Bit	Description
0	31	PFET Control Lock
		Access: R/W Lock 0 = Bits of EU PAIR 2 PGFETCTL register are R/W 1 = All bits of EU PAIR 2 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	Reserved
		Access: RO Reserved
	20	Power Well Status
19	Powergood timer error	
	Access: R/WC 0 = Well is powered Down 1 = Well is powered Up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.	
18:16	Delay from enabling secondary PFETs to power good	
	Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns 3'b100: 640ns	



PFETCTL - EU PAIR 2 PGFET control register with lock

		3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns	
		Value	Name
		011b	[Default]
	15:13	Time period last primay pfet strobe to secondary pfet strobe	
		Access:	R/W Lock
Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)			
	12:10	Time period b/w two adjacent strobes	
		Access:	R/W Lock
		Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
	9:7	FET setup margin from enable to strobe	
		Access:	R/W Lock
Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)			
	6:0	Number of flops to enable primary FETs	
		Default Value:	0001010b
		Access:	R/W Lock
		Number of flops to enable primary FETs. For a setting of N, there will be N+1 total strobes generated. 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed	



FENCE_LSB

FENCE_LSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	100000h
Name:	FENCE0_LSB
ShortName:	FENCE0_LSB
Address:	100008h
Name:	FENCE1_LSB
ShortName:	FENCE1_LSB
Address:	100010h
Name:	FENCE2_LSB
ShortName:	FENCE2_LSB
Address:	100018h
Name:	FENCE3_LSB
ShortName:	FENCE3_LSB
Address:	100020h
Name:	FENCE4_LSB
ShortName:	FENCE4_LSB
Address:	100028h
Name:	FENCE5_LSB
ShortName:	FENCE5_LSB
Address:	100030h
Name:	FENCE6_LSB
ShortName:	FENCE6_LSB
Address:	100038h
Name:	FENCE7_LSB
ShortName:	FENCE7_LSB
Address:	100040h
Name:	FENCE8_LSB
ShortName:	FENCE8_LSB
Address:	100048h
Name:	FENCE9_LSB



FENCE_LSB	
ShortName:	FENCE9_LSB
Address:	100050h
Name:	FENCE10_LSB
ShortName:	FENCE10_LSB
Address:	100058h
Name:	FENCE11_LSB
ShortName:	FENCE11_LSB
Address:	100060h
Name:	FENCE12_LSB
ShortName:	FENCE12_LSB
Address:	100068h
Name:	FENCE13_LSB
ShortName:	FENCE13_LSB
Address:	100070h
Name:	FENCE14_LSB
ShortName:	FENCE14_LSB
Address:	100078h
Name:	FENCE15_LSB
ShortName:	FENCE15_LSB
Address:	100080h
Name:	FENCE16_LSB
ShortName:	FENCE16_LSB
Address:	100088h
Name:	FENCE17_LSB
ShortName:	FENCE17_LSB
Address:	100090h
Name:	FENCE18_LSB
ShortName:	FENCE18_LSB
Address:	100098h
Name:	FENCE19_LSB
ShortName:	FENCE19_LSB
Address:	1000A0h
Name:	FENCE20_LSB
ShortName:	FENCE20_LSB



FENCE_LSB		
Address:	1000A8h	
Name:	FENCE21_LSB	
ShortName:	FENCE21_LSB	
Address:	1000B0h	
Name:	FENCE22_LSB	
ShortName:	FENCE22_LSB	
Address:	1000B8h	
Name:	FENCE23_LSB	
ShortName:	FENCE23_LSB	
Address:	1000C0h	
Name:	FENCE24_LSB	
ShortName:	FENCE24_LSB	
Address:	1000C8h	
Name:	FENCE25_LSB	
ShortName:	FENCE25_LSB	
Address:	1000D0h	
Name:	FENCE26_LSB	
ShortName:	FENCE26_LSB	
Address:	1000D8h	
Name:	FENCE27_LSB	
ShortName:	FENCE27_LSB	
Address:	1000E0h	
Name:	FENCE28_LSB	
ShortName:	FENCE28_LSB	
Address:	1000E8h	
Name:	FENCE29_LSB	
ShortName:	FENCE29_LSB	
Address:	1000F0h	
Name:	FENCE30_LSB	
ShortName:	FENCE30_LSB	
Address:	1000F8h	
Name:	FENCE31_LSB	
ShortName:	FENCE31_LSB	
Fence Registers LSBs		
DWord	Bit	Description



FENCE_LSB			
0	31:12	FENCELO	
		Default Value:	000000h
		Access:	R/W
		Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Lower Bound is included in the fence region). Graphics Address is the offset within GMADR space.	
	11:2	RESERVED	
		Default Value:	000h
		Access:	RO
		Reserved	
	1	TILE	
		Default Value:	0b
		Access:	R/W
		This field specifies the spatial ordering of QW within tiles. 0b - Consecutive SWords (32B) sequenced in the X direction 1b - Consecutive OWords (16B) sequenced in the Y direction	
	0	FENCEVAL	
		Default Value:	0b
		Access:	R/W
		This field specifies whether or not this fence register defines a fence region. 0b - FENCE INVALID 1b - FENCE VALID	



FENCE_MSB

FENCE_MSB	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Size (in bits):	32
Address:	100004h
Name:	FENCE0_MSB
ShortName:	FENCE0_MSB
Address:	10000Ch
Name:	FENCE1_MSB
ShortName:	FENCE1_MSB
Address:	100014h
Name:	FENCE2_MSB
ShortName:	FENCE2_MSB
Address:	10001Ch
Name:	FENCE3_MSB
ShortName:	FENCE3_MSB
Address:	100024h
Name:	FENCE4_MSB
ShortName:	FENCE4_MSB
Address:	10002Ch
Name:	FENCE5_MSB
ShortName:	FENCE5_MSB
Address:	100034h
Name:	FENCE6_MSB
ShortName:	FENCE6_MSB
Address:	10003Ch
Name:	FENCE7_MSB
ShortName:	FENCE7_MSB
Address:	100044h
Name:	FENCE8_MSB
ShortName:	FENCE8_MSB
Address:	10004Ch
Name:	FENCE9_MSB



FENCE_MSB	
ShortName:	FENCE9_MSB
Address:	100054h
Name:	FENCE10_MSB
ShortName:	FENCE10_MSB
Address:	10005Ch
Name:	FENCE11_MSB
ShortName:	FENCE11_MSB
Address:	100064h
Name:	FENCE12_MSB
ShortName:	FENCE12_MSB
Address:	10006Ch
Name:	FENCE13_MSB
ShortName:	FENCE13_MSB
Address:	100074h
Name:	FENCE14_MSB
ShortName:	FENCE14_MSB
Address:	10007Ch
Name:	FENCE15_MSB
ShortName:	FENCE15_MSB
Address:	100084h
Name:	FENCE16_MSB
ShortName:	FENCE16_MSB
Address:	10008Ch
Name:	FENCE17_MSB
ShortName:	FENCE17_MSB
Address:	100094h
Name:	FENCE18_MSB
ShortName:	FENCE18_MSB
Address:	10009Ch
Name:	FENCE19_MSB
ShortName:	FENCE19_MSB
Address:	1000A4h
Name:	FENCE20_MSB
ShortName:	FENCE20_MSB



FENCE_MSB		
Address:	1000ACh	
Name:	FENCE21_MSB	
ShortName:	FENCE21_MSB	
Address:	1000B4h	
Name:	FENCE22_MSB	
ShortName:	FENCE22_MSB	
Address:	1000BCh	
Name:	FENCE23_MSB	
ShortName:	FENCE23_MSB	
Address:	1000C4h	
Name:	FENCE24_MSB	
ShortName:	FENCE24_MSB	
Address:	1000CCh	
Name:	FENCE25_MSB	
ShortName:	FENCE25_MSB	
Address:	1000D4h	
Name:	FENCE26_MSB	
ShortName:	FENCE26_MSB	
Address:	1000DCh	
Name:	FENCE27_MSB	
ShortName:	FENCE27_MSB	
Address:	1000E4h	
Name:	FENCE28_MSB	
ShortName:	FENCE28_MSB	
Address:	1000ECh	
Name:	FENCE29_MSB	
ShortName:	FENCE29_MSB	
Address:	1000F4h	
Name:	FENCE30_MSB	
ShortName:	FENCE30_MSB	
Address:	1000FCh	
Name:	FENCE31_MSB	
ShortName:	FENCE31_MSB	
Fence Registers MSBs		
DWord	Bit	Description



FENCE_MSB			
0	31:12	FENCEUP	
		Default Value: 00000000h	
		Access: R/W	
		Bits 31:12 of the ending Graphics Address of the fence region. Fence regions must be aligned to a 4KB page. This address represents the last 4KB page of the fence region (Upper Bound is included in the fence region). Graphics Address is the offset within GMADR space.	
	11	Reserved	
		Default Value: 0b	
		Access: RO	
		Reserved	
	10:0	Pitch	
		Default Value: 000h	
Access: R/W			
This field specifies the width (pitch) of the fence region in multiple of tile widths. For Tile X this field must be programmed to a multiple of 512B (003 is the minimum value) and for Tile Y this field must be programmed to a multiple of 128B (000 is the minimum value). 000h = 128B 001h = 256B 002h = 384B 003h = 512B 004h = 640B 005h = 768B 006h = 896B 007h = 1024B ... 3FFh = 128KB 4FFh = 160KB 5FFh = 192KB 6FFh = 224KB 7FFh = 256KB			

**FLT_RPT0**

FLT_RPT0 - FLT_RPT0			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	124810h		
GT uses this register to post VT-d faults			
DWord	Bit	Description	
0	31:12	FI	
		Default Value: 00000h	
		Access: R/W	
		Fault Info.	
	11:0	RESERVED	
		Default Value: 000h	
		Access: RO	



FLT_RPT1

FLT_RPT1 - FLT_RPT1			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	124814h		
GT uses this register to post VT-d faults			
DWord	Bit	Description	
0	31:0	FI	
		Default Value:	00000000h
		Access:	R/W
		Fault Info.	

**FLT_RPT2**

FLT_RPT2 - FLT_RPT2			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000010		
Size (in bits):	32		
Address:	124818h		
GT uses this register to post VT-d faults			
DWord	Bit	Description	
0	31	PP	
		Default Value:	0h
		Access:	R/W
		PASID Present.	
	30	EXE	
		Default Value:	0h
		Access:	R/W
		Execute Permission Requested.	
	29	PRIV	
		Default Value:	0h
		Access:	R/W
		Privilege Mode Requested .	
	28:16	RESERVED	
		Default Value:	0000h
		Access:	RO
		Reserved	
	15:0	Source ID	
		Default Value:	0010h
		Access:	RO
		Source ID.	



FLT_RPT3

FLT_RPT3 - FLT_RPT3			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	12481Ch		
GT uses this register to post VT-d faults			
DWord	Bit	Description	
0	31	F	
		Default Value:	0h
		Access:	R/W
		Fault	
	30	T	
		Default Value:	0h
		Access:	R/W
		Type	
	29:28	AT	
		Default Value:	0h
		Access:	R/W
		Address Type	
	27:8	PN	
		Default Value:	00000h
		Access:	R/W
		PASID Number	
	7:0	FR	
		Default Value:	0h
		Access:	R/W
		Fault Reason	



GFX_FLSH_CNT

GFX_FLSH_CNT - GFX_FLSH_CNT			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000000	
Size (in bits):		32	
Address:		101008h	
Used to flush Gunit TLB			
DWord	Bit	Description	
0	31:1	RESERVED	
		Default Value: 00000000h	
		Access: RO	
		Reserved	
	0	GfxFlshCntl	
		Default Value: 0b	
		Access: WO	
		Access type of this register is WO. A write to this bit flushes the Gfx TLB in GUNIT. The data associated with the write is discarded and a read return all 0s.	



GMBUS0

GMBUS0			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	C5100h-C5103h		
Name:	GMBUS0 Clock/Port Select		
ShortName:	GMBUS0		
Power:	PG1		
Reset:	global		
This register controls the clock rate of the serial bus and the device the controller is connected to. This register should be configured before the first data valid bit is set.			
DWord	Bit	Description	
0	31:12	Reserved	
		Format: MBZ	
	11	Reserved	
	10:8	GMBUS Rate Select This field selects the rate that the GMBUS will run at. It also defines the AC timing parameters used.	
		ValueName	
		000b100 KHz	
		001b50 KHz	
		OthersReserved	
		Restriction	
		Restriction : It should only be changed between transfers when the GMBUS is idle.	
		7	Reserved
	Format: MBZ		
	6	Reserved	
		Format: MBZ	
	6	Reserved	
		Format: MBZ	
5:3	Reserved		
	Format: MBZ		

**GMBUS0**

2:0

Pin Pair Select

This field selects a GMBUS pin pair for use in the GMBUS communication.

See the table at the beginning of this section to determine which pin pairs are supported and their intended functions.

Value	Name
000b	None (Disabled)
001b	Pin Pair 1
010b	Pin Pair 2
011b	Pin Pair 3



GMBUS1

GMBUS1				
Register Space:	MMIO: 0/2/0			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W Protect			
Size (in bits):	32			
Address:	C5104h-C5107h			
Name:	GMBUS1 Command/Status			
ShortName:	GMBUS1			
Power:	PG1			
Reset:	global			
This register indicates the slave device address, register index, and when the data write is complete. When the SW_CLR_INT bit is asserted, all writes to the GMBUS2, GMBUS3, and GMBUS4 registers are discarded. The GMBUS1 register writes to any other bit except the SW_CLR_INT are also lost. Reads to these registers always work normally, regardless of the state of the SW_CLR_INT bit.				
DWord	Bit	Description		
0	31	Software Clear Interrupt		
		Access:	R/W	
		(SW_CLR_INT) This bit must be clear for normal operation. Setting the bit then clearing it acts as local reset to the GMBUS controller.		
		This bit is commonly used by software to clear a BUS_ERROR when a slave device delivers a NACK.		
		Value	Name	Description
		0b	Clear HW_RDY	If this bit is written as a zero when its current state is a one, will clear the HW_RDY bit and allows register writes to be accepted to the GMBUS registers (Write Protect Off). This bit is cleared to zero when an event causes the HW_RDY bit transition to occur.
		1b	Assert HW_RDY	Asserted by software after servicing the GMBUS interrupt. Setting this bit causes the INT status bit to be cleared and asserts the HW_RDY bit (until this bit is written with a 0). When this bit is set, no writes to GMBUS registers will cause the contents to change with the exception of this bit which can be written.
		30	Software Ready	
			(SW_RDY) Data handshake bit used in conjunction with HW_RDY bit.	
			Value	Name
0b	De-Assert		De-asserted via the assertion event for HW_RDY bit	
1b	SW Assert		When asserted by software, results in de-assertion of HW_RDY bit	



GMBUS1

29 Enable Timeout

(ENT) Enables timeout for slave response.

When this bit is enabled and the slave device response has exceeded the timeout period, the GMBUS Slave Stall Timeout Error interrupt bit is set.

Value	Name
0b	Disable
1b	Enable

28 Reserved

Format: MBZ

27:25 Bus Cycle Select

GMBUS cycle will always consist of a START followed by Slave Address, followed by an optional read or write data phase.

A read cycle with an index will consist of a START followed by a Slave Address a WRITE indication and the INDEX and then a RESTART with a Slave Address and an optional read data phase.

The GMBUS cycle will terminate either with a STOP or by entering a wait state. The WAIT state is exited by generating a STOP or by starting another GMBUS cycle.

This can only cause a STOP to be generated if a GMBUS cycle is generated, the GMBUS is currently in a data phase, or it is in a WAIT phase.

The three bits can be decoded as follows:

27 = STOP generated

26 = INDEX used

25 = Cycle ends in a WAIT

Value	Name	Description
000b	No cycle	No GMBUS cycle is generated
001b	No Index, No Stop, Wait	GMBUS cycle is generated without an INDEX, with no STOP, and ends with a WAIT
010b	Reserved	Reserved
011b	Index, No Stop, Wait	GMBUS cycle is generated with an INDEX, with no STOP, and ends with a WAIT
100b	Gen Stop	Generates a STOP if currently in a WAIT or after the completion of the current byte if active
101b	No Index, Stop	GMBUS cycle is generated without an INDEX and with a STOP
110b	Reserved	Reserved
111b	Index, Stop	GMBUS cycle is generated with an INDEX and with a STOP

24:16 Total Byte Count

This determines the total number of bytes to be transferred during the DATA phase of a GMBUS cycle.

The DATA phase can be prematurely terminated by generating a STOP while in the DATA phase (see Bus Cycle Select).

Restriction



GMBUS1													
	Restriction : Do not change the value of this field during GMBUS cycles transactions. The byte count must not be zero.												
15:8	8 bit Slave Register Index (INDEX) This field specifies the 8-bits of index to be used for the generated bus write transaction or the index used for the WRITE portion of the WRITE/READ pair. It only has an effect if the enable Index bit is set. Restriction Restriction : Do not change the value of this field during GMBUS cycles transactions.												
7:0	Slave Address And Direction Bits 7:1 = 7-bit GMBUS Slave Address: When a GMBUS cycle is to be generated using the Bus Cycle Select field, this field specifies the value of the slave address that is to be sent out. Bit 0 = Slave Direction Bit: When a GMBUS cycle is to be generated based on the Bus Cycle Select, this bit determines if the operation will be a read or a write. A read operation with the index enabled will perform a write with just the index followed by a re-start and a read. A 1 indicates that a Read from the slave device operation is to be performed. A 0 indicates that a Write to the slave device operation is to be performed. <table> <tr> <th>Value</th><th>Name</th></tr> <tr> <td>00000001b</td><td>General Call Address</td></tr> <tr> <td>00000000b</td><td>Start Byte</td></tr> <tr> <td>0000001Xb</td><td>CBUS Address</td></tr> <tr> <td>11110XXXb</td><td>10-Bit Addressing</td></tr> <tr> <td>Others</td><td>Reserved</td></tr> </table> Programming Notes For 10-bit slave address devices, set this field to 11110XXb (where the last two bits (XX) are the two MSBs of the 10-bit address) and the slave direction bit to a write, and set the first data byte to be the 8 LSBs of the 10-bit address.	Value	Name	00000001b	General Call Address	00000000b	Start Byte	0000001Xb	CBUS Address	11110XXXb	10-Bit Addressing	Others	Reserved
Value	Name												
00000001b	General Call Address												
00000000b	Start Byte												
0000001Xb	CBUS Address												
11110XXXb	10-Bit Addressing												
Others	Reserved												



GMBUS2

GMBUS2										
Register Space:	MMIO: 0/2/0									
Source:	BSpec									
Default Value:	0x00000800									
Access:	R/W Protect									
Size (in bits):	32									
Address:	C5108h-C510Bh									
Name:	GMBUS2 Status									
ShortName:	GMBUS2									
Power:	PG1									
Reset:	global									
When the SW_CLR_INT bit is asserted, all writes to this register are discarded. Reads to this register always work normally regardless of the state of the SW_CLR_INT bit.										
DWord	Bit	Description								
0	31:16	Reserved								
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ						
	Format:	MBZ								
	15	INUSE Software wishing to arbitrate for the GMBUS resource can poll this bit until it reads a zero and will then own usage of the GMBUS controller. This bit has no effect on the hardware, and is only used as semaphore among various independent software threads.								
	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0b</td><td>GMBUS is Acquired</td><td>Reading a 0 indicates that GMBUS is now acquired and subsequent reads will now have this bit set. Writing a 0 has no effect.</td></tr><tr><td>1b</td><td>GMBUS in Use</td><td>Reading a 1 indicates that GMBUS is currently allocated to someone else and "In use". Writing a 1 indicates that the software has relinquished the GMBUS resource, which will reset the value to a 0.</td></tr></table>	Value	Name	Description	0b	GMBUS is Acquired	Reading a 0 indicates that GMBUS is now acquired and subsequent reads will now have this bit set. Writing a 0 has no effect.	1b	GMBUS in Use	Reading a 1 indicates that GMBUS is currently allocated to someone else and "In use". Writing a 1 indicates that the software has relinquished the GMBUS resource, which will reset the value to a 0.
Value	Name	Description								
0b	GMBUS is Acquired	Reading a 0 indicates that GMBUS is now acquired and subsequent reads will now have this bit set. Writing a 0 has no effect.								
1b	GMBUS in Use	Reading a 1 indicates that GMBUS is currently allocated to someone else and "In use". Writing a 1 indicates that the software has relinquished the GMBUS resource, which will reset the value to a 0.								
	14	Hardware Wait Phase								
		<table><tr><td>Access:</td><td>RO</td></tr></table>	Access:	RO						
	Access:	RO								
		Once in a WAIT_PHASE, the software can now choose to generate a STOP cycle or a repeated start (RESTART) cycle followed by another GMBUS transaction. Wait phase is entered at the end of the current transaction when that transaction is selected not to terminate with a STOP.								
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Not in a wait phase</td></tr><tr><td>1b</td><td>In wait phase</td></tr></table>	Value	Name	0b	Not in a wait phase	1b	In wait phase			
Value	Name									
0b	Not in a wait phase									
1b	In wait phase									



GMBUS2

GMBUS2			
13	Slave Stall Timeout Error		
	Access:		RO
	This bit indicates that a slave stall timeout has occurred. It is tied to the Enable Timeout (ENT) bit.		
	Value	Name	
	0b	No Slave Timeout	
1b	Slave Timeout		
12	GMBUS Interrupt Status		
	Access:		RO
	This bit indicates that an event that causes a GMBUS interrupt has occurred. The interrupt can be caused by one of the interrupt types enabled in the GMBUS4 register.		
	Value	Name	
	0b	No Interrupt	
1b	Interrupt		
11	Hardware Ready		
	Access:		RO
	(HW_RDY) This provides a method of detecting when software can proceed with the next step in a sequence of GMBUS operations.		
	This data handshake bit is used in conjunction with the SW_RDY bit.		
	When this bit is asserted by the GMBUS controller, it results in the de-assertion of the SW_RDY bit.		
	This bit resumes to normal operation when the SW_CLR_INT bit is written to a 0.		
	Value	Name	Description
	0b	0	Condition required for assertion has not occurred, or when this bit is a one and: - SW_RDY bit has been asserted - During a GMBUS read transaction, after the each read of the data register - During a GMBUS write transaction, after each write of the data register - SW_CLR_INT bit has been cleared
	1b	1 [Default]	This bit is asserted under the following conditions: - After a reset or when the transaction is aborted by the setting of the SW_CLR_INT bit - When an active GMBUS cycle has terminated with a STOP - When during a GMBUS write transaction, the data register needs and can accept another four bytes of data - During a GMBUS read transaction, this bit is asserted when the data register has four bytes of new data or the read transaction DATA phase is complete and the data register contains the last few bytes of the read data



GMBUS2		
10	NAK Indicator	
	Access:	RO
	MAK is indicated by hardware if any expected device acknowledge is not received from the slave within the timeout.	
	Value	Name
	0b	No bus error
9	GMBUS Active	
	Access:	RO
	This is a status bit that indicates whether the GMBUS controller is in an IDLE state or not. Active states are the START, ADDRESS, INDEX, DATA, WAIT, or STOP Phase.	
	Value	Name
	0b	Idle
8:0	Current Byte Count	
	Access:	RO
	Can be used to determine the number of bytes currently transmitted/received by the GMBUS controller hardware.	
	Hardware sets it to zero at the start of a GMBUS transaction data transfer and increments it after the completion of each byte of the data phase.	
	Restriction	
Restriction: Because reads have internal storage, the byte count on a read operation may be ahead of the data that has been accepted from the data register.		



GMBUS3

GMBUS3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W Protect	
Size (in bits):	32	
Double Buffer	HW_RDY	
Update Point:		
Address:	C510Ch-C510Fh	
Name:	GMBUS3 Data Buffer	
ShortName:	GMBUS3	
Power:	PG1	
Reset:	global	
This is the data read/write register. This register is double buffered. Bit 0 is the first bit sent or read, bit 7 is the 8th bit sent or read, all the way through bit 31 being the 32nd bit sent or read. For GMBUS write operations with a non-zero byte count, this register should be written with the data before the GMBUS cycle is initiated. For byte counts that are greater than four bytes, this register will be written with subsequent data only after the HW_RDY status bit is set indicating that the register is now ready for additional data. When the SW_CLR_INT bit is asserted, all writes to this register are discarded. For GMBUS read operations, software should wait until the HW_RDY bit indicates that the register contains the next set of valid read data before reading this register.		
DWord	Bit	Description
0	31:24	Data Byte 3
	23:16	Data Byte 2
	15:8	Data Byte 1
	7:0	Data Byte 0



GMBUS4

GMBUS4																							
Register Space:	MMIO: 0/2/0																						
Source:	BSpec																						
Default Value:	0x00000000																						
Access:	R/W Protect																						
Size (in bits):	32																						
Address:	C5110h-C5113h																						
Name:	GMBUS4 Interrupt Mask																						
ShortName:	GMBUS4																						
Power:	PG1																						
Reset:	global																						
When the SW_CLR_INT bit is asserted, all writes to this register are discarded. Reads to this register always work normally regardless of the state of the SW_CLR_INT bit.																							
DWord	Bit	Description																					
0	31:5	Reserved <table border="1"><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ																			
	Format:	MBZ																					
4:0	Interrupt Mask This field specifies which GMBUS interrupts events may contribute to the setting of GMBUS interrupt status bit in the second level interrupt status register. For writes, the HW Ready interrupt indicates that software can write the next DWORD. It does NOT mean that the transfer of data to the slave device has completed. The HW Ready interrupt may be used for gmbus write cycles only to detect when to write the next DWORD after the first two DWORDs have been written to GMBUS3. The IDLE or HW wait interrupt may be used to detect the end of writing data to the slave device. For reads, the HWRDY interrupt indicates the arrival of the next dword. <table border="1"><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0XXXXb</td><td>Slave Stall Timeout Interrupt Disable</td></tr><tr><td>1XXXXb</td><td>Slave Stall Timeout Interrupt Enable</td></tr><tr><td>X0XXXb</td><td>NAK Interrupt Disable</td></tr><tr><td>X1XXXb</td><td>NAK Interrupt Enable</td></tr><tr><td>XX0XXb</td><td>Idle Interrupt Disable</td></tr><tr><td>XX1XXb</td><td>Idle Interrupt Enable</td></tr><tr><td>XXX0Xb</td><td>HW Wait Interrupt (cycle without a stop has completed) Disable</td></tr><tr><td>XXX1Xb</td><td>HW Wait Interrupt (cycle without a stop has completed) Enable</td></tr><tr><td>XXXX0b</td><td>HW Ready (Data transferred) Interrupt Disable</td></tr><tr><td>XXXX1b</td><td>HW Ready (Data transferred) Interrupt Enable</td></tr></tbody></table>	Value	Name	0XXXXb	Slave Stall Timeout Interrupt Disable	1XXXXb	Slave Stall Timeout Interrupt Enable	X0XXXb	NAK Interrupt Disable	X1XXXb	NAK Interrupt Enable	XX0XXb	Idle Interrupt Disable	XX1XXb	Idle Interrupt Enable	XXX0Xb	HW Wait Interrupt (cycle without a stop has completed) Disable	XXX1Xb	HW Wait Interrupt (cycle without a stop has completed) Enable	XXXX0b	HW Ready (Data transferred) Interrupt Disable	XXXX1b	HW Ready (Data transferred) Interrupt Enable
Value	Name																						
0XXXXb	Slave Stall Timeout Interrupt Disable																						
1XXXXb	Slave Stall Timeout Interrupt Enable																						
X0XXXb	NAK Interrupt Disable																						
X1XXXb	NAK Interrupt Enable																						
XX0XXb	Idle Interrupt Disable																						
XX1XXb	Idle Interrupt Enable																						
XXX0Xb	HW Wait Interrupt (cycle without a stop has completed) Disable																						
XXX1Xb	HW Wait Interrupt (cycle without a stop has completed) Enable																						
XXXX0b	HW Ready (Data transferred) Interrupt Disable																						
XXXX1b	HW Ready (Data transferred) Interrupt Enable																						



GMBUS5

GMBUS5		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	C5120h-C5123h	
Name:	GMBUS5 2 Byte Index	
ShortName:	GMBUS5	
Power:	PG1	
Reset:	global	
This register provides a method for the software indicate to the GMBUS controller the 2 byte device index.		
DWord	Bit	Description
0	31	2 Byte Index Enable When this bit is set to 1, then bits 15:0 are used as the index. Bits 15:8 are used in the first byte which is the most significant index bits. The slave index in the GMBUS1<15:8> are ignored. Bits 7:0 are used in the second byte which is the least significant index bits.
	30:16	Reserved
		Format:
15:0	2 Byte Slave Index This is the 2 byte index used in all GMBUS accesses when 2 Byte Index Enable is set to 1.	



GMCH Graphics Control

GGC_0_0_0_PCI - GMCH Graphics Control			
Register Space:	PCI: 0/0/0		
Source:	BSpec		
Default Value:	0x00000500		
Size (in bits):	16		
Address:	00050h		
GMCH Graphics Control Register.			
DWord	Bit	Description	
0	15:8	Graphics Mode Select	
		Default Value:	00000101b
		Access:	R/W Lock
		This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.	
		BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.	
		BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions.	
		00h:0MB	
		01h:32MB	
		02h:64MB	
		03h:96MB	
04h:128MB			
05h:160MB (default)			
06h:192MB			
07h:224MB			
08h:256MB			
09h:288MB			
0Ah:320MB			
0Bh:352MB			
0Ch:384MB			
0Dh:416MB			
0Eh:448MB			
0Fh:480MB			
10h:512MB			
11h - 1Fh: Reserved			
20h:1024MB			
21h - 2Fh: Reserved			
30h:1536MB			
31h - 3Fh: Reserved			
40h: 2048MB			



GGC_0_0_0_PCI - GMCH Graphics Control

GGC_0_0_0_PCI - GMCH Graphics Control		
		41h - EFh: Reserved F0h: 4MB F1h: 8MB F2h: 12MB F3h: 16MB F4h: 20MB F5h: 24MB F6h: 28MB F7h: 32MB F8h: 36MB F9h: 40MB FAh: 44MB FBh: 48MB FCh: 52MB FDh: 56MB FEh: 60MB FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.
7:6	GTT Graphics Memory Size	
	Default Value:	00b
	Access:	R/W Lock
	This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. 0x0: No Preallocated Memory 0x1: 2MB of Preallocated Memory 0x2: 4MB of Preallocated Memory 0x3: 8MB of Preallocated Memory	
5:3	RESERVED	
	Default Value:	000b
	Access:	RO
	Reserved	
2	Versatile Acceleration Mode Enable	
	Default Value:	0b
	Access:	R/W Lock
	Enables the use of the iGFX engines for Versatile Acceleration. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.	

**GGC_0_0_0_PCI - GMCH Graphics Control**

GGC_0_0_0_PCI - GMCH Graphics Control			
		1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h.	
	1	IGD VGA Disable	
		Default Value:	0b
		Access:	R/W Lock
		0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0).	
	0	GGC Lock	
		Default Value:	0b
		Access:	R/W Key Lock
		When set to 1b, this bit will lock all bits in this register.	



GPIO_CTL

GPIO_CTL			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000808		
Access:	R/W		
Size (in bits):	32		
Address:	C5014h-C5017h		
Name:	GPIO Control 1		
ShortName:	GPIO_CTL_1		
Power:	PG1		
Reset:	global		
Address:	C5018h-C501Bh		
Name:	GPIO Control 2		
ShortName:	GPIO_CTL_2		
Power:	PG1		
Reset:	global		
Address:	C501Ch-C501Fh		
Name:	GPIO Control 3		
ShortName:	GPIO_CTL_3		
Power:	PG1		
Reset:	global		
The register controls a pair of pins that can be used for general purpose control, but usually is designated for specific functions according to the requirements of the device and the system that the device is in. Each pin of the two pin pair is designated as a clock or data for descriptive purposes. See the table at the beginning of this section to determine which pin pairs are supported and their intended functions. Board design variations are possible and would affect the usage of these pins. There are multiple instances of this register to support each of the GPIO pin pairs.			
DWord	Bit	Description	
0	31:13	Reserved	
		Format: MBZ	
	12	GPIO Data In	
		Default Value:	Ub Undefined (read only, depends on I/O pin)
		Access:	RO
This is the value that is sampled on the GPIO_Data pin as an input.			



GPIO_CTL		
11	GPIO Data Value	
	Default Value:	1b
	Access:	R/W
	This is the value that should be place on the GPIO Data pin as an output. This value is only written into the register if GPIO DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Data DIRECTION VALUE contains a value that will configure the pin as an output. The default of '1' mimics the I2C external pull-ups.	
10	GPIO Data Mask	
	Access:	WO
	This is a mask bit to determine whether the GPIO DATA VALUE bit should be written into the register.	
	Value	Name
	0b	Dot not write
9	GPIO Data Direction Value	
	Access:	R/W
	This is the value that should be used to define the output enable of the GPIO Data pin. This value is only written into the register if GPIO Data DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO DATA VALUE bit.	
	Value	Name
	0b	Input
8	GPIO Data Direction Mask	
	Access:	WO
	This is a mask bit to determine whether the GPIO Data DIRECTION VALUE bit should be written into the register.	
	Value	Name
	0b	Dot not write
7:5	Reserved	
	Format:	MBZ
4	GPIO Clock Data In	
	Default Value:	Ub Undefined (read only, depends on I/O pin)
	Access:	RO
This is the value that is sampled on the GPIO Clock pin as an input.		



GPIO_CTL

3	GPIO Clock Data Value <table><tr><td>Default Value:</td><td>1b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This is the value that should be place on the GPIO Clk pin as an output. This value is only written into the register if GPIO Clock DATA MASK is also asserted. The value will appear on the pin if this data value is actually written to this register and the GPIO Clock DIRECTION VALUE contains a value that will configure the pin as an output. The default of '1' mimics the I2C external pull-ups.	Default Value:	1b	Access:	R/W				
Default Value:	1b								
Access:	R/W								
2	GPIO Clock Data Mask <table><tr><td>Access:</td><td>WO</td></tr></table> This is a mask bit to determine whether the GPIO Clock DATA VALUE bit should be written into the register. <table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Dot not write</td></tr><tr><td>1b</td><td>Write</td></tr></table>	Access:	WO	Value	Name	0b	Dot not write	1b	Write
Access:	WO								
Value	Name								
0b	Dot not write								
1b	Write								
1	GPIO Clock Direction Value <table><tr><td>Access:</td><td>R/W</td></tr></table> This is the value that should be used to define the output enable of the GPIO Clock pin. This value is only written into the register if GPIO Clock DIRECTION MASK is also asserted. The value that will appear on the pin is defined by what is in the register for the GPIO Clock DATA VALUE bit. <table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Input</td></tr><tr><td>1b</td><td>Output</td></tr></table>	Access:	R/W	Value	Name	0b	Input	1b	Output
Access:	R/W								
Value	Name								
0b	Input								
1b	Output								
0	GPIO Clock Direction Mask <table><tr><td>Access:</td><td>WO</td></tr></table> This is a mask bit to determine whether the GPIO Clock DIRECTION VALUE bit should be written into the register. <table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Dot not write</td></tr><tr><td>1b</td><td>Write</td></tr></table>	Access:	WO	Value	Name	0b	Dot not write	1b	Write
Access:	WO								
Value	Name								
0b	Dot not write								
1b	Write								



Graphics Memory Range Address

GMADR_0_2_0_PCI - Graphics Memory Range Address			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x0000000C, 0x00000000		
Size (in bits):	64		
Address:	00018h		
GMADR is the PCI aperture used by S/W to access tiled GFX surfaces in a linear fashion.			
DWord	Bit	Description	
0	63:39	Reserved for Memory Base Address	
		Default Value:	0000000000000000000000000000b
		Access:	R/W
		Must be set to 0 since addressing above 512GB is not supported.	
	38:32	Memory Base Address	
		Default Value:	0000000b
		Access:	R/W
		Set by the OS, these bits correspond to address signals [38:32].	
	31	4096 MB Address Mask	
		Default Value:	0b
		Access:	R/W Lock
		This bit is either part of the Memory Base Address (R/W) or part of Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 4096MB. (i.e. MSAC.APSZ[4]=1)	
	30	2048 MB Address Mask	
		Default Value:	0b
		Access:	R/W Lock
		This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 2048MB. (i.e. MSAC.APSZ[3]=1)	
29	1024 MB Address Mask		
	Default Value:	0b	
	Access:	R/W Lock	
	This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 1024MB. (i.e. MSAC.APSZ[2]=1)		



GMADR_0_2_0_PCI - Graphics Memory Range Address

	28	512MB Address Mask	
		Default Value:	0b
		Access:	R/W Lock
		This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 512MB. (i.e. MSAC.APSZ[1]=1)	
	27	256 MB Address Mask	
		Default Value:	0b
		Access:	R/W Lock
		This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO) depending on the value of MSAC.APSZ. RO and forced to 0 when MSAC.APSZ >= 256MB. (i.e. MSAC.APSZ[0]=1)	
	26:4	Address Mask	
		Default Value:	000000000000000000000000b
		Access:	RO
		Hardwired to 0s to indicate at least 128MB address range.	
	3	Prefetchable Memory	
		Default Value:	1b
		Access:	RO
		Hardwired to 1 to enable prefetching.	
	2:1	Memory Type	
		Default Value:	10b
		Access:	RO
		Hardwired to 2h to indicate 64 bit base address.	
	0	Memory/IO Space	
		Default Value:	0b
		Access:	RO
		Hardwired to 0 to indicate memory space.	



Graphics MOCS Register0

GFX_MOCS_0 - Graphics MOCS Register0			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000030	
Size (in bits):		32	
Address:		0C800h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target		



GFX_MOCS_0 - Graphics MOCS Register0

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2,1, or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	00b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register1

GFX_MOCS_1 - Graphics MOCS Register1			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000034		
Size (in bits):	32		
Address:	0C804h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	



GFX_MOCS_1 - Graphics MOCS Register1

	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2,1, or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
	3:2	Target Cache	
		Default Value:	01b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register2

GFX_MOCS_2 - Graphics MOCS Register2			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000038		
Size (in bits):	32		
Address:	0C808h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target		



GFX_MOCS_2 - Graphics MOCS Register2

GFX_MOCS_2 - Graphics MOCS Register2		
		Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2,1, or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	10b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**GFX_MOCS_2 - Graphics MOCS Register2**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register3

GFX_MOCS_3 - Graphics MOCS Register3			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000031		
Size (in bits):	32		
Address:	0C80Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target		

**GFX_MOCS_3 - Graphics MOCS Register3**

		Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_3 - Graphics MOCS Register3		
	1:0	LLC/eDRAM cacheability control
		Default Value: 01b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register4

GFX_MOCS_4 - Graphics MOCS Register4			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0C810h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target		



GFX_MOCS_4 - Graphics MOCS Register4

GFX_MOCS_4 - Graphics MOCS Register4		
		Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**GFX_MOCS_4 - Graphics MOCS Register4**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register5

GFX_MOCS_5 - Graphics MOCS Register5			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0C814h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_5 - Graphics MOCS Register5**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_5 - Graphics MOCS Register5		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register6

GFX_MOCS_6 - Graphics MOCS Register6			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0C818h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	



GFX_MOCS_6 - Graphics MOCS Register6

	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	

**GFX_MOCS_6 - Graphics MOCS Register6**

	3:2	Target Cache	
		Default Value:	10b
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register7

GFX_MOCS_7 - Graphics MOCS Register7			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000033		
Size (in bits):	32		
Address:	0C81Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**GFX_MOCS_7 - Graphics MOCS Register7**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_7 - Graphics MOCS Register7		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register8

GFX_MOCS_8 - Graphics MOCS Register8			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000037	
Size (in bits):		32	
Address:		0C820h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		



GFX_MOCS_8 - Graphics MOCS Register8

	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	

**GFX_MOCS_8 - Graphics MOCS Register8**

GFX_MOCS_8 - Graphics MOCS Register8		
3:2	Target Cache	
	Default Value:	01b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
1:0	LLC/eDRAM cacheability control	
	Default Value:	11b
	Access:	R/W
	Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register9

GFX_MOCS_9 - Graphics MOCS Register9			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003B		
Size (in bits):	32		
Address:	0C824h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_9 - Graphics MOCS Register9**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_9 - Graphics MOCS Register9		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register10

GFX_MOCS_10 - Graphics MOCS Register10			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0C828h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	



GFX_MOCS_10 - Graphics MOCS Register10

	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	

**GFX_MOCS_10 - Graphics MOCS Register10**

GFX_MOCS_10 - Graphics MOCS Register10		
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
1:0	LLC/eDRAM cacheability control	
	Default Value:	10b
	Access:	R/W
	Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register11

GFX_MOCS_11 - Graphics MOCS Register11			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0C82Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_11 - Graphics MOCS Register11**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_11 - Graphics MOCS Register11		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register12

GFX_MOCS_12 - Graphics MOCS Register12			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0C830h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	



GFX_MOCS_12 - Graphics MOCS Register12

	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
	7	Enable Skip Caching	
		Default Value:	0b
		Access:	R/W
		Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
	6	Dont allocate on miss	
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
	5:4	LRU management	
		Default Value:	11b
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	

**GFX_MOCS_12 - Graphics MOCS Register12**

GFX_MOCS_12 - Graphics MOCS Register12		
3:2	Target Cache	
	Default Value:	10b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
1:0	LLC/eDRAM cacheability control	
	Default Value:	10b
	Access:	R/W
	Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register13

GFX_MOCS_13 - Graphics MOCS Register13			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000033			
Size (in bits): 32			
Address: 0C834h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_13 - Graphics MOCS Register13**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_13 - Graphics MOCS Register13		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register14

GFX_MOCS_14 - Graphics MOCS Register14			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000037	
Size (in bits):		32	
Address:		0C838h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_14 - Graphics MOCS Register14

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**GFX_MOCS_14 - Graphics MOCS Register14**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register15

GFX_MOCS_15 - Graphics MOCS Register15			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003B		
Size (in bits):	32		
Address:	0C83Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_15 - Graphics MOCS Register15**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_15 - Graphics MOCS Register15		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register16

GFX_MOCS_16 - Graphics MOCS Register16			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000030	
Size (in bits):		32	
Address:		0C840h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_16 - Graphics MOCS Register16

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		Default Value:	11b	Access:	R/W
Default Value:	11b					
Access:	R/W					
3:2	Target Cache <table><tr><td>Default Value:</td><td>00b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		Default Value:	00b	Access:	R/W
Default Value:	00b					
Access:	R/W					

**GFX_MOCS_16 - Graphics MOCS Register16**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register17

GFX_MOCS_17 - Graphics MOCS Register17			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000034		
Size (in bits):	32		
Address:	0C844h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_17 - Graphics MOCS Register17**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_17 - Graphics MOCS Register17		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register18

GFX_MOCS_18 - Graphics MOCS Register18			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000038	
Size (in bits):		32	
Address:		0C848h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_18 - Graphics MOCS Register18

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**GFX_MOCS_18 - Graphics MOCS Register18**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register19

GFX_MOCS_19 - Graphics MOCS Register19			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000031		
Size (in bits):	32		
Address:	0C84Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**GFX_MOCS_19 - Graphics MOCS Register19**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_19 - Graphics MOCS Register19		
	1:0	LLC/eDRAM cacheability control
		Default Value: 01b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register20

GFX_MOCS_20 - Graphics MOCS Register20			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0C850h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
Access:		R/W	
This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved			
10:8	Skip Caching control		
	Default Value:	000b	
	Access:	R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		



GFX_MOCS_20 - Graphics MOCS Register20

GFX_MOCS_20 - Graphics MOCS Register20		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**GFX_MOCS_20 - Graphics MOCS Register20**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register21

GFX_MOCS_21 - Graphics MOCS Register21			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0C854h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_21 - Graphics MOCS Register21**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_21 - Graphics MOCS Register21		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register22

GFX_MOCS_22 - Graphics MOCS Register22			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0C858h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_22 - Graphics MOCS Register22

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**GFX_MOCS_22 - Graphics MOCS Register22**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register23

GFX_MOCS_23 - Graphics MOCS Register23			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000033		
Size (in bits):	32		
Address:	0C85Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_23 - Graphics MOCS Register23**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_23 - Graphics MOCS Register23		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register24

GFX_MOCS_24 - Graphics MOCS Register24			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000037	
Size (in bits):		32	
Address:		0C860h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_24 - Graphics MOCS Register24

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		Default Value:	11b	Access:	R/W
Default Value:	11b					
Access:	R/W					
3:2	Target Cache <table><tr><td>Default Value:</td><td>01b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		Default Value:	01b	Access:	R/W
Default Value:	01b					
Access:	R/W					

**GFX_MOCS_24 - Graphics MOCS Register24**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register25

GFX_MOCS_25 - Graphics MOCS Register25			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003B		
Size (in bits):	32		
Address:	0C864h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_25 - Graphics MOCS Register25**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_25 - Graphics MOCS Register25		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register26

GFX_MOCS_26 - Graphics MOCS Register26			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0C868h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
Access: R/W			
This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved			
10:8	Skip Caching control		
	Default Value: 000b		
	Access: R/W		
Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care			



GFX_MOCS_26 - Graphics MOCS Register26

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**GFX_MOCS_26 - Graphics MOCS Register26**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register27

GFX_MOCS_27 - Graphics MOCS Register27			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0C86Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_27 - Graphics MOCS Register27**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_27 - Graphics MOCS Register27		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register28

GFX_MOCS_28 - Graphics MOCS Register28			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0C870h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_28 - Graphics MOCS Register28

GFX_MOCS_28 - Graphics MOCS Register28		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	10b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**GFX_MOCS_28 - Graphics MOCS Register28**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register29

GFX_MOCS_29 - Graphics MOCS Register29			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000033		
Size (in bits):	32		
Address:	0C874h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_29 - Graphics MOCS Register29**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_29 - Graphics MOCS Register29		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register30

GFX_MOCS_30 - Graphics MOCS Register30			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000037			
Size (in bits): 32			
Address: 0C878h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_30 - Graphics MOCS Register30

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target					
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved			Default Value:	11b	Access:	R/W
Default Value:	11b						
Access:	R/W						
3:2	Target Cache <table><tr><td>Default Value:</td><td>01b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed			Default Value:	01b	Access:	R/W
Default Value:	01b						
Access:	R/W						



GFX_MOCS_30 - Graphics MOCS Register30		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register31

GFX_MOCS_31 - Graphics MOCS Register31			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0C87Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_31 - Graphics MOCS Register31**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_31 - Graphics MOCS Register31		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register32

GFX_MOCS_32 - Graphics MOCS Register32			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000030	
Size (in bits):		32	
Address:		0C880h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_32 - Graphics MOCS Register32

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**GFX_MOCS_32 - Graphics MOCS Register32**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register33

GFX_MOCS_33 - Graphics MOCS Register33			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000034			
Size (in bits): 32			
Address: 0C884h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_33 - Graphics MOCS Register33**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_33 - Graphics MOCS Register33		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register34

GFX_MOCS_34 - Graphics MOCS Register34			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000038	
Size (in bits):		32	
Address:		0C888h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_34 - Graphics MOCS Register34

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target					
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved			Default Value:	11b	Access:	R/W
Default Value:	11b						
Access:	R/W						
3:2	Target Cache <table><tr><td>Default Value:</td><td>10b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed			Default Value:	10b	Access:	R/W
Default Value:	10b						
Access:	R/W						

**GFX_MOCS_34 - Graphics MOCS Register34**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register35

GFX_MOCS_35 - Graphics MOCS Register35			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000031		
Size (in bits):	32		
Address:	0C88Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_35 - Graphics MOCS Register35**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_35 - Graphics MOCS Register35		
	1:0	LLC/eDRAM cacheability control
		Default Value: 01b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register36

GFX_MOCS_36 - Graphics MOCS Register36			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0C890h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_36 - Graphics MOCS Register36

	Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	Dont allocate on miss Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	LRU management Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	Target Cache Default Value: 00b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

**GFX_MOCS_36 - Graphics MOCS Register36**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register37

GFX_MOCS_37 - Graphics MOCS Register37			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0C894h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_37 - Graphics MOCS Register37**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_37 - Graphics MOCS Register37		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register38

GFX_MOCS_38 - Graphics MOCS Register38			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0C898h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_38 - Graphics MOCS Register38

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**GFX_MOCS_38 - Graphics MOCS Register38**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register39

GFX_MOCS_39 - Graphics MOCS Register39			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000033		
Size (in bits):	32		
Address:	0C89Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_39 - Graphics MOCS Register39**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_39 - Graphics MOCS Register39		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register40

GFX_MOCS_40 - Graphics MOCS Register40			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000037	
Size (in bits):		32	
Address:		0C8A0h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_40 - Graphics MOCS Register40

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target					
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved			Default Value:	11b	Access:	R/W
Default Value:	11b						
Access:	R/W						
3:2	Target Cache <table><tr><td>Default Value:</td><td>01b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed			Default Value:	01b	Access:	R/W
Default Value:	01b						
Access:	R/W						



GFX_MOCS_40 - Graphics MOCS Register40		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register41

GFX_MOCS_41 - Graphics MOCS Register41			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0C8A4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_41 - Graphics MOCS Register41**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_41 - Graphics MOCS Register41		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register42

GFX_MOCS_42 - Graphics MOCS Register42			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0C8A8h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_42 - Graphics MOCS Register42

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target					
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved			Default Value:	11b	Access:	R/W
Default Value:	11b						
Access:	R/W						
3:2	Target Cache <table><tr><td>Default Value:</td><td>00b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed			Default Value:	00b	Access:	R/W
Default Value:	00b						
Access:	R/W						

**GFX_MOCS_42 - Graphics MOCS Register42**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register43

GFX_MOCS_43 - Graphics MOCS Register43			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000036			
Size (in bits): 32			
Address: 0C8ACh			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**GFX_MOCS_43 - Graphics MOCS Register43**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_43 - Graphics MOCS Register43		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register44

GFX_MOCS_44 - Graphics MOCS Register44			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0C8B0h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_44 - Graphics MOCS Register44

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**GFX_MOCS_44 - Graphics MOCS Register44**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register45

GFX_MOCS_45 - Graphics MOCS Register45			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000033		
Size (in bits):	32		
Address:	0C8B4h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**GFX_MOCS_45 - Graphics MOCS Register45**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_45 - Graphics MOCS Register45		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register46

GFX_MOCS_46 - Graphics MOCS Register46			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0C8B8h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_46 - Graphics MOCS Register46

GFX_MOCS_46 - Graphics MOCS Register46		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	01b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**GFX_MOCS_46 - Graphics MOCS Register46**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register47

GFX_MOCS_47 - Graphics MOCS Register47			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003B		
Size (in bits):	32		
Address:	0C8BCh		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_47 - Graphics MOCS Register47**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_47 - Graphics MOCS Register47		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register48

GFX_MOCS_48 - Graphics MOCS Register48			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000030	
Size (in bits):		32	
Address:		0C8C0h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_48 - Graphics MOCS Register48

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**GFX_MOCS_48 - Graphics MOCS Register48**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register49

GFX_MOCS_49 - Graphics MOCS Register49			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000034		
Size (in bits):	32		
Address:	0C8C4h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_49 - Graphics MOCS Register49**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_49 - Graphics MOCS Register49		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register50

GFX_MOCS_50 - Graphics MOCS Register50			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000038	
Size (in bits):		32	
Address:		0C8C8h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_50 - Graphics MOCS Register50

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**GFX_MOCS_50 - Graphics MOCS Register50**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register51

GFX_MOCS_51 - Graphics MOCS Register51			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000031		
Size (in bits):	32		
Address:	0C8CCh		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_51 - Graphics MOCS Register51**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_51 - Graphics MOCS Register51		
	1:0	LLC/eDRAM cacheability control
		Default Value: 01b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register52

GFX_MOCS_52 - Graphics MOCS Register52			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0C8D0h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_52 - Graphics MOCS Register52

GFX_MOCS_52 - Graphics MOCS Register52		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**GFX_MOCS_52 - Graphics MOCS Register52**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register53

GFX_MOCS_53 - Graphics MOCS Register53			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000036			
Size (in bits): 32			
Address: 0C8D4h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_53 - Graphics MOCS Register53**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_53 - Graphics MOCS Register53		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register54

GFX_MOCS_54 - Graphics MOCS Register54			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0C8D8h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_54 - Graphics MOCS Register54

GFX_MOCS_54 - Graphics MOCS Register54		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	10b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**GFX_MOCS_54 - Graphics MOCS Register54**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register55

GFX_MOCS_55 - Graphics MOCS Register55			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0C8DCh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_55 - Graphics MOCS Register55**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_55 - Graphics MOCS Register55		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register56

GFX_MOCS_56 - Graphics MOCS Register56			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0C8E0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_56 - Graphics MOCS Register56

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		Default Value:	11b	Access:	R/W
Default Value:	11b					
Access:	R/W					
3:2	Target Cache <table><tr><td>Default Value:</td><td>01b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		Default Value:	01b	Access:	R/W
Default Value:	01b					
Access:	R/W					

**GFX_MOCS_56 - Graphics MOCS Register56**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register57

GFX_MOCS_57 - Graphics MOCS Register57			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0C8E4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_57 - Graphics MOCS Register57**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_57 - Graphics MOCS Register57		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register58

GFX_MOCS_58 - Graphics MOCS Register58			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0C8E8h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_58 - Graphics MOCS Register58

GFX_MOCS_58 - Graphics MOCS Register58		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**GFX_MOCS_58 - Graphics MOCS Register58**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register59

GFX_MOCS_59 - Graphics MOCS Register59			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0C8ECh		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_59 - Graphics MOCS Register59**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_59 - Graphics MOCS Register59		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register60

GFX_MOCS_60 - Graphics MOCS Register60			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0C8F0h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_60 - Graphics MOCS Register60

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**GFX_MOCS_60 - Graphics MOCS Register60**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register61

GFX_MOCS_61 - Graphics MOCS Register61			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0C8F4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_61 - Graphics MOCS Register61**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_61 - Graphics MOCS Register61		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics MOCS Register62

GFX_MOCS_62 - Graphics MOCS Register62			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0C8F8h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



GFX_MOCS_62 - Graphics MOCS Register62

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target					
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved			Default Value:	11b	Access:	R/W
Default Value:	11b						
Access:	R/W						
3:2	Target Cache <table><tr><td>Default Value:</td><td>01b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed			Default Value:	01b	Access:	R/W
Default Value:	01b						
Access:	R/W						

**GFX_MOCS_62 - Graphics MOCS Register62**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Graphics MOCS Register63

GFX_MOCS_63 - Graphics MOCS Register63			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003B		
Size (in bits):	32		
Address:	0C8FCh		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**GFX_MOCS_63 - Graphics MOCS Register63**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



GFX_MOCS_63 - Graphics MOCS Register63		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Graphics System Event

GSE_0_2_0_PCI - Graphics System Event			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	000E4h		
This register can be accessed by either Byte, Word, or Dword PCI config cycles. A write to this register will cause the Graphics System Event display interrupt if it is enabled and unmasked in the display interrupt registers.			
DWord	Bit	Description	
0	31:24	GSE Scratch Trigger 3	
		Default Value:	00000000b
		Access:	R/W
	23:16	GSE Scratch Trigger 2	
		Default Value:	00000000b
		Access:	R/W
	15:8	GSE Scratch Trigger 1	
		Default Value:	00000000b
		Access:	R/W
	7:0	GSE Scratch Trigger 0	
		Default Value:	00000000b
		Access:	R/W



Graphics Translation Table Memory Mapped Range Address

GTTMMADR_0_2_0_PCI - Graphics Translation Table Memory Mapped Range Address			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x000000004, 0x000000000		
Size (in bits):	64		
Address:	00010h		
This register requests allocation for the combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 2MB of that used by MMIO, 6MB reserved, and 8MB used by GTT. GTTADR will begin at (GTTMMADR + 8 MB) while the MMIO base address will be the same as GTTMMADR. The region between (GTTMMADR + 2MB) - (GTTMMADR + 8MB) is reserved. For the Global GTT, this range is defined as a memory BAR in graphics device config space. It is an alias into which software is required to write Page Table Entry values (PTEs). Software may read PTE values from the global Graphics Translation Table (GTT). PTEs cannot be written directly into the global GTT memory area. The device snoops writes to this region in order to invalidate any cached translations within the various TLB's implemented on-chip. The allocation is for 16MB and the base address is defined by bits [38:24].			
DWord	Bit	Description	
0	63:39	Reserved for Memory Base Address	
		Default Value:	000000000000000000000000b
		Access:	R/W
		Must be set to 0 since addressing above 512GB is not supported.	
	38:24	Memory Base Address	
		Default Value:	0000000000000000b
		Access:	R/W
		Set by the OS, these bits correspond to address signals [38:24].	
	23:4	Address Mask	
		Default Value:	00000000000000000000b
		Access:	RO
		Hardwired to 0s to indicate at least 16MB address range.	
	3	Prefetchable Memory	
		Default Value:	0b
		Access:	RO
		Hardwired to 0 to prevent prefetching.	



GTTMMADR_0_2_0_PCI - Graphics Translation Table Memory Mapped Range Address

	2:1	Memory Type	
		Default Value:	10b
		Access:	RO
		Hardwired to 2h to indicate 64 bit base address.	
	0	Memory/IO Space	
		Default Value:	0b
		Access:	RO
		Hardwired to 0 to indicate memory space.	



GT_FLUSH_BCLD_ACK

GT_FLUSH_BCLD_ACK - GT_FLUSH_BCLD_ACK			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	030C0h		
GT writes a '1' to this bit to acknowledge PRMRR range registers are loaded into GT. This register is a LOCAL CR register and not an MMIO register			
DWord	Bit	Description	
0	31:1	RESERVED	
		Default Value:	00000000h
		Access:	RO
		Reserved	
	0	ACK	
		Default Value:	0b
		Access:	R/W
GT Boot Context Load Ack			



GT_RELOAD_FLUSH

GT_RELOAD_FLUSH - GT_RELOAD_FLUSH			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	030B0h		
Ucode writes a '1' to bits 0 which triggers GT to flush and re-load PRMRR range registers. This register is a LOCAL CR register and not an MMIO register			
DWord	Bit	Description	
0	31:1	RESERVED	
		Default Value:	00000000h
		Access:	RO
		Reserved	
	0	BCLD_REQ	
		Default Value:	0b
		Access:	R/W
GT Boot Context Load Request. Write to this bit will initiate ?Mcheck Complete Routine? (PPPE flow).			



GTACK

GTACK - GTACK		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 120004h		
This register is written to by GT for various device 2 sequencer flows.		
DWord	Bit	Description
0	31:5	RESERVED
		Default Value: 0000000h
		Access: R/W
		Reserved
	4	RTPACK
		Default Value: 0h
		Access: R/W
		GT indicates that the set root table pointer flow is complete from its point of view by writing a 1b to this field. Once SW is notified with the appropriate status bit, this bit is cleared by the HW.
	3	DESCRACK
		Default Value: 0h
		Access: R/W
		GT indicates that the generic descriptor flow is complete from its point of view by writing a 1b to this field Once SW is notified with the appropriate status bit, this bit is cleared by the HW.
	2	VTDACK
		Default Value: 0h
		Access: R/W
		GT indicates that the Translation Enable/Disable or IOTLB Invalidation flow is complete from its point of view by writing a 1b to this field. Once SW is notified with the appropriate status bit, this bit is cleared by the HW.



GTACK - GTACK		
	1	DPRACK
		Default Value: 0h
		Access: R/W
		GT indicates that DPR Update flow is complete from its point of view by writing a 1b to this field. Once SW is notified with the appropriate status bit, this bit is cleared by the HW.
	0	PMRACK
		Default Value: 0h
		Access: R/W
		GT indicates that PMR Enable/Disable flow is complete from its point of view by writing a 1b to this field. Once SW is notified with the appropriate status bit, this bit is cleared by the HW.



GTI PFET control register with lock

PFETCTL - GTI PFET control register with lock		
Register Space:		MMIO: 0/2/0
Source:		BSpec
Default Value:		0x0005000A
Size (in bits):		32
Address:		24008h
DWord	Bit	Description
0	31	PFET Control Lock
		Access: R/W Lock 0 = Bits of GTI PFETCTL register are R/W 1 = All bits of GTI PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:23	Reserved
		Access: RO Reserved
	22	Leave firewall disabled
21		Access: R/W Lock When this bit is set SPC will not firewall the gated domain for a power down flow. But it will pretend to complete the flow with PM. Encodings: 0 = Default mode, that is, firewall gated domain to ungated domain crossing during power down flows 1 = Leave firewall disabled, that is, don't firewall the gated domain, but complete logical flow
		Leave FET On
		Access: R/W Lock When This bit is set SPC will not turn off the PFET eventhough it will complete the flow with PM Encodings: 0 = Default mode, that is, power off fets during power down flows 1 = Leave ON mode, that is, don't power off pfet, but complete logical flow
		Programming Notes
		This bit should be programmed before the powerup sequence is initiated for GTI.
20	Power Well Status	
	Access: R/WC 0 = Well is powered Down 1 = Well is powered Up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.	

**PFETCTL - GTI PFET control register with lock**

	19	Powergood timer error	
		Access:	R/WC
		0 = Well is powered Down 1 = Well is powered Up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.	
	18:16	Delay from enabling secondary PFETs to power good	
		Access:	R/W Lock
		Delay from enabling secondary PFETs to power good 3'b000: BXT - 60ns 3'b001: BXT - 120ns 3'b010: BXT - 240ns 3'b011: BXT - 480ns 3'b100: BXT - 960ns 3'b101: BXT - 1920ns 3'b110: BXT - 3840ns 3'b111: BXT - 7680ns	
		Value	Name
		101b	[Default]
	15:13	Time period last primay pfet strobe to secondary pfet strobe	
		Access:	R/W Lock
		Time period last primary pfet strobe to secondary pfet strobe 3'b000: BXT - 60ns (or 6 bclks) 3'b001: BXT - 120ns (or 12 bclks) 3'b010: BXT - 180ns (or 18 bclks) 3'b111: BXT - 480ns (or 48 bclks)	
	12:10	Time period b/w two adjacent strobes	
		Access:	R/W Lock
		Time period b/w two adjacent strobes to the primary FETs 3'b000: BXT - 60ns (or 6 bclks) 3'b001: BXT - 120ns (or 12 bclks) 3'b010: BXT - 180ns (or 18 bclks) 3'b111: BXT - 480ns (or 48 bclks)	
	9:7	FET setup margin from enable to strobe	
		Access:	R/W Lock
		Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: BXT - 60ns (or 6 bclks) 3'b001: BXT - 120ns (or 12 bclks)	



PFETCTL - GTI PFET control register with lock				
		3'b010: BXT - 180ns (or 18 bclks) 3'b111: BXT - 480ns (or 48 bclks)		
	6:0	Number of flops to enable primary FETs		
		Access:	R/W Lock	
		Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed		
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0001010b</td><td>[Default]</td></tr></table>	Value	Name
Value	Name			
0001010b	[Default]			



GT Mode Register

GT_MODE - GT Mode Register				
Register Space:		MMIO: 0/2/0		
Source:		RenderCS		
Default Value:		0x00000000		
Access:		R/W		
Size (in bits):		32		
Trusted Type:		1		
Address:		07008h		
This Register is used to control the 6EU and 12EU configuration for GT. Writing 0x01FF01FF to this register enables the 6EU mode.				
DWord	Bit	Description		
0	31:16	Mask		
		Access:	WO	
		Format:	Mask[15:0]	
		Must be set to modify corresponding bit in Bits 15:0. (All implemented bits)		
	15	EU Local Thread Checking Enable		
		Access:	r/w	
		This field configures the EU local thread checking. If enable the stateless access will be checked against the local thread's scratch space size and start address.		
		Value	Name	Description
		0h	Disable [Default]	EU local thread checking is disabled.
		1h	Enable	EU local thread checking is enabled.
		Restriction		
		Restriction : BXT configuration do not properly support Per-Thread Scratch Space checking when headerless Data Port messages are used. The workaround is either to disable this control, or not use SFID_DP_DC0 or SFID_DP_DC2 headerless messages.		
		14:13	SFR mode	
			Access:	r/w
Format:	U2			
This field must be zero when not in GT4(SFR) configuration i.e GTB_rendermode fuse set to SFR.				
12:11	Cross Slice Hashing Mode			
	Access:	r/w		
	Format:	U2		



GT_MODE - GT Mode Register

	<table><tr><th>Value</th><th>Name</th><th>Description</th><th>Programming Notes</th></tr><tr><td>0h</td><td>Normal Mode [Default]</td><td>GT3: 16x16 Hashing enabled GT2 or lower modes: No cross slice hashing</td><td></td></tr><tr><td>1h</td><td>Cross Slice Hashing Disable</td><td>Disables the cross slice hashing</td><td></td></tr><tr><td>2h</td><td>32x16 Hahsing</td><td>32x16 Pixel hashing across slices</td><td></td></tr><tr><td>3h</td><td>32X32 hashing</td><td>32X32 pixel hashing across slices</td><td>This setting must be used when sub-slice hashing mode is 16x16.</td></tr><tr><td colspan="4"> </td></tr><tr><td colspan="4">Programming Notes</td></tr></table>	Value	Name	Description	Programming Notes	0h	Normal Mode [Default]	GT3: 16x16 Hashing enabled GT2 or lower modes: No cross slice hashing		1h	Cross Slice Hashing Disable	Disables the cross slice hashing		2h	32x16 Hahsing	32x16 Pixel hashing across slices		3h	32X32 hashing	32X32 pixel hashing across slices	This setting must be used when sub-slice hashing mode is 16x16.					Programming Notes				Normal mode of operation in GT3 mode will be to use either 16x16 Hashing or 32x32 Hashing.		
	Value	Name	Description	Programming Notes																												
	0h	Normal Mode [Default]	GT3: 16x16 Hashing enabled GT2 or lower modes: No cross slice hashing																													
	1h	Cross Slice Hashing Disable	Disables the cross slice hashing																													
	2h	32x16 Hahsing	32x16 Pixel hashing across slices																													
	3h	32X32 hashing	32X32 pixel hashing across slices	This setting must be used when sub-slice hashing mode is 16x16.																												
Programming Notes																																
10	Reserved																															
	Access:	r/w																														
	Format:	PBC																														
9:8	Subslice Hashing Mode																															
	Access:	r/w																														
	Format:	U2																														
	This field defines hashing modes across subslices.																															
	Value	Name	Description																													
	0h	[Default]	8X8 hashing																													
	1h		16x4 hashing																													
	2h		8x4 hashing																													
	3h		16x16 hashing																													
7	Reserved																															
	Access:	r/w																														
	Format:	PBC																														
7	Bindless Surface Base Address Select																															
	Access:	r/w																														
	Format:	Enable																														
	This field selects Bindless_Surface_State_Base_Addr versus Dynamic_State_Base_Addr for sampler state heap base address. It only applies when Bindless Surfaces are being enabled via the BTI encoding. It is intended to allow support for bindless samplers in BXT by sharing the Bindless Surface heap, and using the Bindless Surface Base Addr.																															
	Value	Name	Description																													
	0h	Disable [Default]	Selects Dynanmic State Base Addr for Sampler State.																													

**GT_MODE - GT Mode Register**

	1h	Enable	Selects Bindless Surface Base Address for Sampler State
6	Reserved		
	Access:		r/w
	Format:		PBC
5:4	Slice2 IZ Hashing: 7 EU subslice encoding		
	Access:		r/w
	These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.		
	Value	Name	Description
	0h	[Default]	All subslices have equal number of EUs.
	1h		Subslice 2 has 7 EUs.
	2h		Subslice 1 has 7 EU.
	3h		Subslice 0 has 7 EUs.
	Programming Notes		
	SW must program these bits based on EU Disable Fuses in Slice 2.		
3:2	Slice1 IZ Hashing: 7 EU subslice encoding		
	Access:		r/w
	These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.		
	Value	Name	Description
	0h	[Default]	All subslices have equal number of EUs.
	1h		Subslice 2 has 7 EUs.
	2h		Subslice 1 has 7 EUs.
	3h		Subslice 0 has 7 EUs.
	Programming Notes		
	SW must program these bits based on EU Disable Fuses in Slice 1.		
1:0	Slice 0 IZ Hashing: 7 EU subslice encoding		
	Access:		r/w
	These bits control 3-way sub-slice hashing by conveying which sub-slice has 7 EUs.		
	Value	Name	Description
	0h	[Default]	All subslices have equal number of EUs.
	1h		Subslice 2 has 7 EUs.
	2h		Subslice 1 has 7 EUs.
	3h		Subslice 0 has 7 EUs.
	Programming Notes		
	SW must program these bits based on EU Disable Fuses in Slice 0.		



Hardware Scratch Read Write

HSRW_0_2_0_PCI - Hardware Scratch Read Write		
Register Space: PCI: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 16		
Address: 00060h		
This register is reserved as a HW scratchpad.		
DWord	Bit	Description
0	15:0	Reserved R/W
		Default Value: 0000000000000000b
		Access: R/W
		Reserved for future usage.



HDPORT_STATE

HDPORT_STATE			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	RO		
Size (in bits):	32		
Address:	45050h-45053h		
Name:	HDPORT State		
ShortName:	HDPORT_STATE		
Power:	PG0		
Reset:	soft		
This register is used to indicate when display resources have been pre-empted by hardware for the HDPORT feature. The usage is set during boot, before BIOS or software is active. The list of DPLLs and DDIs in this register many not accurately reflect the total number of DPLLs and DDIs supported by display engine. HDPORT will not use any DPLL or DDI not listed here. It will not use any DPLL or DDI that is listed here, but not supported by the particular product or SKU.			
Programming Notes			
HDPORT is not used on Broxton, so all bits will always be 0.			
Restriction			
Restriction : Display software must not use resources that are marked as being used by HDPORT.			
DWord	Bit	Description	
0	31:16	Reserved	
		Format: MBZ	
	15	DPLL2 Used	
		This field indicates whether DPLL 2 is being used by HDPORT.	
		Value	Name
		0b	Not used
	14	DPLL3 Used	
		This field indicates whether DPLL 3 is being used by HDPORT.	
		Value	Name
		0b	Not used
	13	DPLL1 Used	
		This field indicates whether DPLL 1 is being used by HDPORT.	



HDPOR_T_STATE			
		Value	Name
		0b	Not used
		1b	Used
	12	DPLL0 Used	
		This field indicates whether DPLL 0 is being used by HDPOR_T.	
		Value	Name
		0b	Not used
	11	Spare 11	
		Spare 10	
		Spare 9	
	8	DDI3 Type	
		This field indicates whether DDI 3 (DDI D) is being used in HDMI or DP mode by HDPOR_T.	
		Value	Name
		0b	DP
	7	DDI3 Used	
		This field indicates whether DDI 3 (DDI D) is being used by HDPOR_T.	
		Value	Name
		0b	Not used
	6	DDI2 Type	
		This field indicates whether DDI 2 (DDI C) is being used in HDMI or DP mode by HDPOR_T.	
		Value	Name
		0b	DP
	5	DDI2 Used	
		This field indicates whether DDI 2 (DDI C) is being used by HDPOR_T.	
		Value	Name
		0b	Not used
	4	DDI1 Type	
		This field indicates whether DDI 1 (DDI B) is being used by the HDPOR_T in HDMI or DP mode.	
		Value	Name



HDPORT_STATE			
		0b	DP
		1b	HDMI
	3	DDI1 Used This field indicates whether DDI 1 (DDI B) is being used by HDPORT.	
		Value	Name
		0b	Not used
		1b	Used
	2	DDI0 Type This field indicates whether DDI 0 (DDI A and DDI E) is being used in HDMI or DP mode by HDPORT.	
		Value	Name
		0b	DP
		1b	HDMI
	1	DDI0 Used This field indicates whether DDI 0 (DDI A and DDI E) is being used by HDPORT.	
		Value	Name
		0b	Not used
		1b	Used
	0	HDPORT Enabled This field indicates whether HDPORT is enabled.	
		Value	Name
		0b	Disabled
		1b	Enabled



Header Type

HDR2_0_2_0_PCI - Header Type			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	0000Eh		
This register contains the Header Type of the IGD.			
DWord	Bit	Description	
0	7	Multi Function Status	
		Default Value:	0b
		Access:	RO
	Indicates if the device is a Multi-Function Device. The Value of this register is hardwired to 0, internal graphics is a single function.		
	6:0	Header Code	
		Default Value:	0000000b
		Access:	RO
This is a 7-bit value that indicates the Header Code for the IGD. This code is hardwired to the value 00h, indicating a type 0 configuration space format.			



HOTPLUG_CTL

HOTPLUG_CTL			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	C4030h-C4033h		
Name:	Hot Plug Control		
ShortName:	HOTPLUG_CTL		
Power:	PG0		
Reset:	soft		
Hot plug detect (HPD) is used for notification of plug, unplug, and other sink events. The short pulse durations are programmed in HPD_PULSE_CNT. The hotplug ISR gives the live states of the HPD pins.			
Programming Notes			
Due to the possibility of back to back HPD events it is recommended that software filters the value read from the ISR.			
DWord	Bit	Description	
0	31:29	Reserved	
		Format: MBZ	
	28	DDI A HPD Input Enable	
		This field enables the HPD buffer for digital port A.	
		Value	Name
		0b	Disable
	1b	Enable	
		27	DDI A HPD Invert
			This field inverts the HPD sense for digital port A.
	Value		Name
	1b		Invert
	0b	Do not invert	
		26	Reserved
	Format: MBZ		
	25:24	DDI A HPD Status	
Access: R/WC			
This field indicates the hot plug detect status on port A.			



HOTPLUG_CTL												
		When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR). These are sticky bits, cleared by writing 1s to both of them. <table><tr><th>Value</th><th>Name</th></tr><tr><td>00b</td><td>Hot plug event not detected</td></tr><tr><td>01b</td><td>Short pulse detected</td></tr><tr><td>10b</td><td>Long pulse detected</td></tr><tr><td>11b</td><td>Short and long pulses detected</td></tr></table>	Value	Name	00b	Hot plug event not detected	01b	Short pulse detected	10b	Long pulse detected	11b	Short and long pulses detected
Value	Name											
00b	Hot plug event not detected											
01b	Short pulse detected											
10b	Long pulse detected											
11b	Short and long pulses detected											
23:13	Reserved											
	Format:	MBZ										
12	DDI C HPD Input Enable This field enables the HPD buffer for digital port C.											
	Value	Name										
	0b	Disable										
	1b	Enable										
11	DDI C HPD Invert This field inverts the HPD sense for digital port C.											
	Value	Name										
	1b	Invert										
	0b	Do not invert										
10	Reserved											
	Format:	MBZ										
9:8	DDI C HPD Status											
	Access:	R/WC										
	This field indicates the hot plug detect status on port C. When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR). These are sticky bits, cleared by writing 1s to both of them.											
	Value	Name										
	00b	Hot plug event not detected										
	01b	Short pulse detected										
	10b	Long pulse detected										
	11b	Short and long pulses detected										
7:5	Reserved											
	Format:	MBZ										



HOTPLUG_CTL											
	4	DDI B HPD Input Enable This field enables the HPD buffer for digital port B.									
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Disable</td></tr><tr><td>1b</td><td>Enable</td></tr></table>	Value	Name	0b	Disable	1b	Enable			
		Value	Name								
		0b	Disable								
	1b	Enable									
	3	DDI B HPD Invert This field inverts the HPD sense for digital port B.									
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>1b</td><td>Invert</td></tr><tr><td>0b</td><td>Do not invert</td></tr></table>	Value	Name	1b	Invert	0b	Do not invert			
		Value	Name								
		1b	Invert								
	0b	Do not invert									
	2	Reserved									
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ							
	Format:	MBZ									
1:0	DDI B HPD Status										
	<table><tr><td>Access:</td><td>R/WC</td></tr></table>	Access:	R/WC								
	Access:	R/WC									
	This field indicates the hot plug detect status on port B. When HPD input is enabled and either a long or short pulse is detected, one of these bits will set and the hotplug IIR will be set (if unmasked in the IMR). These are sticky bits, cleared by writing 1s to both of them.										
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>00b</td><td>Hot plug event not detected</td></tr><tr><td>01b</td><td>Short pulse detected</td></tr><tr><td>10b</td><td>Long pulse detected</td></tr><tr><td>11b</td><td>Short and long pulses detected</td></tr></table>	Value	Name	00b	Hot plug event not detected	01b	Short pulse detected	10b	Long pulse detected	11b	Short and long pulses detected
	Value	Name									
	00b	Hot plug event not detected									
01b	Short pulse detected										
10b	Long pulse detected										
11b	Short and long pulses detected										



HPD_FILTER_CNT

HPD_FILTER_CNT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x000001F2	
Access:	R/W	
Size (in bits):	32	
Address:	C4038h-C403Bh	
Name:	HPD Filter Count	
ShortName:	HPD_FILTER_CNT	
Power:	PG0	
Reset:	global	
This register is on the chip reset, not the FLR.		
Restriction		
Restriction : This register must be programmed properly before enabling DDI HPD detection.		
DWord	Bit	Description
0	31:17	Reserved
		Format: MBZ
	16:0	HPD Filter Count
		Default Value: 001F2h 500 microseconds These bits define the duration of the filter for DDI HPD. The value is the number of microseconds minus 2.



HPD_PULSE_CNT

HPD_PULSE_CNT			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x000007CE		
Access:	R/W		
Size (in bits):	32		
Address:	C4034h-C4037h		
Name:	HPD Pulse Count DDI B		
ShortName:	HPD_PULSE_CNT_B		
Power:	PG0		
Reset:	global		
Address:	C4044h-C4047h		
Name:	HPD Pulse Count DDI C		
ShortName:	HPD_PULSE_CNT_C		
Power:	PG0		
Reset:	global		
Address:	C404Ch-C404Fh		
Name:	HPD Pulse Count DDI A		
ShortName:	HPD_PULSE_CNT_A		
Power:	PG0		
Reset:	global		
There is one instance of this register per DDI. This register is on the chip reset, not the FLR.			
Restriction			
Restriction : This register must be programmed properly before enabling DDI HPD detection.			
DWord	Bit	Description	
0	31:17	Reserved	
		Format: MBZ	
	16:0	ShortPulse Count	
		These bits define the duration of the pulse defined as a short pulse for DDI HPD. The value is the number of microseconds minus 2.	
		Value	Name
		007CEh	2,000 microseconds for DisplayPort [Default]
1869Eh	100,000 microseconds for HDMI and DVI		



Indirect Context Pointer

INDIRECT_CTX - Indirect Context Pointer	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Trusted Type:	1
This register is used to program the indirect address to be executed between CS and SVG engine context if enabled. This will only get executed due to regular context save/restore and not during power restore. This register is part of the execution list context and will be executed per context. Only supported if execution list is enabled. There is no preempting workloads within this context.	
Programming Notes	Source
BlitterCS/VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be programmed for these command streamers.	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS
The following commands are not supported within Render CS indirect context:	RenderCS
Command Name	
MI_WAIT_FOR_EVENT	
MI_SEMAPHORE_SIGNAL	
MI_ARB_CHECK	
MI_RS_CONTROL	
MI_REPORT_HEAD	
MI_URB_ATOMIC_ALLOC	
MI_SUSPEND_FLUSH	
MI_TOPOLOGY_FILTER	
MI_RS_CONTEXT	
MI_SET_CONTEXT	
MI_URB_CLEAR	
MI_SEMAPHORE_WAIT in Memory Poll Mode is not supported. [BXT]: MI_SEMAPHORE_WAIT in register poll mode is supported.	
MI_BATCH_BUFFER_START	
MI_CONDITIONAL_BATCH_BUFFER_END	
MEDIA_OBJECT_WALKER	
GPGPU_WALKER	
3DPRIMITIVE	
3DSTATE_BINDING_TABLE_POINTERS_VS	

**INDIRECT_CTX - Indirect Context Pointer**

3DSTATE_BINDING_TABLE_POINTERS_HS	
3DSTATE_BINDING_TABLE_POINTERS_DS	
3DSTATE_BINDING_TABLE_POINTERS_GS	
3DSTATE_BINDING_TABLE_POINTERS_PS	
3DSTATE_GATHER_CONSTANT_VS	
3DSTATE_GATHER_CONSTANT_GS	
3DSTATE_GATHER_CONSTANT_HS	
3DSTATE_GATHER_CONSTANT_DS	
3DSTATE_GATHER_CONSTANT_PS	
3DSTATE_DX9_CONSTANTF_VS	
3DSTATE_DX9_CONSTANTF_HS	
3DSTATE_DX9_CONSTANTF_DS	
3DSTATE_DX9_CONSTANTF_GS	
3DSTATE_DX9_CONSTANTF_PS	
3DSTATE_DX9_CONSTANTI_VS	
3DSTATE_DX9_CONSTANTI_HS	
3DSTATE_DX9_CONSTANTI_DS	
3DSTATE_DX9_CONSTANTI_GS	
3DSTATE_DX9_CONSTANTI_PS	
3DSTATE_DX9_CONSTANTB_VS	
3DSTATE_DX9_CONSTANTB_HS	
3DSTATE_DX9_CONSTANTB_DS	
3DSTATE_DX9_CONSTANTB_GS	
3DSTATE_DX9_CONSTANTB_PS	
3DSTATE_DX9_LOCAL_VALID_VS	
3DSTATE_DX9_LOCAL_VALID_DS	
3DSTATE_DX9_LOCAL_VALID_HS	
3DSTATE_DX9_LOCAL_VALID_GS	
3DSTATE_DX9_LOCAL_VALID_PS	
3DSTATE_DX9_GENERATE_ACTIVE_VS	
3DSTATE_DX9_GENERATE_ACTIVE_HS	
3DSTATE_DX9_GENERATE_ACTIVE_DS	
3DSTATE_DX9_GENERATE_ACTIVE_GS	
3DSTATE_DX9_GENERATE_ACTIVE_PS	
3DSTATE_BINDING_TABLE_EDIT_VS	



INDIRECT_CTX - Indirect Context Pointer

3DSTATE_BINDING_TABLE_EDIT_GS
3DSTATE_BINDING_TABLE_EDIT_HS
3DSTATE_BINDING_TABLE_EDIT_DS
3DSTATE_BINDING_TABLE_EDIT_PS
3DSTATE_CONSTANT_VS
3DSTATE_CONSTANT_GS
3DSTATE_CONSTANT_PS
3DSTATE_CONSTANT_HS
3DSTATE_CONSTANT_DS
MI_BATCH_BUFFER_END

Workaround

[Render CS Only][Execlist Mode of Scheduling]: SW must ensure arbitration is switched off while context restore is in progress for any given context. This is achieved by disabling arbitration by programming MI_ARB_ON_OFF to "Arbitration Disable" in RCS_INDIRECT_CTX buffer and by enabling back the arbitration by programming MI_ARB_ON_OFF to "Arbitration Enable" as the last command prior to MI_BATCH_END in the BB_PER_CTX_PTR buffer of every context submitted. Note that RCS_INDIRECT_CTX_OFFSET could be set to default value or any other legitimate value as per the programming notes of the register definition. Arbitration disable by programming MI_ARB_ON_OFF (Arbitration Disabled) in RCS_INDIRECT_CTX buffer. Arbitration enabled by programming MI_ARB_ON_OFF (Arbitration Enabled) as the last command prior to MI_BATCH_BUFFER_END in BB_PER_CTX_PTR buffer. Additional Note: This WA need not be applied when it is guaranteed for no preemption to occur during execution of GPGPU workload. Preemption of GPGPU workload can be avoided by Bracketing the GPGPU workload with MI_ARB_ON_OFF (Arbitration Disable) and MI_ARB_ON_OFF (Arbitration Enable) command. MI_ARB_ON_OFF is a privileged command and can only be programmed in ring buffer or in privileged batch buffer (batch buffer in GGTT memory). Pending execlist submitted must not trigger preemption of the ongoing GPGPU workload due to following reasons First context of the pending execlist submitted is not the same as the ongoing GPGPU context. Force restore bit set for the submitted pending execlist.

DWord	Bit	Description		
0	31:6	Indirect CS Context Address		
		<table><tr><td>Format:</td><td>GraphicsAddress[31:6]</td></tr></table> Pointer to the Context in memory to be executed as a batch.	Format:	GraphicsAddress[31:6]
	Format:	GraphicsAddress[31:6]		
	5:0	Size of Indirect CS Context		
<table><tr><td>Format:</td><td>U6</td></tr></table> This is the size of the Indirect Context for CS. This size supports up to 63 cache lines worth of commands where a cache line is 64B. If programmed to zero then the indirect fetch of the CS context is disabled.		Format:	U6	
Format:		U6		
<table><tr><th>Value</th><th>Name</th></tr><tr><td>[0,63]</td><td></td></tr></table>	Value	Name	[0,63]	
Value	Name			
[0,63]				



Interrupt Line

INTRLINE_0_2_0_PCI - Interrupt Line			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	0003Ch		
This register is used to communicate interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.			
DWord	Bit	Description	
0	7:0	Interrupt Connection	
		Default Value:	00000000b
		Access:	R/W
		Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates to which input of the system interrupt controller the device's interrupt pin is connected.	



Interrupt Pin

INTRPIN_0_2_0_PCI - Interrupt Pin			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000001		
Size (in bits):	8		
Address:	0003Dh		
This register tells which interrupt pin the device uses.			
DWord	Bit	Description	
0	7:0	Interrupt Pin Value	
		Default Value:	00000001b
		Access:	RO
		As a single function device, the IGD specifies INTA# as its interrupt pin. Hardwired to 01h = INTA#.	



I/O Base Address

IOBAR_0_2_0_PCI - I/O Base Address			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000001		
Size (in bits):	32		
Address:	00020h		
This register provides the Base offset of the I/O registers within Device #2. Bits 15:6 are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space. Bits 2:1 are fixed and return zero; bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded. Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if Internal graphics is disabled through the fuse or fuse override mechanisms. Note that access to this IO BAR is independent of VGA functionality within Device #2. If accesses to this IO bar is allowed then all 8, 16 or 32 bit IO cycles from IA cores that falls within the 8B are claimed.			
DWord	Bit	Description	
0	31:16	Reserved	
		Default Value:	0000000b
		Access:	RO
		Reserved	
	15:6	IO Base Address	
		Default Value:	000000000b
		Access:	R/W
		Set by the OS, these bits correspond to address signals [15:6].	
	5:3	Reserved	
		Default Value:	0000000b
		Access:	RO
		Reserved	
	2:1	Memory Type	
		Default Value:	00b
		Access:	RO
		Hardwired to 0s to indicate 32-bit address.	



IOBAR_0_2_0_PCI - I/O Base Address			
	0	Memory/IO Space	
		Default Value:	1b
		Access:	RO
		Hardwired to "1" to indicate IO space.	



IOMMU_DEFEATURE_CAPECAPDIS

IOMMU_DEFEATURE_CAPECAPDIS - IOMMU_DEFEATURE_CAPECAPDIS			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	03000h		
Description			
Capability/Extended Capability Disable Register. Register providing control of various IOMMU functionality. This register is a LOCAL CR register and not an MMIO register			
DWord	Bit	Description	
0	31:25	RSVD	
		Default Value:	0b
		Access:	RO
		RSVD	
	24	EAFCAPDIS	
		Default Value:	0b
		Access:	R/W
		1: Hardware does not support the extended-accessed (EA) bit in first-level paging-structure entries. 0: Hardware supports the extendedaccessed (EA) bit in first-level paging-structure entries.	
	23	NWFSCAPDIS	
		Default Value:	0b
		Access:	R/W
		1: Hardware ignores the "No Write" (NW) flag in Device-TLB translationrequests, and behaves as if NW is always 0. 0: Hardware supports the "No Write" (NW) flag in Device-TLB translationrequests.	
	22	POT	
		Default Value:	0b
		Access:	R/W
		1: Hardware does not support PASID-only Translation Type in extended-context-entries. 0: Hardware supports PASID-only Translation Type in extended-context-entries.	



IOMMU_DEFEATURE_CAPECAPDIS - IOMMU_DEFEATURE_CAPECAPDIS

	21	SRS	
		Default Value:	0b
		Access:	R/W
		1: H/W does not support requests-with-PASID seeking supervisor privilege. 0: H/W supports requests-with-PASID seeking supervisor privilege.	
	20	ERS	
		Default Value:	0b
		Access:	R/W
		1: H/W does not support requests seeking execute permission. 0: H/W supports requests seeking execute permission.	
	19	PRSCAPDIS	
		Default Value:	0b
		Access:	R/W
		1: Hardware does not support Page Requests. 0: Hardware supports Page Requests.	
	18	PASIDCAPDIS	
		Access:	R/W
		1: Hardware does not support process address space IDs. 0: Hardware supports Process Address Space IDs.	
		Value	Name
		0b	
	17	DISCAPDIS	
		Default Value:	0b
		Access:	R/W
		1: Hardware does not support deferred invalidations of IOTLB and Device-TLB. 0: Hardware supports deferred invalidations of IOTLB and Device-TLB.	
	16	NESTCAPDIS	
		Default Value:	0b
		Access:	R/W
		1: Hardware does not support nested translations. 0: Hardware supports nested translations.	



IOMMU_DEFEATURE_CAPECAPDIS - IOMMU_DEFEATURE_CAPECAPDIS

IOMMU_DEFEATURE_CAPECAPDIS - IOMMU_DEFEATURE_CAPECAPDIS		
15	MTSCAPDIS	
	Default Value:	0b
	Access:	R/W
	1: Hardware does not support Memory Type in first-level translation and Extended in second-level.	
	0: Hardware supports Memory Type in first-level translation and Extended mem type in second-level.	
14	ECSCAPDIS	
	Default Value:	0b
	Access:	R/W
	1: Hardware does not support extended-root-entries and Extended Context-Entries	
	0: Hardware supports extended-root-entries and Extended Context-Entries	
13	SCCAPDIS	
	Default Value:	0b
	Access:	R/W
	1: Hardware does not support 1-setting of the SNP field in the page-table entries.	
	0: Hardware supports the 1-setting of the SNP field in the page-table entries.	
12	PTCAPDIS	
	Default Value:	0b
	Access:	R/W
	1: Hardware does not support pass-through translation type in context entries.	
	0: Hardware supports pass-through translation type in context entries.	
11	EIM	
	Default Value:	0b
	Access:	R/W
	1: On Intelx64 platforms, hardware supports only 8-bit APIC-IDs (xAPIC mode).	
	0: On Intelx64 platforms, hardware supports 32-bit APIC-IDs (x2APIC mode).	
10	IRCAPDIS	
	Default Value:	0b
	Access:	R/W
	1: Hardware does not support interrupt remapping.	
	0: Hardware supports interrupt remapping.	



IOMMU_DEFEATURE_CAPECAPDIS - IOMMU_DEFEATURE_CAPECAPDIS

IOMMU_DEFEATURE_CAPECAPDIS - IOMMU_DEFEATURE_CAPECAPDIS		
9	DTCAPDIS	
	Default Value:	0b
	Access:	R/W
	1: Hardware does not support device-IOTLBs. 0: Hardware supports Device-IOTLBs.	
8	QICAPDIS	
	Default Value:	0b
	Access:	R/W
	1: Hardware does not support queued invalidations. 0: Hardware supports queued invalidations.	
7	C	
	Default Value:	0b
	Access:	R/W
	This field indicates if hardware access to the root, context, page-table and interrupt-remap structures are coherent (snooped) or not. 1: Indicates hardware accesses to remapping structures are non-coherent. 0: Indicates hardware accesses to remapping structures are coherent.	
6	FL1GPCAPDIS	
	Default Value:	0b
	Access:	R/W
	A value of 1 in this field indicates 1-GBYTE page size is disabled for first-level translation.	
5	PSI	
	Default Value:	0b
	Access:	R/W
	Page Selective Invalidation. 1: Hardware supports only domain and global invalidates for IOTLB 0: Hardware supports page selective, domain and global invalidates for IOTLB	
4:1	SLLPSCAPCTRL	
	Default Value:	0h
	Access:	R/W
	This field indicates the super page sizes supported by hardware. A value of 1 in any of these bits indicates the corresponding super-page size is supported. The super-page sizes corresponding to various bit positions within this field are: 0: 21-bit offset to page frame (2MB)	



IOMMU_DEFEATURE_CAPECAPDIS - IOMMU_DEFEATURE_CAPECAPDIS

		1: 30-bit offset to page frame (1GB) 2: 39-bit offset to page frame (512GB) 3: 48-bit offset to page frame (1TB) Hardware implementations supporting a specific super-page size must support all smaller super-page sizes, i.e. only valid values for this field are 0000b, 0001b, 0011b, 0111b, 1111b.SLLPSCAPCTRL	
	0	ZLR	
		Default Value:	0b
		Access:	R/W
1: Indicates the remapping hardware unit blocks (and treats as fault) zero length DMA read requests to write-only pages. 0: Indicates the remapping hardware unit supports zero length DMA read requests to write-only pages.			



IOMMU_DEFEATURE_MISCDIS

IOMMU_DEFEATURE_MISCDIS - IOMMU_DEFEATURE_MISCDIS			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0300Ch		
Description			
Miscellaneous Disable Register. Register to disable certain functionality of IOMMU. This register is a LOCAL CR register and not an MMIO register			
DWord	Bit	Description	
0	31	Reserved	
	30:23	Reserved	
	22:10	SPARE	
		Default Value:	000h
		Access:	R/W
		Reserved bit	
	9	PRQCOHDIS	
		Default Value:	0b
		Access:	R/W
		PRQ Coherency Disability	
	8	QICOHDIS	
		Default Value:	0b
		Access:	R/W
		QI Coherency Disability	
	7	H2PDIS	
		Default Value:	0b
		Access:	R/W
		Hit2pend Disability	
	6	DMA_RSRV_CTL	
		Default Value:	0b
		Access:	R/W
		Reserved bit check Disability	

**IOMMU_DEFEATURE_MISCDIS - IOMMU_DEFEATURE_MISCDIS**

	5:4	COLORLIMDIS	
		Default Value:	00b
		Access:	R/W
		Disable color limit	
	3	STALLFETCHFIFODIS	
		Default Value:	0b
		Access:	R/W
		Stall Fetch FIFO	
	2	STALLCBFIFODIS	
		Default Value:	0b
		Access:	R/W
		Stall CB FIFO	
	1	CTXPARTINVDIS	
		Default Value:	0b
		Access:	R/W
		Convert Context function/domain invalidations to global	
	0	IOTLBPARTINVDIS	
		Default Value:	0b
		Access:	R/W
		Convert IOTLB page/domain invalidations to global	



IOMMU_DEFEATURE_PWRDNOVRD

IOMMU_DEFEATURE_PWRDNOVRD - IOMMU_DEFEATURE_PWRDNOVRD			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	03010h		
Description			
Power Down Override Register. Power Down Override for individual IOMMU component. This register is a LOCAL CR register and not an MMIO register			
DWord	Bit	Description	
0	31:20	RSVD	
		Default Value:	000h
		Access:	RO
		RSVD	
	19	PDO_Spare	
		Default Value:	0b
		Access:	R/W
		Spare Powerdown override.	
	18	PDO_FAULTCAP	
		Default Value:	0b
		Access:	R/W
		Powerdown override for Fault Handling Module.	
	17	PDO_QINV	
		Default Value:	0b
		Access:	R/W
		Powerdown override for QI Module.	
	16	PDO_MSG	
		Default Value:	0b
		Access:	R/W
		Powerdown override for Message Interface.	



IOMMU_DEFEATURE_PWRDNOVRD - IOMMU_DEFEATURE_PWRDNOVRD						
	15	PDO_INV <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Powerdown override for Invalidation Engine.	Default Value:	0b	Access:	R/W
	Default Value:	0b				
	Access:	R/W				
	14	PDO_SEQ <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Powerdown override for Sequencer.	Default Value:	0b	Access:	R/W
	Default Value:	0b				
	Access:	R/W				
	13	PDO_CREG <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Powerdown override for CREG Module.	Default Value:	0b	Access:	R/W
	Default Value:	0b				
	Access:	R/W				
	12	PDO_FETCH_RET <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Powerdown override for fetch return.	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
11	PDO_FETCH_FIFO <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Powerdown override for fetch fifo.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
10	PDO_L4_TLB <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Powerdown override for L4 TLB.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
9	PDO_RC_TLB <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Powerdown override for RC TLB.	Default Value:	0b	Access:	R/W	
Default Value:	0b					
Access:	R/W					
8	PDO_PQ_FSM <table><tr><td>Default Value:</td><td>0b</td></tr></table>	Default Value:	0b			
Default Value:	0b					



IOMMU_DEFEATURE_PWRDNOVRD - IOMMU_DEFEATURE_PWRDNOVRD			
		Access:	R/W
		Powerdown override for PQ FSM.	
	7	PDO_FILL_FSM	
		Default Value:	0b
		Access:	R/W
		Powerdown override for Fill FSM.	
	6	PDO_L4_FSM	
		Default Value:	0b
		Access:	R/W
		Powerdown override for L4 FSM.	
	5	PDO_RC_FSM	
		Default Value:	0b
		Access:	R/W
		Powerdown override for RC FSM.	
	4	PDO_IR_FSM	
		Default Value:	0b
		Access:	R/W
		Powerdown override for IR FSM.	
	3	PDO_PWT_ARB	
		Default Value:	0b
		Access:	R/W
		Powerdown override for PWT Arbiter.	
	2	PDO_PWT_PQ_ALLOC	
		Default Value:	0b
		Access:	R/W
		Powerdown override for Pending Queue Allocation.	
	1	PDO_TLB	
		Default Value:	0b
		Access:	R/W
		Powerdown override for TLB.	



IOMMU_DEFEATURE_PWRDNOVRD - IOMMU_DEFEATURE_PWRDNOVRD		
	0	PDO_CB
		Default Value: 0b
		Access: R/W
		Powerdown override for Credit Buffer.



IOMMU_DEFEATURE_PWSWTRDIS

IOMMU_DEFEATURE_PWSWTRDIS - IOMMU_DEFEATURE_PWSWTRDIS			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000000			
Size (in bits): 32			
Address: 03008h			
Description			
Page Walk Structure Disable Register.Disable Page Walk ways. This register is a LOCAL CR register and not an MMIO register			
DWord	Bit	Description	
0	31:14	RSVD	
		Default Value:	00000h
		Access:	RO
		RSVD	
	13:12	PQDIS	
		Default Value:	0h
		Access:	R/W
		Disable # of PQ entries. 11 : All but one entry/priority, 10 : 1/2, 01 : 1/4, 00 : none	
	11:10	PWTDIS	
		Default Value:	0h
		Access:	R/W
		Disable # of PWT entries. 11 : All but one entry/priority, 10 : 1/2, 01 : 1/4, 00 : none	
	9:8	RCCDIS	
		Default Value:	0h
		Access:	R/W
		Per TLBID, disable RCC. 11 : full, 10 : 1/2, 01 : 1/4, 00 : none.	
	7:6	SL5DIS	
		Default Value:	0h
		Access:	R/W
		Per TLBID, disable TLB. 11 : full, 10 : 1/2, 01 : 1/4, 00 : none.	



IOMMU_DEFEATURE_PWSWTRDIS - IOMMU_DEFEATURE_PWSWTRDIS

	5:4	SL4DIS	
		Default Value:	0h
		Access:	R/W
		Per TLBID, disable TLB. 11 : full, 10 : 1/2, 01 : 1/4, 00 : none.	
	3:2	SL3DIS	
		Default Value:	0h
		Access:	R/W
		Per TLBID, disable TLB. 11 : full, 10 : 1/2, 01 : 1/4, 00 : none.	
	1:0	SL2DIS	
		Default Value:	0h
		Access:	R/W
		Per TLBID, disable TLB 11 : full, 10 : 1/2, 01 : 1/4, 00 : none.	



IOMMU_DEFEATURE_TLBDIS

IOMMU_DEFEATURE_TLBDIS - IOMMU_DEFEATURE_TLBDIS		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 03004h		
Description		
IOTLB Disable Register. Per TLBID, disable TLB ways. This register is a LOCAL CR register and not an MMIO register		
DWord	Bit	Description
0	31:0	IOTLBDIS
		Default Value: 00000000h
		Access: R/W
		Per TLBID, disable TLB 11:full, 10:1/2, 01: 1/4, 00:none.



L3 Control Register

L3CNTLREG - L3 Control Register				
Register Space:	MMIO: 0/2/0			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	07034h			
Programming Notes				
The L3 allocation programming should assign all ways of the cache with no left over ways. Refer to L3 section for the recommended settings.				
Any L3 configuration change that reduces the data cache allocation when strong IA coherency is used requires the full flush of L3 prior to the programming update.				
An explicit or implicit flush of L3 (DC Flush) through the command streamer doesn't result in flushing/invalidating the IA Coherent lines from L3. However this can be achieved by setting the "Pipe line flush Coherent lines" control bit in the "L3SQCREG4" register.				
DWord	Bit	Description		
0	31:25	All L3 Client Pool		
		Access:	R/W	
		Number of ways allocated for the all client pool. This is a combined pool for all clients.		
		Value	Name	Description
		[0h,40h]		Increments of 4KB
		30h	[Default]	
		Programming Notes		
		When this field is non-zero, DC Way Assignment and Read Only Client Pool should be 0KB.		
		24:18	DC Way Assignment	
				Access:
Number of ways allocated for DC. Note this allocation is only for DC data types.				
Value	Name			Description
[0h,40h]	0KB-256KB			Increments of 4KB
Programming Notes				
Note: This field must be 0KB if All L3 Client Pool is non-zero. Please refer to L3 HAS for valid programming values				



L3CNTLREG - L3 Control Register

	17:11	Read Only Client Pool	
		Access:	R/W
		Number of ways allocated for Read Only L3 clients. This is a combined pool for all Read Only clients.	
		Value	Name
		[0h,40h]	0KB-256KB
		Increments of 4KB	
		Programming Notes	
		Note: This field must be 0KB if All L3 Client Pool is non-zero. Please refer to L3 HAS for valid programming values	
	10	Reserved	
		Access:	R/W
		Format:	PBC
	9	Error Detection Behavior Control	
		Access:	R/W
		Format:	Enable
		The L3 error detection can be enabled to hang the GPU on a non-recoverable error due to SER type events. Such option will be used when corresponding context has data consistency requirements.	
		Once error detection is enabled, s/w has to initialize URB or SLM to all 0's (based on usage model) prior to execution of the workload. Initialization is required to clean up the error detection logic and syndrome tracking.	
		Value	Name
		0h	[Default]
		1h	
		Description	
		RTL does not hang on parity errors or double bit error	
	8	GPGPU L3 Credit Mode Enable	
		Access:	R/W
		Format:	Enable
		This bit is required to be enabled under GPGPU workloads to provide the MAX latency coverage from L3 cache. It will override the registers 0xB100[18:14] and 0xB100[23:19], to 0 and the maximum value respectively.	
	7:1	URB Allocation	
		Access:	R/W
		Number of ways allocated for URB usage	
		Value	Name
		[0h,40h]	
		30h	[Default]
		Description	
		Increments of 4KB	



L3CNTLREG - L3 Control Register		
		Programming Notes
		Please refer to L3 HAS for valid programming values. At least one way needs to be programmed in L3 space.
	0	SLM Mode Enable
		Access: R/W
		Format: Enable
		When enabled, a 64KB (per bank) region of L3 is reserved for SLM.



L3 Control Register1

L3CNTLREG1 - L3 Control Register1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0xD007FFFF	
Size (in bits):	32	
Address:	0B10Ch	
DWord	Bit	Description
0	31:28	Data Fifo Depth Control
		Access: R/W
		Data Fifo Depth Control (TS mode).
		Value cannot be zero for normal operation.
		lbcf_csr_lc_datafifo_depth[3:0].
	27:24	Data Clock off time
		Access: R/W
		Description
		Data Clock off time (DATACLKOFF): Data Clock off time - Data block is shut off after these many number of clocks programmed in this register bits. lbcf_csr_lc_dataclkoff_time[3:0]. Min value to be 4'h0100. It should be between 4'h4 : 4'hf.
		Value Name
		1100b [Default]
	23:20	TAG CLK OFF TIME
		Access: R/W
		Description
		TAG CLK OFF TIME (TAGCLKOFF): TAG Clock Off time. This is the time, which Clock gating Logic checks before it turns off the clock. lbcf_csr_lc_tagclkoff_time[3:0]. Value can be between 4'h4 - 4'hf.
		Value Name
		1100b [Default]

**L3CNTLREG1 - L3 Control Register1**

		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0100b</td><td>[Default]</td></tr></table>	Value	Name	0100b	[Default]
Value	Name					
0100b	[Default]					
19	L3 Aging Disable Bit	<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> L3 Aging Disable Bit (L3AGDIS): Aging Disable. lbcf_csr_lc_agingdis.	Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
18:15	Fill aging	<table><tr><td>Default Value:</td><td>1111b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Fill aging (L3AGF): Aging Counter for Fill. lbcf_csr_lc_fill_aging_cnt[3:0]. If bit B103.19 is 0 then this register value has to be nonzero.	Default Value:	1111b	Access:	R/W
Default Value:	1111b					
Access:	R/W					
14:11	Aging Counter for Read 1 Port	<table><tr><td>Default Value:</td><td>1111b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Aging Counter for Read 1 Port (L3AGR1): Aging Counter for Read 1 Port. lbcf_csr_lc_r1_aging_cnt[3:0]. If bit B103.19 is 0 then this register value has to be nonzero.	Default Value:	1111b	Access:	R/W
Default Value:	1111b					
Access:	R/W					
10:7	L3 Aging Counter for R0	<table><tr><td>Default Value:</td><td>1111b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> L3 Aging Counter for R0 (L3AGR0): Aging Counter for R0 Port. lbcf_csr_lc_r0_aging_cnt[3:0]. If bit B103.19 is 0 then this register value has to be nonzero.	Default Value:	1111b	Access:	R/W
Default Value:	1111b					
Access:	R/W					
6:4	L3 Aging Counter for SNOOP	<table><tr><td>Default Value:</td><td>111b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> L3 Aging Counter for SNOOP: Aging Counter for Snoop Port. lbcf_csr_lc_snp_aging_cnt[3:0].	Default Value:	111b	Access:	R/W
Default Value:	111b					
Access:	R/W					



L3CNTLREG1 - L3 Control Register1			
	3:0	Fill aging for port1	
		Default Value:	1111b
		Access:	R/W
		Fill aging (L3AGF): Aging Counter for Fill port 1. lbcf_csr_lc_fill1_aging_cnt[3:0]. If bit B103.19 is 0 then this register value has to be nonzero.	



L3 LRA 0 GPGPU

L3_LRA_0_GPGPU - L3 LRA 0 GPGPU		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x0400FC00	
Size (in bits):	32	
Address:	04DD0h	
DWord	Bit	Description
0	31:30	L3 GPGPU
		Default Value: 00b
		Access: R/W
		Which LRA should L3 use.
	29:20	L3 LRA1 Min GPGPU
		Default Value: 0001000000b
		Access: R/W
		Minimum value of programmable LRA1.
	19:10	L3 LRA0 Max GPGPU
		Default Value: 0000111111b
		Access: R/W
		Maximum value of programmable LRA0.
	9:0	L3 LRA0 Min GPGPU
		Default Value: 0000000000b
		Access: R/W
		Minimum value of programmable LRA0.



L3 LRA 1 GPGPU

L3_LRA_1_GPGPU - L3 LRA 1 GPGPU		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x5FF6C1AF	
Size (in bits):	32	
Address:	04DD4h	
DWord	Bit	Description
0	31:30	DC GPGPU
		Default Value: 01b
		Access: R/W
		Which LRA should DC use.
	29:20	L3 LRA2 Max GPGPU
		Default Value: 011111111b
		Access: R/W
		Maximum value of programmable LRA2.
	19:10	L3 LRA2 Min GPGPU
		Default Value: 0110110000b
		Access: R/W
		Minimum value of programmable LRA2.
	9:0	L3 LRA1 Max GPGPU
		Default Value: 011010111b
		Access: R/W
		Maximum value of programmable LRA1.



L3 LRA 0 3D

L3_LRA_0_3D - L3 LRA 0 3D		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x0400FC00	
Size (in bits):	32	
Address:	04A10h	
DWord	Bit	Description
0	31:30	L3 3D
		Default Value: 00b
		Access: R/W
		Which LRA should L3 use.
	29:20	L3 LRA1 Min 3D
		Default Value: 0001000000b
		Access: R/W
		Minimum value of programmable LRA1.
	19:10	L3 LRA0 Max 3D
		Default Value: 0000111111b
		Access: R/W
		Maximum value of programmable LRA0.
	9:0	L3 LRA0 Min 3D
		Default Value: 0000000000b
		Access: R/W
		Minimum value of programmable LRA0.



L3 LRA 1 3D

L3_LRA_1_3D - L3 LRA 1 3D						
Register Space:		MMIO: 0/2/0				
Source:		BSpec				
Default Value:		0x5EF2408F				
Size (in bits):		32				
Address:		04A14h				
DWord	Bit	Description				
0	31:30	DC 3D				
		Default Value: 01b				
		Access: R/W				
		Which LRA should DC use.				
	29:20	L3 LRA2 Max 3D				
		Access: R/W				
		Maximum value of programmable LRA2.				
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0111101111b</td><td>[Default]</td></tr></table>		Value	Name	0111101111b
	Value	Name				
	0111101111b	[Default]				
	19:10	L3 LRA2 Min 3D				
		Default Value: 0010010000b				
		Access: R/W				
		Minimum value of programmable LRA2.				
	9:0	L3 LRA1 Max 3D				
		Default Value: 0010001111b				
Access: R/W						
Maximum value of programmable LRA1.						



L3 LRA 2 3D

L3_LRA_2_3D - L3 LRA 2 3D		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x007FDF0E	
Size (in bits):	32	
Address:	04A18h	
DWord	Bit	Description
0	31:24	Reserved
		Default Value: 00000000b
		Access: RO
	23:14	L3 LRA3 Max 3D
		Default Value: 011111111b
		Access: R/W
		Maximum value of programmable LRA2. If L3LRA3Min_3D == L3LRA3Max_3D , GATR LRA is disabled, GATR cycles are mapped to L3LRA0 If L3LRA3Min_3D == L3LRA3Max_3D , GATR LRA is disabled, L3LRA2Max_3D will default to L3LRA3Max_3D to reuse GATR entries
	13:4	L3 LRA3 Min 3D
		Default Value: 0111110000b
		Access: R/W
		Minimum value of programmable LRA3.
	3:2	GATR_3D
		Default Value: 11b
		Access: R/W
		Which LRA should GATR use.
	1:0	Texture 3D
		Default Value: 10b
		Access: R/W
		Which LRA should Texture use.



L3 SQC register 4

L3SQCREG4 - L3 SQC register 4		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x40400000	
Size (in bits):	32	
Address:	0B118h	
DWord	Bit	Description
0	31	Reserved
	30	L3SQ URB Read CAM Match Disable
		Default Value: 1b
		Access: R/W
L3SQ URB Read CAM Match Disable (SQURBRDCAMDIS): Disables the L3SQ Cam Match ability for URB Reads. By disabling, this allows a performance mode where URB reads are not dependent upon one another but only on any previous URB writes to the same address. This allows many URB reads to the same cacheline at any given time instead of serializing the requests. 1 = URB Read CAM matching is disabled; multiple URB reads to the same cacheline are allowed to be concurrent (default). 0 = URB Read CAM matching is enabled; multiple URB reads to the same cacheline are serialized. lbcf_csr_lsqc_urbrdcam_dis.		
	29:28	Traffic regulation in LSQC for URB lookup traffic
		Default Value: 00b
		Access: R/W
		Traffic regulation in LSQC for URB lookup traffic (URB lookups are issued to ltcc these many clocks apart). 00b - Continuous. 01b - 4 clocks apart. 10b - 8 clocks apart. 11b - 16 clocks apart. lbcf_lsqc_urb_traffic.
	27	LQSC RO PERF DIS
		Default Value: 0b
		Access: R/W
		Default: 0. when set, RO performance mode is disabled and all Reads proceed only after Parent recycles. lbcf_csr_lsqc_roperf_dis.

**L3SQCREG4 - L3 SQC register 4**

	26	Order Cam Snp Reject	
		Default Value:	0b
		Access:	R/W
		Default: 0. when set, all slots resulting in matches to snp addr result in snprsp as REJECT instead of MISS. lbcf_csr_lsqc_ordercam_snpreject.	
	25	LQSC RW PERF DIS	
		Default Value:	0b
		Access:	R/W
		Default: 0. 0: Performance mode is enabled. when set, Rd to RW performance mode is disabled and all cycles proceed only after Parent recycles.	
		lbcf_csr_lsqc_rwperf_dis.	
	24	LSQC read rtn local crdt pre-consume disable	
		Default Value:	0b
		Access:	R/W
		0 - Default, LSQD consumes the LNE local slice credit when read return pending. 1 - LSQD consumes read rtn credit in the clock it is ready to send read return data. lbcf_csr_lsqc_rdtrn_precredit_dis.	
	23	LSQC Mem Write sqcam HITM response disable	
		Default Value:	0b
		Access:	R/W
		0 - Default. 1 - This disables any Memory Write from cache with HitM tag response to respond for SQCAMs. lbcf_csr_lsqc_sqcam_l3tagrsphitm_dis.	
	22	Non-IA coherent atomics enable	
		Default Value:	1b
		Access:	R/W
		0: Atomics in GTI. 1: Atomics in L3 (non-IA atomic) (default). lbcf_csr_lsqc_glblatmcs_l3. Value of this bit should be same as LNCf register bit 0xb008[0]. Value of this bit should be same as LBCF register bit 0xb11c[8].	



L3SQCREG4 - L3 SQC register 4

	21	Pipe line flush Coherent lines	
		Default Value:	0b
		Access:	R/W
		1: Treat pipeline flush as invalidating even coherent lines along with non coherent lines . 0: Flush invalidates non coherent lines only. lbcf_csr_lsqc_pipeflush_coh.	
	20:6	Reserved	
		Access:	RO
	5	ltcd b2b 2x dis	
		Default Value:	0b
		Access:	R/W
		0-ltcd b2b 2x feature enabled 1-ltcd b2b 2x feature disabled ltcd_ltcd_b2b_2x_dis	
	4	lslm b2b 2x dis	
		Default Value:	0b
		Access:	R/W
		0-lslm b2b 2x feature enabled 1-lslm b2b 2x feature disabled lbcf_lslm_b2b_2x_dis	
	3	lslm flush denorm	
		Default Value:	0b
		Access:	R/W
		lbcf_csr_lslm_flush_denorm_to_zero When this bit is enabled (1b), Floating Point SLM atomics output will be flushed to zero if it is a De-Norm.	
	2	lsqc disable sla coh	
		Default Value:	0b
		Access:	R/W
		lbcf_lsqc_disable_sla_coh If this bit is set to 1b, it will disable Short loop atomics access for Coherent atomics.	
	1	lsqc disable sla	
		Default Value:	0b
		Access:	R/W
		lbcf_lsqc_disable_sla	

**L3SQCREG4 - L3 SQC register 4**

L3SQCREG4 - L3 SQC register 4			
		If this bit is set to 1b, it will disable Short loop atomics access for Coherent and non-coherent atomics. In BXT, if L3SQCREG4[LTCB_B2B_2X_DIS] (B118[5]) is set to 1, then this bit needs to be set to 1	
0	lsqd flush denorm		
	Default Value:		0b
	Access:		R/W
	lbcf_csr_lsqd_flush_denorm_to_zero When this bit is enabled (1b), Floating Point atomics output will be flushed to zero if it is a De-Norm.		



L3 SQC registers 1

L3SQCREG1 - L3 SQC registers 1			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00E10000			
Size (in bits): 32			
Address: 0B100h			
DWord	Bit	Description	
0	31:24	Reserved	
		Access:	RO
		Reserved.	
	23:19	L3SQ General Priority Credit Initialization	
		Default Value:	11100b
		Access:	R/W
		L3SQ General Priority Credit Initialization (SQGPCI):	
		Number of general and high priority credits that SQ presents to L3 Arbiter blocks This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots.	
		This field can be programmed only after a stalling flush (HSD:2133794/2133796/2134058)	
		Any value not listed here is considered Reserved.	
Gen priority credits is always greater than high priority credits.			
Value			
# General Credits			
00000b			
0			
00001b			
2			
00010b			
4			
00011b			
6			
00100b			
8			
00101b			
10			
00110b			
12			
00111b			
14			
01000b			
16			
01001b			

**L3SQCREG1 - L3 SQC registers 1**

	18 01010b 20 01011b 22 01100b 24 01101b 26 01110b 28 01111b 30 10000b 32 ... 11100b 56 (default) Other values are not possible. Can go up to 62 credits. lbcf_csr_lsqc_gen_credit_init[4:0].				
18:14	L3SQ High Priority Credit Initialization <table><tr><td>Default Value:</td><td>00100b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> L3SQ High Priority Credit Initialization (SQHPCI): Number of general and high priority credits that SQ presents to L3 Arbiter blocks. This inherently also determines the depth of the SQ; reduce the number of credits and SQ uses fewer slots. This field can be programmed only after a stalling flush (HSD:2133794/2133796/2134058) Any value not listed here is considered Reserved. gen priority credits is always greater than high priority credits. Value # High Pri Credits 00000b 0 00001b 2 00010b 4 00011b 6 00100b 8 (default) 00101b 10	Default Value:	00100b	Access:	R/W
Default Value:	00100b				
Access:	R/W				



L3SQCREG1 - L3 SQC registers 1

L3SQCREG1 - L3 SQC registers 1				
		00110b 12 00111b 14 01000b 16 01001b 18 01010b 20 01011b 22 01100b 24 01101b 26 01110b 28 01111b 30 10000b 32 ... 11111b 62 Can to go up to 62 credits for BXT-SOC_BIG. lbcf_csr_lsqc_hp_credit_init[4:0] + lbcf_csr_lsqc_gen_credit_init[4:0] should always be less than or equal to 62(BXT-SOC_BIG). lbcf_csr_lsqc_hp_credit_init[4:0].		
13:10	Reserved	<table><tr><td>Access:</td><td>RO</td></tr></table> Reserved.	Access:	RO
Access:	RO			
9	L3SQ Read Once Enable for Sampler Client	<table><tr><td>Access:</td><td>R/W</td></tr></table> L3SQ Read Once Enable for Sampler Client (SQROE): Enables Read Once indications to L3 Cache from SQ. Once enabled, any reads from Sampler client (MT) are sent as Read Once. 0 = (default) Reads from Sampler clients issue Read to L3 Cache. 1 = Reads from Sampler clients issue Read Once to L3 Cache. lbcf_csr_sampler_readonce_en.	Access:	R/W
Access:	R/W			

**L3SQCREG1 - L3 SQC registers 1**

	8:6	Reserved	
		Access:	RO
		Reserved.	
	5:3	L3SQ Outstanding L3 Fills	
		Access:	R/W
		L3SQ Outstanding L3 Fills (SQOUTSL3F): Identifies the number of L3 Fills that can be outstanding before SQ throttles the fill requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. Once the fill count is greater than or equal to the threshold, then no fills are issued until the fill responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 fill. 010b = 2 fills. 011b = 4 fills. 100b = 8 fills. 101b = 16 fills. 11Xb = Reserved. lbcf_csr_lsqc_outs_fill[2:0].	
	2:0	L3SQ Outstanding L3 Lookups	
		Access:	R/W
		L3SQ Outstanding L3 Lookups (SQOUTSL3L): Identifies the number of L3 lookups that can be outstanding before SQ throttles the lookup requests to L3 Cache. This is not an exact limit, but instead it is used as a threshold to throttling. once the lookup count is greater than or equal to the threshold, then no lookups are issued until the lookup responses are received to bring the outstanding count back below the threshold. 000b = (default) No limit. 001b = 1 lookup. 010b = 2 lookups. 011b = 4 lookups. 100b = 8 lookups. 101b = 16 lookups. 11Xb = Reserved. lbcf_csr_lsqc_outs_lookup[2:0].	



MAILBOX0

MAILBOX0 - MAILBOX0		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 120800h		
This register contains bits 31:0 of the generic descriptor, fetched from the invalidate queue for GT.		
DWord	Bit	Description
0	31:0	DATA
		Default Value: 00000000h
		Access: R/W
		This field contains bits 31:0 of the generic descriptor, fetched from the invalidate queue for GT.



MAILBOX1

MAILBOX1 - MAILBOX1		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 120804h		
This register contains bits 63:32 of the generic descriptor, fetched from the invalidate queue for GT.		
DWord	Bit	Description
0	31:0	DATA
		Default Value: 00000000h
		Access: R/W
		This field contains bits 63:32 of the generic descriptor, fetched from the invalidate queue for GT.



MAILBOX2

MAILBOX2 - MAILBOX2		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 120808h		
This register contains bits 95:64 of the generic descriptor, fetched from the invalidate queue for GT.		
DWord	Bit	Description
0	31:0	DATA
		Default Value: 00000000h
		Access: R/W
		This field contains bits 95:64 of the generic descriptor, fetched from the invalidate queue for GT.



MAILBOX3

MAILBOX3 - MAILBOX3		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 12080Ch		
This register contains bits 127:96 of the generic descriptor, fetched from the invalidate queue for GT.		
DWord	Bit	Description
0	31:0	DATA
		Default Value: 00000000h
		Access: R/W
		This field contains bits 127:96 of the generic descriptor, fetched from the invalidate queue for GT.



Master Latency Timer

MLT2_0_2_0_PCI - Master Latency Timer			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	0000Dh		
The IGD does not support the programmability of the master latency timer because it does not perform bursts.			
DWord	Bit	Description	
0	7:0	Master Latency Timer Count Value	
		Default Value:	00000000b
		Access:	RO
		Hardwired to 0s.	



Maximum Latency

MAXLAT_0_2_0_PCI - Maximum Latency			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	0003Fh		
The Integrated Graphics Device has no requirement for the settings of Latency Timers.			
DWord	Bit	Description	
0	7:0	Maximum Latency Value	
		Default Value:	00000000b
		Access:	RO
		Hardwired to 0s because the IGD has no specific requirements for how often it needs to access the PCI bus.	



MBDSM

MBDSM - MBDSM			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	1080C0h		
This register contains the base address of graphics data stolen DRAM memory. BIOS determines the base of graphics data stolen memory by subtracting the graphics data stolen memory size (PCI Device 0 offset 52 bits 7:4) from TOLUD (PCI Device 0 offset BC bits 31:20).			
DWord	Bit	Description	
0	31:20	BDSM	
		Default Value:	000h
		Access:	RO
		This BitField contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 50 bits 15:8) from TOLUD (PCI Device 0 offset BC bits 31:20).	
	19:1	RESERVED	
		Default Value:	000h
		Access:	RO
		Reserved	
	0	LOCK	
		Default Value:	0b
Access:		RO	
This bit will lock all writeable settings in this register, including itself.			



MBGSM

MBGSM - MBGSM			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00100000	
Size (in bits):		32	
Address:		108100h	
This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 52 bits 9:8) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).			
DWord	Bit	Description	
0	31:20	BGSM	
		Default Value:	001h
		Access:	RO
		This register contains the base address of stolen DRAM memory for the GTT. BIOS determines the base of GTT stolen memory by subtracting the GTT graphics stolen memory size (PCI Device 0 offset 50 bits 7:6) from the Graphics Base of Data Stolen Memory (PCI Device 0 offset B0 bits 31:20).	
	19:1	RESERVED	
		Default Value:	000h
		Access:	RO
		Reserved	
	0	LOCK	
		Default Value:	0b
		Access:	RO
		This bit will lock all writeable settings in this register, including itself.	



MCHBAR_LSB

MCHBAR_LSB - MCHBAR_LSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	06C88h		
This is the base address for the Graphics VT configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the GFX-VT configuration space is disabled and must be enabled by writing a 1 to GFX-VTBAREN. All the bits in this register are locked in Intel TXT mode. BIOS programs this register after which the register cannot be altered.			
DWord	Bit	Description	
0	31:12	GFXVTBAR	
		Default Value:	000000h
		Access:	R/W Lock
		This field corresponds to bits 38 to 12 of the base address GFX-VT configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space. System Software uses this base address to program the GFX-VT register set. All the Bits in this register are locked in Intel TXT mode.	
	11:2	RESERVED	
		Default Value:	000h
		Access:	RO
		Reserved	
	1	LOCK	
		Default Value:	000h
		Access:	R/W Lock
		Lock	
	0	GFXVTBAREN	
		Default Value:	0b
		Access:	R/W Lock
		0: GFX-VTBAR is disabled and does not claim any memory. 1: GFX-VTBAR memory mapped accesses are claimed and decoded appropriately This bit will remain 0 if VTd capability is disabled.	



MCHBAR_MSB

MCHBAR_MSB - MCHBAR_MSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	06C8Ch		
This is the base address for the Graphics VT configuration space. There is no physical memory within this 4KB window that can be addressed. The 4KB reserved by this register does not alias to any PCI 2.3 compliant memory mapped space. On reset, the GFX-VT configuration space is disabled and must be enabled by writing a 1 to GFX-VTBAREN. All the bits in this register are locked in Intel TXT mode. BIOS programs this register after which the register cannot be altered.			
DWord	Bit	Description	
0	31:7	RESERVED	
		Default Value:	0000000h
		Access:	RO
		Reserved	
	6:0	GFXVTBAR	
		Default Value:	00h
		Access:	R/W Lock
		This field corresponds to bits 38 to 12 of the base address GFX-VT configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space.	
		This register ensures that a naturally aligned 4KB space is allocated within the first 512GB of addressable memory space.	
	System Software uses this base address to program the GFX-VT register set. All the Bits in this register are locked in Intel TXT mode.		



Media0 MOCS Register0

MFX0_MOCS_0 - Media0 MOCS Register0			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000030		
Size (in bits):	32		
Address:	0C900h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target		

**MFX0_MOCS_0 - Media0 MOCS Register0**

	Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	Default Value:	11b	Access:	R/W
Default Value:	11b				
Access:	R/W				
3:2	Target Cache <table><tr><td>Default Value:</td><td>00b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	Default Value:	00b	Access:	R/W
Default Value:	00b				
Access:	R/W				



MFX0_MOCS_0 - Media0 MOCS Register0		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register1

MFX0_MOCS_1 - Media0 MOCS Register1			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000034	
Size (in bits):		32	
Address:		0C904h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care Bit[8]=1: address bit[9] needs to be "0" to cache in target		



MFX0_MOCS_1 - Media0 MOCS Register1

MFX0_MOCS_1 - Media0 MOCS Register1		
		Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	01b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	



MFX0_MOCS_1 - Media0 MOCS Register1		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register2

MFX0_MOCS_2 - Media0 MOCS Register2			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000038	
Size (in bits):		32	
Address:		0C908h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx0_MOCS_2 - Media0 MOCS Register2**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_2 - Media0 MOCS Register2		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register3

MFX0_MOCS_3 - Media0 MOCS Register3			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000031	
Size (in bits):		32	
Address:		0C90Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_3 - Media0 MOCS Register3

MFX0_MOCS_3 - Media0 MOCS Register3		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	



MFX0_MOCS_3 - Media0 MOCS Register3		
	1:0	LLC/eDRAM cacheability control
		Default Value: 01b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register4

MFX0_MOCS_4 - Media0 MOCS Register4			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0C910h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx0_MOCS_4 - Media0 MOCS Register4**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_4 - Media0 MOCS Register4		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register5

MFX0_MOCS_5 - Media0 MOCS Register5			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0C914h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_5 - Media0 MOCS Register5

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_5 - Media0 MOCS Register5		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register6

MFX0_MOCS_6 - Media0 MOCS Register6			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x0000003A			
Size (in bits): 32			
Address: 0C918h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFx0_MOCS_6 - Media0 MOCS Register6**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_6 - Media0 MOCS Register6		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register7

MFX0_MOCS_7 - Media0 MOCS Register7			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0C91Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_7 - Media0 MOCS Register7

MFX0_MOCS_7 - Media MOCS Register7		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	



MFX0_MOCS_7 - Media0 MOCS Register7		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register8

MFX0_MOCS_8 - Media0 MOCS Register8			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000037	
Size (in bits):		32	
Address:		0C920h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_8 - Media0 MOCS Register8**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_8 - Media0 MOCS Register8		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register9

MFX0_MOCS_9 - Media0 MOCS Register9			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0C924h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_9 - Media0 MOCS Register9

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_9 - Media0 MOCS Register9		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register10

MFX0_MOCS_10 - Media0 MOCS Register10			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0C928h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_10 - Media0 MOCS Register10**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_10 - Media0 MOCS Register10		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register11

MFX0_MOCS_11 - Media0 MOCS Register11			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0C92Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_11 - Media0 MOCS Register11

MFX0_MOCS_11 - Media0 MOCS Register11		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	01b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFX0_MOCS_11 - Media0 MOCS Register11**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register12

MFX0_MOCS_12 - Media0 MOCS Register12			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x0000003A			
Size (in bits): 32			
Address: 0C930h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_12 - Media0 MOCS Register12**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_12 - Media0 MOCS Register12		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register13

MFX0_MOCS_13 - Media0 MOCS Register13			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0C934h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_13 - Media0 MOCS Register13

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX0_MOCS_13 - Media0 MOCS Register13**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media0 MOCS Register14

MFX0_MOCS_14 - Media0 MOCS Register14			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0C938h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_14 - Media0 MOCS Register14**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_14 - Media0 MOCS Register14		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register15

MFX0_MOCS_15 - Media0 MOCS Register15			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0C93Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_15 - Media0 MOCS Register15

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_15 - Media0 MOCS Register15		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register16

MFX0_MOCS_16 - Media0 MOCS Register16			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000030			
Size (in bits): 32			
Address: 0C940h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 00000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFX0_MOCS_16 - Media0 MOCS Register16**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_16 - Media0 MOCS Register16		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register17

MFX0_MOCS_17 - Media0 MOCS Register17			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000034	
Size (in bits):		32	
Address:		0C944h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_17 - Media0 MOCS Register17

MFX0_MOCS_17 - Media0 MOCS Register17		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	01b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFX0_MOCS_17 - Media0 MOCS Register17**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register18

MFX0_MOCS_18 - Media0 MOCS Register18			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000038			
Size (in bits): 32			
Address: 0C948h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_18 - Media0 MOCS Register18**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_18 - Media0 MOCS Register18		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register19

MFX0_MOCS_19 - Media0 MOCS Register19			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000031	
Size (in bits):		32	
Address:		0C94Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_19 - Media0 MOCS Register19

MFX0_MOCS_19 - Media0 MOCS Register19		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFX0_MOCS_19 - Media0 MOCS Register19**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	01b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register20

MFX0_MOCS_20 - Media0 MOCS Register20			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0C950h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_20 - Media0 MOCS Register20**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_20 - Media0 MOCS Register20		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register21

MFX0_MOCS_21 - Media0 MOCS Register21			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0C954h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_21 - Media0 MOCS Register21

MFX0_MOCS_21 - Media MOCS Register21		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	01b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFX0_MOCS_21 - Media0 MOCS Register21**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register22

MFX0_MOCS_22 - Media0 MOCS Register22			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x0000003A			
Size (in bits): 32			
Address: 0C958h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_22 - Media0 MOCS Register22**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_22 - Media0 MOCS Register22		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register23

MFX0_MOCS_23 - Media0 MOCS Register23			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0C95Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_23 - Media0 MOCS Register23

	Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	Default Value:	11b	Access:	R/W
Default Value:	11b				
Access:	R/W				
3:2	Target Cache <table><tr><td>Default Value:</td><td>00b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	Default Value:	00b	Access:	R/W
Default Value:	00b				
Access:	R/W				

**MFX0_MOCS_23 - Media0 MOCS Register23**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register24

MFX0_MOCS_24 - Media0 MOCS Register24			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000037			
Size (in bits): 32			
Address: 0C960h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFX0_MOCS_24 - Media0 MOCS Register24**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_24 - Media0 MOCS Register24		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register25

MFX0_MOCS_25 - Media0 MOCS Register25			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0C964h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_25 - Media0 MOCS Register25

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX0_MOCS_25 - Media0 MOCS Register25**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media0 MOCS Register26

MFX0_MOCS_26 - Media0 MOCS Register26			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000032			
Size (in bits): 32			
Address: 0C968h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFX0_MOCS_26 - Media0 MOCS Register26**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_26 - Media0 MOCS Register26		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register27

MFX0_MOCS_27 - Media0 MOCS Register27			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0C96Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_27 - Media0 MOCS Register27

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX0_MOCS_27 - Media0 MOCS Register27**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register28

MFX0_MOCS_28 - Media0 MOCS Register28			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0C970h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFX0_MOCS_28 - Media0 MOCS Register28**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_28 - Media0 MOCS Register28		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register29

MFX0_MOCS_29 - Media0 MOCS Register29			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0C974h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_29 - Media0 MOCS Register29

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX0_MOCS_29 - Media0 MOCS Register29**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register30

MFX0_MOCS_30 - Media0 MOCS Register30			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0C978h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_30 - Media0 MOCS Register30**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_30 - Media0 MOCS Register30		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register31

MFX0_MOCS_31 - Media0 MOCS Register31			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0C97Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_31 - Media0 MOCS Register31

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX0_MOCS_31 - Media0 MOCS Register31**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register32

MFX0_MOCS_32 - Media0 MOCS Register32			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000030		
Size (in bits):	32		
Address:	0C980h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFX0_MOCS_32 - Media0 MOCS Register32**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_32 - Media0 MOCS Register32		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register33

MFX0_MOCS_33 - Media0 MOCS Register33			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000034	
Size (in bits):		32	
Address:		0C984h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_33 - Media0 MOCS Register33

	Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	Default Value:	11b	Access:	R/W
Default Value:	11b				
Access:	R/W				
3:2	Target Cache <table><tr><td>Default Value:</td><td>01b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	Default Value:	01b	Access:	R/W
Default Value:	01b				
Access:	R/W				

**MFX0_MOCS_33 - Media0 MOCS Register33**

1:0

LLC/eDRAM cacheability control

Default Value:

00b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media0 MOCS Register34

MFX0_MOCS_34 - Media0 MOCS Register34			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000038		
Size (in bits):	32		
Address:	0C988h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_34 - Media0 MOCS Register34**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_34 - Media0 MOCS Register34		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register35

MFX0_MOCS_35 - Media0 MOCS Register35			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000031	
Size (in bits):		32	
Address:		0C98Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_35 - Media0 MOCS Register35

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target					
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS			Default Value:	0b	Access:	R/W
Default Value:	0b						
Access:	R/W						
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved			Default Value:	11b	Access:	R/W
Default Value:	11b						
Access:	R/W						
3:2	Target Cache <table><tr><td>Default Value:</td><td>00b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed			Default Value:	00b	Access:	R/W
Default Value:	00b						
Access:	R/W						

**MFX0_MOCS_35 - Media0 MOCS Register35**

1:0

LLC/eDRAM cacheability control

Default Value:

01b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media0 MOCS Register36

MFX0_MOCS_36 - Media0 MOCS Register36			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0C990h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_36 - Media0 MOCS Register36**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_36 - Media0 MOCS Register36		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register37

MFX0_MOCS_37 - Media0 MOCS Register37			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0C994h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_37 - Media0 MOCS Register37

MFX0_MOCS_37 - Media0 MOCS Register37		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	01b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	



MFX0_MOCS_37 - Media0 MOCS Register37		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register38

MFX0_MOCS_38 - Media0 MOCS Register38			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0C998h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_38 - Media0 MOCS Register38**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_38 - Media0 MOCS Register38		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register39

MFX0_MOCS_39 - Media0 MOCS Register39			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0C99Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_39 - Media0 MOCS Register39

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX0_MOCS_39 - Media0 MOCS Register39**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register40

MFX0_MOCS_40 - Media0 MOCS Register40			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0C9A0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_40 - Media0 MOCS Register40**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_40 - Media0 MOCS Register40		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register41

MFX0_MOCS_41 - Media0 MOCS Register41			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0C9A4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_41 - Media0 MOCS Register41

	Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	Default Value:	11b	Access:	R/W
Default Value:	11b				
Access:	R/W				
3:2	Target Cache <table><tr><td>Default Value:</td><td>10b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	Default Value:	10b	Access:	R/W
Default Value:	10b				
Access:	R/W				



MFX0_MOCS_41 - Media0 MOCS Register41		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register42

MFX0_MOCS_42 - Media0 MOCS Register42			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000032			
Size (in bits): 32			
Address: 0C9A8h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_42 - Media0 MOCS Register42**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_42 - Media0 MOCS Register42		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register43

MFX0_MOCS_43 - Media0 MOCS Register43			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0C9ACh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_43 - Media0 MOCS Register43

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX0_MOCS_43 - Media0 MOCS Register43**

1:0

LLC/eDRAM cacheability control

Default Value:

10b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media0 MOCS Register44

MFX0_MOCS_44 - Media0 MOCS Register44			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x0000003A			
Size (in bits): 32			
Address: 0C9B0h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_44 - Media0 MOCS Register44**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_44 - Media0 MOCS Register44		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register45

MFX0_MOCS_45 - Media0 MOCS Register45			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0C9B4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_45 - Media0 MOCS Register45

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_45 - Media0 MOCS Register45		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register46

MFX0_MOCS_46 - Media0 MOCS Register46			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000037			
Size (in bits): 32			
Address: 0C9B8h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care			

**MFX0_MOCS_46 - Media0 MOCS Register46**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_46 - Media0 MOCS Register46		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register47

MFX0_MOCS_47 - Media0 MOCS Register47			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0C9BCh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_47 - Media0 MOCS Register47

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX0_MOCS_47 - Media0 MOCS Register47**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media0 MOCS Register48

MFX0_MOCS_48 - Media0 MOCS Register48			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000030		
Size (in bits):	32		
Address:	0C9C0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_48 - Media0 MOCS Register48**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_48 - Media0 MOCS Register48		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register49

MFX0_MOCS_49 - Media0 MOCS Register49			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000034	
Size (in bits):		32	
Address:		0C9C4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_49 - Media0 MOCS Register49

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX0_MOCS_49 - Media0 MOCS Register49**

1:0

LLC/eDRAM cacheability control

Default Value:

00b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media0 MOCS Register50

MFX0_MOCS_50 - Media0 MOCS Register50			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000038		
Size (in bits):	32		
Address:	0C9C8h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_50 - Media0 MOCS Register50**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_50 - Media0 MOCS Register50		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register51

MFX0_MOCS_51 - Media0 MOCS Register51			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000031		
Size (in bits):	32		
Address:	0C9CCh		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_51 - Media0 MOCS Register51

	Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	Default Value:	11b	Access:	R/W
Default Value:	11b				
Access:	R/W				
3:2	Target Cache <table><tr><td>Default Value:</td><td>00b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	Default Value:	00b	Access:	R/W
Default Value:	00b				
Access:	R/W				

**MFX0_MOCS_51 - Media0 MOCS Register51**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	01b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register52

MFX0_MOCS_52 - Media0 MOCS Register52			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0C9D0h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_52 - Media0 MOCS Register52**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_52 - Media0 MOCS Register52		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register53

MFX0_MOCS_53 - Media0 MOCS Register53			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0C9D4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_53 - Media0 MOCS Register53

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX0_MOCS_53 - Media0 MOCS Register53**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register54

MFX0_MOCS_54 - Media0 MOCS Register54			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0C9D8h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_54 - Media0 MOCS Register54**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_54 - Media0 MOCS Register54		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register55

MFX0_MOCS_55 - Media0 MOCS Register55			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0C9DCh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_55 - Media0 MOCS Register55

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX0_MOCS_55 - Media0 MOCS Register55**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media0 MOCS Register56

MFX0_MOCS_56 - Media0 MOCS Register56			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0C9E0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_56 - Media0 MOCS Register56**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_56 - Media0 MOCS Register56		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register57

MFX0_MOCS_57 - Media0 MOCS Register57			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0C9E4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_57 - Media0 MOCS Register57

MFX0_MOCS_57 - Media0 MOCS Register57		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	10b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFX0_MOCS_57 - Media0 MOCS Register57**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register58

MFX0_MOCS_58 - Media0 MOCS Register58			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000032			
Size (in bits): 32			
Address: 0C9E8h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFX0_MOCS_58 - Media0 MOCS Register58**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_58 - Media0 MOCS Register58		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register59

MFX0_MOCS_59 - Media0 MOCS Register59			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0C9ECh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_59 - Media0 MOCS Register59

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX0_MOCS_59 - Media0 MOCS Register59**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register60

MFX0_MOCS_60 - Media0 MOCS Register60			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x0000003A			
Size (in bits): 32			
Address: 0C9F0h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFX0_MOCS_60 - Media0 MOCS Register60**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_60 - Media0 MOCS Register60		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register61

MFX0_MOCS_61 - Media0 MOCS Register61			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0C9F4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_61 - Media0 MOCS Register61

MFX0_MOCS_61 - Media0 MOCS Register61		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFX0_MOCS_61 - Media0 MOCS Register61**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media0 MOCS Register62

MFX0_MOCS_62 - Media0 MOCS Register62			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000037			
Size (in bits): 32			
Address: 0C9F8h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX0_MOCS_62 - Media0 MOCS Register62**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX0_MOCS_62 - Media0 MOCS Register62		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media0 MOCS Register63

MFX0_MOCS_63 - Media0 MOCS Register63			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0C9FCh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX0_MOCS_63 - Media0 MOCS Register63

MFX0_MOCS_63 - Media0 MOCS Register63		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	10b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFX0_MOCS_63 - Media0 MOCS Register63**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media1 MOCS Register0

MFX1_MOCS_0 - Media1 MOCS Register0			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000030		
Size (in bits):	32		
Address:	0CA00h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_0 - Media1 MOCS Register0**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_0 - Media1 MOCS Register0		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register1

MFX1_MOCS_1 - Media1 MOCS Register1			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000034	
Size (in bits):		32	
Address:		0CA04h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_1 - Media1 MOCS Register1

MFX1_MOCS_1 - Media1 MOCS Register1		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	01b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	



MFX1_MOCS_1 - Media1 MOCS Register1		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register2

MFX1_MOCS_2 - Media1 MOCS Register2			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000038	
Size (in bits):		32	
Address:		0CA08h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_2 - Media1 MOCS Register2**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_2 - Media1 MOCS Register2		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register3

MFX1_MOCS_3 - Media1 MOCS Register3			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000031	
Size (in bits):		32	
Address:		0CA0Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_3 - Media1 MOCS Register3

MFX1_MOCS_3 - Media1 MOCS Register3		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	



MFX1_MOCS_3 - Media1 MOCS Register3		
	1:0	LLC/eDRAM cacheability control
		Default Value: 01b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register4

MFX1_MOCS_4 - Media1 MOCS Register4			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0CA10h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_4 - Media1 MOCS Register4**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_4 - Media1 MOCS Register4		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register5

MFX1_MOCS_5 - Media1 MOCS Register5			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CA14h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_5 - Media1 MOCS Register5

MFX1_MOCS_5 - Media1 MOCS Register5		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	01b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	



MFX1_MOCS_5 - Media1 MOCS Register5		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register6

MFX1_MOCS_6 - Media1 MOCS Register6			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0CA18h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_6 - Media1 MOCS Register6**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_6 - Media1 MOCS Register6		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register7

MFX1_MOCS_7 - Media1 MOCS Register7			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CA1Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_7 - Media1 MOCS Register7

MFX1_MOCS_7 - Media1 MOCS Register7		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFx1_MOCS_7 - Media1 MOCS Register7**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register8

MFX1_MOCS_8 - Media1 MOCS Register8			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000037	
Size (in bits):		32	
Address:		0CA20h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_8 - Media1 MOCS Register8**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_8 - Media1 MOCS Register8		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register9

MFX1_MOCS_9 - Media1 MOCS Register9			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CA24h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_9 - Media1 MOCS Register9

MFX1_MOCS_9 - Media1 MOCS Register9		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	10b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	



MFX1_MOCS_9 - Media1 MOCS Register9		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register10

MFX1_MOCS_10 - Media1 MOCS Register10			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000032			
Size (in bits): 32			
Address: 0CA28h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_10 - Media1 MOCS Register10**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_10 - Media1 MOCS Register10		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register11

MFX1_MOCS_11 - Media1 MOCS Register11			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CA2Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_11 - Media1 MOCS Register11

MFX1_MOCS_11 - Media1 MOCS Register11		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	01b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFX1_MOCS_11 - Media1 MOCS Register11**

1:0

LLC/eDRAM cacheability control

Default Value:

10b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register12

MFX1_MOCS_12 - Media1 MOCS Register12			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CA30h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX1_MOCS_12 - Media1 MOCS Register12**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_12 - Media1 MOCS Register12		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register13

MFX1_MOCS_13 - Media1 MOCS Register13			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CA34h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_13 - Media1 MOCS Register13

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		Default Value:	11b	Access:	R/W
Default Value:	11b					
Access:	R/W					
3:2	Target Cache <table><tr><td>Default Value:</td><td>00b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		Default Value:	00b	Access:	R/W
Default Value:	00b					
Access:	R/W					

**MFx1_MOCS_13 - Media1 MOCS Register13**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register14

MFX1_MOCS_14 - Media1 MOCS Register14			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0CA38h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX1_MOCS_14 - Media1 MOCS Register14**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_14 - Media1 MOCS Register14		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register15

MFX1_MOCS_15 - Media1 MOCS Register15			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CA3Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_15 - Media1 MOCS Register15

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX1_MOCS_15 - Media1 MOCS Register15**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register16

MFX1_MOCS_16 - Media1 MOCS Register16			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000030	
Size (in bits):		32	
Address:		0CA40h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX1_MOCS_16 - Media1 MOCS Register16**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_16 - Media1 MOCS Register16		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register17

MFX1_MOCS_17 - Media1 MOCS Register17			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000034	
Size (in bits):		32	
Address:		0CA44h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_17 - Media1 MOCS Register17

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFx1_MOCS_17 - Media1 MOCS Register17**

1:0

LLC/eDRAM cacheability control

Default Value:

00b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register18

MFX1_MOCS_18 - Media1 MOCS Register18			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000038			
Size (in bits): 32			
Address: 0CA48h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFX1_MOCS_18 - Media1 MOCS Register18**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_18 - Media1 MOCS Register18		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register19

MFX1_MOCS_19 - Media1 MOCS Register19			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000031	
Size (in bits):		32	
Address:		0CA4Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_19 - Media1 MOCS Register19

MFX1_MOCS_19 - Media1 MOCS Register19		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFx1_MOCS_19 - Media1 MOCS Register19**

1:0

LLC/eDRAM cacheability control

Default Value:

01b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register20

MFX1_MOCS_20 - Media1 MOCS Register20			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0CA50h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_20 - Media1 MOCS Register20**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_20 - Media1 MOCS Register20		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register21

MFX1_MOCS_21 - Media1 MOCS Register21			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CA54h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_21 - Media1 MOCS Register21

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_21 - Media1 MOCS Register21		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register22

MFX1_MOCS_22 - Media1 MOCS Register22			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x0000003A			
Size (in bits): 32			
Address: 0CA58h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_22 - Media1 MOCS Register22**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_22 - Media1 MOCS Register22		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register23

MFX1_MOCS_23 - Media1 MOCS Register23			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CA5Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_23 - Media1 MOCS Register23

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX1_MOCS_23 - Media1 MOCS Register23**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media1 MOCS Register24

MFX1_MOCS_24 - Media1 MOCS Register24			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0CA60h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_24 - Media1 MOCS Register24**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_24 - Media1 MOCS Register24		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register25

MFX1_MOCS_25 - Media1 MOCS Register25			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CA64h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_25 - Media1 MOCS Register25

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFx1_MOCS_25 - Media1 MOCS Register25**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media1 MOCS Register26

MFX1_MOCS_26 - Media1 MOCS Register26			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0CA68h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX1_MOCS_26 - Media1 MOCS Register26**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_26 - Media1 MOCS Register26		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register27

MFX1_MOCS_27 - Media1 MOCS Register27			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CA6Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_27 - Media1 MOCS Register27

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFx1_MOCS_27 - Media1 MOCS Register27**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media1 MOCS Register28

MFX1_MOCS_28 - Media1 MOCS Register28			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CA70h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX1_MOCS_28 - Media1 MOCS Register28**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_28 - Media1 MOCS Register28		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register29

MFX1_MOCS_29 - Media1 MOCS Register29			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CA74h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_29 - Media1 MOCS Register29

MFX1_MOCS_29 - Media1 MOCS Register29		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFX1_MOCS_29 - Media1 MOCS Register29**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register30

MFX1_MOCS_30 - Media1 MOCS Register30			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000037			
Size (in bits): 32			
Address: 0CA78h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFx1_MOCS_30 - Media1 MOCS Register30**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_30 - Media1 MOCS Register30		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register31

MFX1_MOCS_31 - Media1 MOCS Register31			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CA7Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_31 - Media1 MOCS Register31

MFX1_MOCS_31 - Media1 MOCS Register31		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	10b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	



MFX1_MOCS_31 - Media1 MOCS Register31		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register32

MFX1_MOCS_32 - Media1 MOCS Register32			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000030		
Size (in bits):	32		
Address:	0CA80h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX1_MOCS_32 - Media1 MOCS Register32**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_32 - Media1 MOCS Register32		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register33

MFX1_MOCS_33 - Media1 MOCS Register33			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000034	
Size (in bits):		32	
Address:		0CA84h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_33 - Media1 MOCS Register33

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFx1_MOCS_33 - Media1 MOCS Register33**

1:0

LLC/eDRAM cacheability control

Default Value:

00b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register34

MFX1_MOCS_34 - Media1 MOCS Register34			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000038			
Size (in bits): 32			
Address: 0CA88h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFX1_MOCS_34 - Media1 MOCS Register34**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_34 - Media1 MOCS Register34		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register35

MFX1_MOCS_35 - Media1 MOCS Register35			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000031	
Size (in bits):		32	
Address:		0CA8Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_35 - Media1 MOCS Register35

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFx1_MOCS_35 - Media1 MOCS Register35**

1:0

LLC/eDRAM cacheability control

Default Value:

01b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register36

MFX1_MOCS_36 - Media1 MOCS Register36			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0CA90h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX1_MOCS_36 - Media1 MOCS Register36**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_36 - Media1 MOCS Register36		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register37

MFX1_MOCS_37 - Media1 MOCS Register37			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CA94h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_37 - Media1 MOCS Register37

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_37 - Media1 MOCS Register37		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register38

MFX1_MOCS_38 - Media1 MOCS Register38			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CA98h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX1_MOCS_38 - Media1 MOCS Register38**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_38 - Media1 MOCS Register38		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register39

MFX1_MOCS_39 - Media1 MOCS Register39			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CA9Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_39 - Media1 MOCS Register39

MFX1_MOCS_39 - Media1 MOCS Register39		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	



MFX1_MOCS_39 - Media1 MOCS Register39		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register40

MFX1_MOCS_40 - Media1 MOCS Register40			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000037			
Size (in bits): 32			
Address: 0CAA0h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFx1_MOCS_40 - Media1 MOCS Register40**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_40 - Media1 MOCS Register40		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register41

MFX1_MOCS_41 - Media1 MOCS Register41			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CAA4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_41 - Media1 MOCS Register41

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFx1_MOCS_41 - Media1 MOCS Register41**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register42

MFX1_MOCS_42 - Media1 MOCS Register42			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000032			
Size (in bits): 32			
Address: 0CAA8h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_42 - Media1 MOCS Register42**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_42 - Media1 MOCS Register42		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register43

MFX1_MOCS_43 - Media1 MOCS Register43			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CAACH	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_43 - Media1 MOCS Register43

	Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	Default Value:	11b	Access:	R/W
Default Value:	11b				
Access:	R/W				
3:2	Target Cache <table><tr><td>Default Value:</td><td>01b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	Default Value:	01b	Access:	R/W
Default Value:	01b				
Access:	R/W				



MFX1_MOCS_43 - Media1 MOCS Register43		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register44

MFX1_MOCS_44 - Media1 MOCS Register44			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0CAB0h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_44 - Media1 MOCS Register44**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_44 - Media1 MOCS Register44		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register45

MFX1_MOCS_45 - Media1 MOCS Register45			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CAB4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_45 - Media1 MOCS Register45

MFX1_MOCS_45 - Media1 MOCS Register45		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	



MFX1_MOCS_45 - Media1 MOCS Register45		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register46

MFX1_MOCS_46 - Media1 MOCS Register46			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0CAB8h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_46 - Media1 MOCS Register46**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_46 - Media1 MOCS Register46		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register47

MFX1_MOCS_47 - Media1 MOCS Register47			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CABCh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_47 - Media1 MOCS Register47

MFX1_MOCS_47 - Media1 MOCS Register47		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	10b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFx1_MOCS_47 - Media1 MOCS Register47**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register48

MFX1_MOCS_48 - Media1 MOCS Register48			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000030			
Size (in bits): 32			
Address: 0CAC0h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX1_MOCS_48 - Media1 MOCS Register48**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching	Default Value:	0b
		Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss	Default Value:	0b
		Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management	Default Value:	11b
		Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache	Default Value:	00b
		Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_48 - Media1 MOCS Register48		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register49

MFX1_MOCS_49 - Media1 MOCS Register49			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000034	
Size (in bits):		32	
Address:		0CAC4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_49 - Media1 MOCS Register49

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX1_MOCS_49 - Media1 MOCS Register49**

1:0

LLC/eDRAM cacheability control

Default Value:

00b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register50

MFX1_MOCS_50 - Media1 MOCS Register50			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000038			
Size (in bits): 32			
Address: 0CAC8h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 00000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX1_MOCS_50 - Media1 MOCS Register50**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_50 - Media1 MOCS Register50		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register51

MFX1_MOCS_51 - Media1 MOCS Register51			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000031		
Size (in bits):	32		
Address:	0CACCh		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_51 - Media1 MOCS Register51

MFX1_MOCS_51 - Media1 MOCS Register51		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFx1_MOCS_51 - Media1 MOCS Register51**

1:0

LLC/eDRAM cacheability control

Default Value:

01b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register52

MFX1_MOCS_52 - Media1 MOCS Register52			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0CAD0h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_52 - Media1 MOCS Register52**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_52 - Media1 MOCS Register52		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register53

MFX1_MOCS_53 - Media1 MOCS Register53			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CAD4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_53 - Media1 MOCS Register53

MFX1_MOCS_53 - Media1 MOCS Register53		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	01b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	



MFX1_MOCS_53 - Media1 MOCS Register53		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register54

MFX1_MOCS_54 - Media1 MOCS Register54			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0CAD8h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_54 - Media1 MOCS Register54**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_54 - Media1 MOCS Register54		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register55

MFX1_MOCS_55 - Media1 MOCS Register55			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CADCh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_55 - Media1 MOCS Register55

MFX1_MOCS_55 - Media1 MOCS Register55		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFX1_MOCS_55 - Media1 MOCS Register55**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media1 MOCS Register56

MFX1_MOCS_56 - Media1 MOCS Register56			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0CAE0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX1_MOCS_56 - Media1 MOCS Register56**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_56 - Media1 MOCS Register56		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register57

MFX1_MOCS_57 - Media1 MOCS Register57			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CAE4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_57 - Media1 MOCS Register57

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_57 - Media1 MOCS Register57		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register58

MFX1_MOCS_58 - Media1 MOCS Register58			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000032			
Size (in bits): 32			
Address: 0CAE8h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**MFx1_MOCS_58 - Media1 MOCS Register58**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_58 - Media1 MOCS Register58		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register59

MFX1_MOCS_59 - Media1 MOCS Register59			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CAECh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_59 - Media1 MOCS Register59

MFX1_MOCS_59 - Media1 MOCS Register59		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	01b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFX1_MOCS_59 - Media1 MOCS Register59**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media1 MOCS Register60

MFX1_MOCS_60 - Media1 MOCS Register60			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x0000003A			
Size (in bits): 32			
Address: 0CAF0h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFx1_MOCS_60 - Media1 MOCS Register60**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_60 - Media1 MOCS Register60		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register61

MFX1_MOCS_61 - Media1 MOCS Register61			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CAF4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_61 - Media1 MOCS Register61

MFX1_MOCS_61 - Media1 MOCS Register61		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	00b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**MFX1_MOCS_61 - Media1 MOCS Register61**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Media1 MOCS Register62

MFX1_MOCS_62 - Media1 MOCS Register62			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000037			
Size (in bits): 32			
Address: 0CAF8h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**MFX1_MOCS_62 - Media1 MOCS Register62**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



MFX1_MOCS_62 - Media1 MOCS Register62		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



Media1 MOCS Register63

MFX1_MOCS_63 - Media1 MOCS Register63			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CAFCh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



MFX1_MOCS_63 - Media1 MOCS Register63

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**MFX1_MOCS_63 - Media1 MOCS Register63**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



Media 1 PFET control register with lock

PFETCTL - Media 1 PFET control register with lock		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x0005000A 0x0007000A	
Size (in bits):	32	
Address:	24088h	
DWord	Bit	Description
0	31	PFET Control Lock
		Access: R/W Lock 0 = Bits of MEDIA1 PGFETCTL register are R/W 1 = All bits of MEDIA1 PGFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	Reserved
		Access: RO Reserved
	20	Power Well Status
19	Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.	
	Powergood timer error	
18:16	Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (that is, writing a 0 will not clear the lock). These bits are not reset on FLR.	
	Delay from enabling secondary PFETs to power good.	
	Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns	

**PFETCTL - Media 1 PFET control register with lock**

		3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns	
		Value	Name
		101b	[Default]
	15:13	Time period last primay pfet strobe to secondary pfet strobe	
		Access:	R/W Lock
		Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
	12:10	Time period b/w two adjacent strobes	
		Access:	R/W Lock
		Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
	9:7	FET setup margin from enable to strobe	
		Access:	R/W Lock
		Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
	6:0	Number of flops to enable primary FETs	
		Access:	R/W Lock
		Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed	
		Value	Name
		0001010b	[Default]



MEMRR_BASE_LSB

MEMRR_BASE_LSB - MEMRR_BASE_LSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	108340h		
The EMRR range is used to protect Xucode memory from unauthorized reads and writes. Any IO access to this range is aborted. This register controls the location of the EMRR range by indicating its starting address. It functions in tandem with the EMRR mask register.			
DWord	Bit	Description	
0	31:12	RANGE_BASE	
		Default Value:	0000000h
		Access:	RO
		This field corresponds to bits 38:12 of the base address memory range which is allocated to EMRR memory.	
	11:0	RESERVED	
		Default Value:	000h
		Access:	RO
Reserved			



MEMRR_BASE_MSB

MEMRR_BASE_MSB - MEMRR_BASE_MSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	108344h		
The EMRR range is used to protect Xucode memory from unauthorized reads and writes. Any IO access to this range is aborted. This register controls the location of the EMRR range by indicating its starting address. It functions in tandem with the EMRR mask register.			
DWord	Bit	Description	
0	31:7	RESERVED	
		Default Value:	00000000h
		Access:	RO
		Reserved	
	6:0	RANGE_BASE	
		Default Value:	000h
		Access:	RO
		This field corresponds to bits 38:12 of the base address memory range which is allocated to EMRR memory.	



MEMRR_MASK_LSB

MEMRR_MASK_LSB - MEMRR_MASK_LSB			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000000	
Size (in bits):		32	
Address:		108380h	
This register controls the size of the EMRR range by indicating which address bits must match the EMRR base register value.			
DWord	Bit	Description	
0	31:12	RANGE_BASE	
		Default Value:	0000000h
		Access:	RO
		This field indicates which address bits must match EMRR base in order to qualify as an EMRR access.	
	11	RANGE_EN	
		Default Value:	0b
		Access:	RO
		Indicates whether the EMRR range is enabled and valid.	
	10	LOCK	
		Default Value:	0b
		Access:	RO
		Setting this bit locks all writeable settings in this register, including itself.	
	9:0	RESERVED	
		Default Value:	000h
		Access:	R/W
		Reserved	



MEMRR_MASK_MSB

MEMRR_MASK_MSB - MEMRR_MASK_MSB			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000000			
Size (in bits): 32			
Address: 108384h			
This register controls the size of the EMRR range by indicating which address bits must match the EMRR base register value.			
DWord	Bit	Description	
0	31:7	RESERVED	
		Default Value:	00000000h
		Access:	RO
		Reserved	
	6:0	RANGE_MASK	
		Default Value:	000h
		Access:	RO
		This field indicates which address bits must match EMRR base in order to qualify as an EMRR access.	



Message Address

MA_0_2_0_PCI - Message Address			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	000B0h		
This register contains the Message Address for MSIs sent by the device.			
DWord	Bit	Description	
0	31:2	Message Address	
		Default Value:	000000000000000000000000000000b
		Access:	R/W
		Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.	
	1:0	Force Dword Align	
		Default Value:	00b
		Access:	RO
		Hardwired to 0 so that addresses assigned by system software are always aligned on a DWORD address boundary.	



Message Control

MC_0_2_0_PCI - Message Control			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	16		
Address:	000AEh		
Message Signaled Interrupt control register. System software can modify bits in this register, but the device is prohibited from doing so. If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.			
DWord	Bit	Description	
0	15:8	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	7	64 Bit Capable	
		Default Value:	0b
		Access:	RO
		Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message address register and is incapable of generating a 64-bit memory address.	
	6:4	Multiple Message Enable	
		Default Value:	000b
		Access:	R/W
		System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested.	
		Value: Number of requests	
		000: 1	
		001: 2	
		010: 4	
011: 8			
100: 16			
101: 32			
110: Reserved			
111: Reserved			
3:1	Multiple Message Capable		
	Default Value:	000b	
	Access:	RO	
	System Software reads this field to determine the number of messages being requested by this device.		



MC_0_2_0_PCI - Message Control			
		Hardwired to 000b to indicate number of requests is 1.	
	0	MSI Enable	
		Default Value:	0b
		Access:	R/W
		Controls the ability of this device to generate MSIs.	



Message Data

MD_0_2_0_PCI - Message Data			
Register Space:		PCI: 0/2/0	
Source:		BSpec	
Default Value:		0x00000000	
Size (in bits):		16	
Address:		000B4h	
This register contains the Message Data for MSIs sent by the device.			
DWord	Bit	Description	
0	15:0	MESSDATA	
		Default Value:	0000000000000000b
		Access:	R/W
		Base message data pattern assigned by system software and used to handle an MSI from the device.	
		When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.	



Message Signaled Interrupts Capability ID

MSI_CAPID_0_2_0_PCI - Message Signaled Interrupts Capability ID			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x0000D005		
Size (in bits):	16		
Address:	000ACh		
When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.			
DWord	Bit	Description	
0	15:8	Pointer to Next Capability	
		Default Value:	11010000b
		Access:	RO
		This is a hardwired pointer to the next item in the capabilities list.	
	7:0	Capability ID	
		Default Value:	00000101b
		Access:	RO
		This field is hardwired to the value 05h to identify the CAP_ID as being for MSI registers.	



MGCMD

MGCMD - MGCMD			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	108300h		
Mirror GT hardware uses for Vtd state.			
DWord	Bit	Description	
0	31	TE	
		Default Value:	0b
		Access:	R/W
		0: Disable Vtd DMA remapping 1: Enable Vtd DMA remapping	
	30	SPARE1	
		Default Value:	0b
		Access:	R/W
		Reserved. No hardware usage model.	
	29	SPARE2	
		Default Value:	0b
		Access:	R/W
		Reserved. No hardware usage model.	
	28	SPARE3	
		Default Value:	0b
		Access:	R/W
		Reserved. No hardware usage model.	
	27	SPARE4	
		Default Value:	0b
		Access:	R/W
		Reserved. No hardware usage model.	
	26	SPARE5	
		Default Value:	0b



MGCMD - MGCMD			
		Access:	R/W
		Reserved. No hardware usage model.	
	25	Reserved	
	24	SPARE6	
		Default Value:	0b
		Access:	R/W
		Reserved. No HW usage model.	
	23	SPARE7	
		Default Value:	0b
		Access:	R/W
		Reserved. No HW usage model.	
	22:0	RESERVED	
		Default Value:	00000000h
		Access:	RO
		Reserved	



Minimum Grant

MINGNT_0_2_0_PCI - Minimum Grant			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	0003Eh		
The Integrated Graphics Device has no requirement for the settings of Latency Timers.			
DWord	Bit	Description	
0	7:0	Minimum Grant Value	
		Default Value:	00000000b
		Access:	RO
		Hardwired to 0s because the IGD does not burst as a PCI compliant master.	



MIPI_AUTOPWG

MIPI_AUTOPWG		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B0C8h-6B0CBh	
Name:	MIPIA_AUTOPWG	
ShortName:	MIPIA_AUTOPWG	
Power:	PG1	
Reset:	soft	
Address:	6B8C8h-6B8CBh	
Name:	MIPIC_AUTOPWG	
ShortName:	MIPIC_AUTOPWG	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:1	RESERVED
		Format: MBZ
	0	MIPI_AUTO_PWG_ENABLE
		Access: R/W SW driver writes to this bit to enable auto power gating for MIPI



MIPI_CLK_LANE_SWITCHING_TIME_CNT

MIPI_CLK_LANE_SWITCHING_TIME_CNT					
Register Space:		MMIO: 0/2/0			
Source:		BSpec			
Default Value:		0x00000000			
Access:		R/W			
Size (in bits):		32			
Address:		6B088h-6B08Bh			
Name:		MIPIA_CLK_LANE_SWITCHING_TIME_CNT			
ShortName:		MIPIA_CLK_LANE_SWITCHING_TIME_CNT			
Power:		PG1			
Reset:		soft			
Address:		6B888h-6B88Bh			
Name:		MIPIC_CLK_LANE_SWITCHING_TIME_CNT			
ShortName:		MIPIC_CLK_LANE_SWITCHING_TIME_CNT			
Power:		PG1			
Reset:		soft			
DWord	Bit	Description			
0	31:16	LS_HS_SSW_CNT			
		<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs</td></tr></table>	Access:	R/W	Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs
	Access:	R/W			
	Low power to high speed switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks required to switch from low power mode to high speed mode after txrequesths_clk is asserted. Current Value is ah = 10 txbyteclkhs				
15:0	HS_LS_PWR_SW_CNT				
	<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is de-asserted. Current Value is 14h = 20 txbyteclkhs</td></tr></table>	Access:	R/W	High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is de-asserted. Current Value is 14h = 20 txbyteclkhs	
Access:	R/W				
High speed to low power switching time in terms byte clock (txbyteclkhs). This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc). Typical value - Number of byte clocks request to switch from high speed mode to low power mode after txrequesths_clk is de-asserted. Current Value is 14h = 20 txbyteclkhs					



MIPI_CLOCK_CTL

MIPI_CLOCK_CTL			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x6C006C00		
Access:	R/W		
Size (in bits):	32		
Address:	46090h-46093h		
Name:	MIPI Clock Control		
ShortName:	MIPI_CLOCK_CTL		
Power:	Always on		
Reset:	soft		
This register configures the additional MIPI clock dividers. MIPI1 fields are used for transcoder MIPI A. MIPI2 fields are used for transcoder MIPI C.			
Restriction			
Restriction : The Tx escape clock must be as close as possible to, but not exceeding, 20 MHz.			
Restriction : The Rx escape clock must be programmed to be as close as possible to, but not exceeding, 150 MHz.			
DWord	Bit	Description	
0	31:26	MIPI1 Variable Divider	
		Default Value:	011011b
		Description	
		Tx Escape Clock Divider: This field specifies the amount to divide the MIPI 8X clock to create the Tx escape clock. Program with the desired value -1.	
	25	Spare 25	
	24	Spare 24	
	23	Spare 23	
	22:21	MIPI1 Controller Divider	
		Description	
		Rx Escape Clock Divider Upper: This field, concatenated with Rx Escape Clock Divider Lower value, specifies the amount to divide the MIPI 8X clock to create the RX escape clock. Program the combined value of the upper and lower fields with the desired value -1.	
	20:19	MIPI1 8by3X Divider	
		Description	
		This field specifies the amount to divide the MIPI 8X clock to create the MIPI 8/3X clock.	



MIPI_CLOCK_CTL																		
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>00b</td><td>Reserved</td><td></td></tr><tr><td>01b</td><td>Divide by 2</td><td></td></tr><tr><td>10b</td><td>Divide by 3</td><td>Use divide by 3 for both DPI and DBI modes</td></tr><tr><td>11b</td><td>Divide by 4</td><td></td></tr></table>	Value	Name	Description	00b	Reserved		01b	Divide by 2		10b	Divide by 3	Use divide by 3 for both DPI and DBI modes	11b	Divide by 4		
	Value	Name	Description															
	00b	Reserved																
	01b	Divide by 2																
	10b	Divide by 3	Use divide by 3 for both DPI and DBI modes															
	11b	Divide by 4																
	18	Spare 18																
	17:16	MIPI1 DPHY Divider																
		<table><tr><th>Description</th></tr><tr><td>Rx Escape Clock Divider Lower: This field, concatenated with Rx Escape Clock Divider Upper value, specifies the amount to divide the MIPI 8X clock to create the RX escape clock. Program the combined value of the upper and lower fields with the desired value -1.</td></tr></table>			Description	Rx Escape Clock Divider Lower: This field, concatenated with Rx Escape Clock Divider Upper value, specifies the amount to divide the MIPI 8X clock to create the RX escape clock. Program the combined value of the upper and lower fields with the desired value -1.												
	Description																	
	Rx Escape Clock Divider Lower: This field, concatenated with Rx Escape Clock Divider Upper value, specifies the amount to divide the MIPI 8X clock to create the RX escape clock. Program the combined value of the upper and lower fields with the desired value -1.																	
	15:10	MIPI2 Variable Divider																
		Default Value:	011011b Divide by 28															
		<table><tr><th>Description</th></tr><tr><td>Tx Escape Clock Divider: This field specifies the amount to divide the MIPI 8X clock to create the Tx escape clock. Program with the desired value -1.</td></tr></table>			Description	Tx Escape Clock Divider: This field specifies the amount to divide the MIPI 8X clock to create the Tx escape clock. Program with the desired value -1.												
	Description																	
	Tx Escape Clock Divider: This field specifies the amount to divide the MIPI 8X clock to create the Tx escape clock. Program with the desired value -1.																	
	9	Spare 9																
	8	Spare 8																
	7	Spare 7																
6:5	MIPI2 Controller Divider																	
	<table><tr><th>Description</th></tr><tr><td>Rx Escape Clock Divider Upper: This field, concatenated with Rx Escape Clock Divider Lower value, specifies the amount to divide the MIPI 8X clock to create the RX escape clock. Program the combined value of the upper and lower fields with the desired value -1.</td></tr></table>			Description	Rx Escape Clock Divider Upper: This field, concatenated with Rx Escape Clock Divider Lower value, specifies the amount to divide the MIPI 8X clock to create the RX escape clock. Program the combined value of the upper and lower fields with the desired value -1.													
Description																		
Rx Escape Clock Divider Upper: This field, concatenated with Rx Escape Clock Divider Lower value, specifies the amount to divide the MIPI 8X clock to create the RX escape clock. Program the combined value of the upper and lower fields with the desired value -1.																		
4:3	MIPI2 8by3X Divider																	
	<table><tr><th>Description</th></tr><tr><td>This field specifies the amount to divide the MIPI 8X clock to create the MIPI 8/3X clock.</td></tr></table>			Description	This field specifies the amount to divide the MIPI 8X clock to create the MIPI 8/3X clock.													
Description																		
This field specifies the amount to divide the MIPI 8X clock to create the MIPI 8/3X clock.																		
	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>00b</td><td>Reserved</td><td></td></tr><tr><td>01b</td><td>Divide by 2</td><td></td></tr><tr><td>10b</td><td>Divide by 3</td><td>Use divide by 3 for both DPI and DBI modes</td></tr><tr><td>11b</td><td>Divide by 4</td><td></td></tr></table>	Value	Name	Description	00b	Reserved		01b	Divide by 2		10b	Divide by 3	Use divide by 3 for both DPI and DBI modes	11b	Divide by 4			
Value	Name	Description																
00b	Reserved																	
01b	Divide by 2																	
10b	Divide by 3	Use divide by 3 for both DPI and DBI modes																
11b	Divide by 4																	
2	Spare 2																	



MIPI_CLOCK_CTL		
	1:0	MIPI2 DPHY Divider
		Description
		Rx Escape Clock Divider Lower: This field, concatenated with Rx Escape Clock Divider Upper value, specifies the amount to divide the MIPI 8X clock to create the RX escape clock. Program the combined value of the upper and lower fields with the desired value -1.



MIPI_CTRL

MIPI_CTRL		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B104h-6B107h	
Name:	MIPIA_CTRL	
ShortName:	MIPIA_CTRL	
Power:	PG1	
Reset:	soft	
Address:	6B904h-6B907h	
Name:	MIPIC_CTRL	
ShortName:	MIPIC_CTRL	
Power:	PG1	
Reset:	soft	
Restriction		
Restriction : Changing this register can only be done when the MIPI device_ready is turned OFF		
DWord	Bit	Description
0	31	Reserved
		Format: MBZ
	30	Reserved
		Format: MBZ
	29	Reserved
		Format: MBZ
	28	Reserved
		Format: MBZ
	27:26	Reserved
		Format: MBZ
	25	Reserved
		Format: MBZ
24:23	Reserved	
	Format: MBZ	



MIPI_CTRL			
22:20	Reserved		
	Format:	MBZ	
19:17	Reserved		
	Format:	MBZ	
16	Reserved		
	Format:	MBZ	
15:14	Reserved		
	Format:	MBZ	
9:7	Pipe Select		
	Access:	R/W	
	These bits determine which Pipe this MIPI port will connect to. It is not valid to enable and direct more than one pipe to one MIPI port.		
	Value	Name	
	000b	Pipe A	
	001b	Pipe B	
	010b	Pipe C	
	Others	Reserved	
6:4	RESERVED		
	Format:	MBZ	
3	DSC Enable		
	This bit enables Display Stream Compression. It is double buffered to the rising edge of vblank.		
	Value	Name	
	0b	DSC Disable [Default]	
2	1b	DSC Enable	
	RGB FLIP		
	Access:	R/W	
	Value	Name	Description
0b	Enable	DPI mode: RGB data from display pipe is flipped before MIPI IP and in MIPI IP. Result is RGB. DBI mode: RGB data from display pipe is flipped before MIPI IP. Result is BGR.	
1b	Disable	DPI mode: RGB data from display pipe is flipped in MIPI IP. Result is BGR. DBI mode: RGB data from display pipe is not flipped. Result is RGB.	
Programming Notes			
The behavior of this setting is different between DPI and DBI.			



MIPI_CTRL			
	1:0	RESERVED	
		Format:	MBZ



MIPI_DBI_BW_CTRL_REG

MIPI_DBI_BW_CTRL_REG		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Access: R/W		
Size (in bits): 32		
Address: 6B084h-6B087h		
Name: MIPIA_DBI_BW_CTRL_REG		
ShortName: MIPIA_DBI_BW_CTRL_REG		
Power: PG1		
Reset: soft		
Address: 6B884h-6B887h		
Name: MIPIC_DBI_BW_CTRL_REG		
ShortName: MIPIC_DBI_BW_CTRL_REG		
Power: PG1		
Reset: soft		
DWord	Bit	Description
0	31:0	BANDWIDTH_TIMER
		<table><tr><td>Access:</td><td>R/W</td></tr></table> DBI Bandwidth control Register. The bandwidth essential for transmitting 16 long packets containing 252 bytes meant for DCS write memory command is programmed in this register in terms of byte clocks. Based on the DSI transfer rate and the number of lanes configured the time taken to transmit 16 long packets in a DSI stream varies.Note: The value programmed in this timer must be greater than the actual time taken to carryout 16 long packets transmission in DSI stream plus the time taken to transmit two blanking packets
Access:	R/W	



MIPI_DBI_FIFO_THRTL_REG

MIPI_DBI_FIFO_THRTL_REG				
Register Space:		MMIO: 0/2/0		
Source:		BSpec		
Default Value:		0x00000000		
Access:		R/W		
Size (in bits):		32		
Address:		6B024h-6B027h		
Name:		MIPIA_DBI_FIFO_THRTL_REG		
ShortName:		MIPIA_DBI_FIFO_THRTL_REG		
Power:		PG1		
Reset:		soft		
Address:		6B824h-6B827h		
Name:		MIPIC_DBI_FIFO_THRTL_REG		
ShortName:		MIPIC_DBI_FIFO_THRTL_REG		
Power:		PG1		
Reset:		soft		
DWord	Bit	Description		
0	31:2	RESERVED		
		Format: MBZ		
	1:0	DBI_FIFO_THRTL		
		Access: R/W		
		DBI FIFO's watermark can be set using the following bits so as to enable dbi_stall de-assertion whenever the below FIFO condition is reached		
		Value	Name	Description
		00b	half	(1/2) DBI fifo empty
		01b	quarter	(1/4) DBI fifo empty
10b	empty	7 locations are empty		
11b	Reserved			



MIPI_DEVICE_READY_REG

MIPI_DEVICE_READY_REG		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B000h-6B003h	
Name:	MIPIA_DEVICE_READY_REG	
ShortName:	MIPIA_DEVICE_READY_REG	
Power:	PG1	
Reset:	soft	
Address:	6B800h-6B803h	
Name:	MIPIC_DEVICE_READY_REG	
ShortName:	MIPIC_DEVICE_READY_REG	
Power:	PG1	
Reset:	soft	
MIPI Device Ready Register		
DWord	Bit	Description
0	31:4	RESERVED
		Format: MBZ
	3	BUS_POSSESSION
		Access: R/W
	2:1	ULPS_STATE
		Access: R/W
	0	DEVICE_READY_
		Access: R/W
Set by the processor to inform that device is ready		



MIPI_DEVICE_RESET_TIMER

MIPI_DEVICE_RESET_TIMER		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B01Ch-6B01Fh	
Name:	MIPIA_DEVICE_RESET_TIMER	
ShortName:	MIPIA_DEVICE_RESET_TIMER	
Power:	PG1	
Reset:	soft	
Address:	6B81Ch-6B81Fh	
Name:	MIPIC_DEVICE_RESET_TIMER	
ShortName:	MIPIC_DEVICE_RESET_TIMER	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:0	DEVICE_RESET_TIMER
		Access: R/W Timeout value to be checked for device to be reset after issuing reset entry command. If the timer expires the DSI Host enters normal operation



MIPI_DLBUFFER_CTRL

MIPI_DLBUFFER_CTRL								
Register Space: MMIO: 0/2/0								
Source: BSpec								
Default Value: 0x00000000								
Access: R/W								
Size (in bits): 32								
Address: 6B144h-6B147h								
Name: MIPIA Dual Link Buffer Control								
ShortName: MIPIA_DLBUFFER_CTRL								
Power: PG1								
Reset: soft								
Address: 6B944h-6B947h								
Name: MIPIC Dual Link Buffer Control								
ShortName: MIPIC_DLBUFFER_CTRL								
Power: PG1								
Reset: soft								
DWord	Bit	Description						
0	31	ENABLE						
		Access: R/W						
		This field enables the dual link buffer for DBI mode.						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>Disable</td></tr><tr><td>1</td><td>Enable</td></tr></table>	Value	Name	0	Disable	1	Enable
		Value	Name					
		0	Disable					
	1	Enable						
	30	Frame vs Line Buffering						
		Access: R/W						
		This field selects the buffering boundary.						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>Begin buffering on a frame boundary</td></tr><tr><td>1</td><td>Begin buffering on a line boundary</td></tr></table>	Value	Name	0	Begin buffering on a frame boundary	1	Begin buffering on a line boundary
		Value	Name					
		0	Begin buffering on a frame boundary					
1	Begin buffering on a line boundary							
Restriction								
Restriction : Only use the frame boundary setting.								
29:11	RESERVED							
	Format: MBZ							



MIPI_DLBUFFER_CTRL		
	10:0	TARGET
		Access:
		R/W
		This field indicates the number of pixels to hold in the slave link buffer before enabling the timing generator, so the Master and Slave DSI controllers are in sync. Valid only when operating in front back dual link mode. Value should only be programmed for the Slave DSI controller. If bit 31 is set then the target for the Slave DSI controller must be non-zero. Maximum value is 1440 decimal.
		Programming Notes
		Program target to 1/2 the frame width.



MIPI_DPHY_PARAM_REG

MIPI_DPHY_PARAM_REG		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B080h-6B083h	
Name:	MIPIA_DPHY_PARAM_REG	
ShortName:	MIPIA_DPHY_PARAM_REG	
Power:	PG1	
Reset:	soft	
Address:	6B880h-6B883h	
Name:	MIPIC_DPHY_PARAM_REG	
ShortName:	MIPIC_DPHY_PARAM_REG	
Power:	PG1	
Reset:	soft	
Description		
This register needs to be programmed in terms of HSDDR clock count.		
DWord	Bit	Description
0	31:24	EXIT_ZERO_COUNT Access: R/W THS_0_TIM_UI_CNT and THS_EXIT_TIM_UI_CNT for dphy are programmed as exit zero count by the processor
	23:16	TRAIL_COUNT Access: R/W TCLK_POST_TIM_UI_CNT and TCLK_TRAIL_TIM_UI_CNT for dphy are programmed as trail count by the processor
	15:8	CLK_ZERO_COUNT Access: R/W TCLK_0_TIM_UI_CNT for dphy is programmed as clk zero count by the processor
	7:0	PREPARE_COUNT Access: R/W TCLK_PREP_TIM_UI_CNT and THS_PREP_TIM_UI_CNT for dphy are programmed as prepare count by the processor



MIPI_DPI_CTRL_REG

MIPI_DPI_CTRL_REG				
Register Space:		MMIO: 0/2/0		
Source:		BSpec		
Default Value:		0x00000000		
Access:		R/W		
Size (in bits):		32		
Address:		6B048h-6B04Bh		
Name:		MIPIA_DPI_CTRL_REG		
ShortName:		MIPIA_DPI_CTRL_REG		
Power:		PG1		
Reset:		soft		
Address:		6B848h-6B84Bh		
Name:		MIPIC_DPI_CTRL_REG		
ShortName:		MIPIC_DPI_CTRL_REG		
Power:		PG1		
Reset:		soft		
DWord	Bit	Description		
0	31:8	RESERVED		
		Format: MBZ		
	7	RSTTRG		
		Access: R/W		
	6	HS_LP		
		Access: R/W		
		Set to '0' to indicate the special packets are sent through the DSI link using HS transmission and set to '1' to indicate that the special packets are sent through the DSI link using low power mode		
		Value	Name	Description
		0	High Speed	special packets are sent through the DSI link using HS transmission
		1	Low Power	special packets are sent through the DSI link using low power mode
		5	BACK_LIGHT_OFF	
	Access: R/W			
Set to '1' to indicate a backlight OFF short packet has to be packetised for the DPI's virtual channel				



MIPI_DPI_CTRL_REG		
	4	BACK_LIGHT_ON Access: R/W Set to '1' to indicate a backlight ON short packet has to be packetised for the DPI's virtual channel
	3	COLOR_MODE_OFF Access: R/W Set to '1' to indicate a color mode OFF short packet has to be packetised for the DPI's virtual channel
	2	COLOR_MODE_ON Access: R/W Set to '1' to indicate a color mode ON short packet has to be packetised for the DPI's virtual channel
	1	TURN_ON Access: R/W Set to '1' to indicate a turn on short packet has to be packetised for the DPI's virtual channel
	0	SHUT_DOWN Access: R/W Set to '1' to indicate a shut down short packet has to be packetised for the DPI's virtual channel



MIPI_DPI_DATA_REGISTER

MIPI_DPI_DATA_REGISTER		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B04Ch-6B04Fh	
Name:	MIPIA_DPI_DATA_REGISTER	
ShortName:	MIPIA_DPI_DATA_REGISTER	
Power:	PG1	
Reset:	soft	
Address:	6B84Ch-6B84Fh	
Name:	MIPIC_DPI_DATA_REGISTER	
ShortName:	MIPIC_DPI_DATA_REGISTER	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:6	RESERVED
		Format: MBZ
	5:0	COMMAND_BYTE
		Access: R/W Command Byte to represent the new or not defined command bytes usage for special features representation. [Like backlight ON and OFF]. This register should be programmed before the DPI control register is being programmed for backlight ON/OFF



MIPI_DPI_RESOLUTION_REG

MIPI_DPI_RESOLUTION_REG		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B020h-6B023h	
Name:	MIPIA_DPI_RESOLUTION_REG	
ShortName:	MIPIA_DPI_RESOLUTION_REG	
Power:	PG1	
Reset:	soft	
Address:	6B820h-6B823h	
Name:	MIPIC_DPI_RESOLUTION_REG	
ShortName:	MIPIC_DPI_RESOLUTION_REG	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	VERTICAL_ADDRESS
		Access: R/W Shows the vertical address count in lines
	15:0	HORIZONTAL_ADDRESS
		Access: R/W Shows the horizontal address count in pixels If supported format in video mode is Compressed Image, Data Horizontal address counts in bytes



MIPI_DSI_FUNC_PRG_REG

MIPI_DSI_FUNC_PRG_REG		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000001	
Access:	R/W	
Size (in bits):	32	
Address:	6B00Ch-6B00Fh	
Name:	MIPIA_DSI_FUNC_PRG_REG	
ShortName:	MIPIA_DSI_FUNC_PRG_REG	
Power:	PG1	
Reset:	soft	
Address:	6B80Ch-6B80Fh	
Name:	MIPIC_DSI_FUNC_PRG_REG	
ShortName:	MIPIC_DSI_FUNC_PRG_REG	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:13	SUPPORTED_DATA_WIDTH_IN_COMMAND_MODE
		Access: R/W
	12:11	RESERVED_1
		Format: MBZ
	10:7	SUPPORTED_FORMAT_IN_VIDEO_MODE
		Access: R/W



MIPI_DSI_FUNC_PRG_REG				
		Value	Name	Programming Notes
		0000b	Video Mode not supported	
		0001b	RGB565	
		0010b	RGB666	Restriction : The RGB666 format has restrictions on the horizontal resolution. For isolated MIPI, the horizontal resolution must be evenly divisible by 4. For dual link MIPI, 1/2 the horizontal resolution plus the overlapping pixels must be evenly divisible by 4.
		0011b	RGB 666 loosely packed format	
		0100b	RGB888	
6:5	CHANNEL_NUMBER_FOR_COMMAND_MODE			
	Access:		R/W	
Virtual channel number for command mode is programmed by the processor				
4:3	CHANNEL_NUMBER_FOR_VIDEO_MODE			
	Access:		R/W	
Virtual channel number for video mode is programmed by the processor				
2:0	DATA_LANES_PRG_R_REG			
	Default Value:			001b
	Access:			R/W
Number of data lanes to be supported is programmed by the processor				



MIPI_EN_DLY_CNTR

MIPI_EN_DLY_CNTR						
Register Space: MMIO: 0/2/0						
Source: BSpec						
Default Value: 0x00000000						
Access: R/W						
Size (in bits): 32						
Address: 6B0F4h-6B0F7h						
Name: MIPIA_EN_DLY_CNTR						
ShortName: MIPIA_EN_DLY_CNTR						
Power: PG1						
Reset: soft						
Address: 6B8F4h-6B8F7h						
Name: MIPIC_EN_DLY_CNTR						
ShortName: MIPIC_EN_DLY_CNTR						
Power: PG1						
Reset: soft						
DWord	Bit	Description				
0	31:0	TG_ENABLE_DELAY_COUNTER				
		<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">This is the delay value which is counted down to delay the assertion of the ip_fg_enable on the DPI interface after the setting of the 'EN' signal in MIPI_PORT_CTRL register by s/w</td></tr></table>	Access:	R/W	This is the delay value which is counted down to delay the assertion of the ip_fg_enable on the DPI interface after the setting of the 'EN' signal in MIPI_PORT_CTRL register by s/w	
Access:	R/W					
This is the delay value which is counted down to delay the assertion of the ip_fg_enable on the DPI interface after the setting of the 'EN' signal in MIPI_PORT_CTRL register by s/w						



MIPI_EOT_DISABLE_REGISTER

MIPI_EOT_DISABLE_REGISTER				
Register Space:		MMIO: 0/2/0		
Source:		BSpec		
Default Value:		0x00000000		
Access:		R/W		
Size (in bits):		32		
Address:		6B05Ch-6B05Fh		
Name:		MIPIA_EOT_DISABLE_REGISTER		
ShortName:		MIPIA_EOT_DISABLE_REGISTER		
Power:		PG1		
Reset:		soft		
Address:		6B85Ch-6B85Fh		
Name:		MIPIC_EOT_DISABLE_REGISTER		
ShortName:		MIPIC_EOT_DISABLE_REGISTER		
Power:		PG1		
Reset:		soft		
DWord	Bit	Description		
0	31:10	RESERVED		
		Format:		MBZ
	9	DEFEATURE_DPI_FIFO_CTR		
		Access:		R/W
		Set by the processor to enable or disable the belowfeatures.		
		Value	Name	Description
		0	Disable	Feature Disabled
		1	Enable	The "mipi_dpf_vblank_start" signal is asserted only when the complete frame is transferred in the DPHY line and also the DPI FIFO is flushed out at the end of each frame.
	8	DPHY_DEFEATURE_EN		
		Access:		R/W
		Set by the processor to enable or disable DPHY RTL fix for misaligned data lanes.		
		Value	Name	Description
		0	Disable	disables the DPHY fix.
		1	Enable	enables the DPHY fix.
	7	LP_RX_TIMEOUT_ERROR_RECOVERY_DISABLE		

**MIPI_EOT_DISABLE_REGISTER**

MIPI_EOT_DISABLE_REGISTER					
		Access:		R/W	
		Set by the processor to enable or disable the LP_Rx_timeout error recovery if the processor clears LP_Rx_timeout error interrupt.			
		Value	Name	Description	
		0	Enable	LP_Rx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the LP_Rx_timeout error interrupt.	
		1	Disable	If the processor clears the LP_Rx_timeout error interrupt, LP_Rx_timeout error recovery action will not happen in DSI Tx contorller. LP Rx timeout error interrupt will act as an informative interrupt	
6	HS_TX_TIMEOUT_ERROR_RECOVERY_DISABLE				
	Access:		R/W		
	Set by the processor to enable or disable the HS_Tx_timeout error recovery if the processor clears HS_Tx_timeout interrupt.				
	Value	Name	Description		
	0	Enable	HS_Tx_timeout error recovery action will be taken by the DSI Tx controller if the processor clears the HS_Tx_timeout error interrupt.		
		1	Disable	If the processor clears the HS_Tx_timeout error interrupt, HS_Tx_timeout error recovery action will not happen in DSI Tx contorller. HS Tx timeout error interrupt will act as an informative interrupt	
		LOW_CONTENTION_RECOVERY_DISABLE			
		Access:		R/W	
		Set by the processor to enable or disable the contention recovery procedure if the processor clears Low contention interrupt.			
		Value	Name	Description	
		0	Enable	Contention recovery will happen if the processor clears Low contention interrupt.	
		1	Disable	If the processor clears the low contention interrupt, contention recovery procedure will not be initiated by the DSI Tx contorller. Low contention interrupt will act as an informative interrupt	
		HIGH_CONTENTION_RECOVERY_DISABLE			
		Access:		R/W	
		Set by the processor to enable or disable the contention recovery procedure if the processor clears High contention interrupt.			
4		Value	Name	Description	
		0	Enable	Contention recovery will happen if the processor clears High contention interrupt.	
		1	Disable	If the processor clears the high contention interrupt, contention recovery procedure will not be initiated by the DSI Tx contorller. Ignore the High Contention Interrupt in MIPI_INTR_STAT_REG	



MIPI_EOT_DISABLE_REGISTER

	3	TXDSI_TYPE_NOT_RECOGNISED_ERROR_RECOVERY_DISABLE	
		Access:	R/W
		Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if TxDSI data type not recognised error interrupt is cleared by the processor.	
		Value	Name
	2	TXECC_MULTIBIT_ERR_RECOVERY_DISABLE	
		Access:	R/W
		Set by the processor to enable or disable the error recovery action to be taken by the DSI Tx controller if Tx ECC multibit error interrupt is cleared by the processor.	
		Value	Name
	1	CLOCKSTOP	
		Access:	R/W
		Set by the processor to enable or disable clock stopping feature during BLLP timing in a DPI transfer in dual channel mode or during DPI only mode and also when there is no traffic in the DBI interface in DBI only enabled mode. By default this register value is 0.	
		Value	Name
	0	EOT_DIS	
		Access:	R/W
		Set by the processor to enable or disable EOT short packet transmission. By default this register value is 0. For backward compatibility of earlier DSI systems, EOT short packet transmission can be disabled.	
		Value	Name



MIPI_GEN_FIFO_STAT_REGISTER

MIPI_GEN_FIFO_STAT_REGISTER			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x1E060606		
Access:	RO		
Size (in bits):	32		
Address:	6B074h-6B077h		
Name:	MIPIA_GEN_FIFO_STAT_REGISTER		
ShortName:	MIPIA_GEN_FIFO_STAT_REGISTER		
Power:	PG1		
Reset:	soft		
Address:	6B874h-6B877h		
Name:	MIPIC_GEN_FIFO_STAT_REGISTER		
ShortName:	MIPIC_GEN_FIFO_STAT_REGISTER		
Power:	PG1		
Reset:	soft		
DWord	Bit	Description	
0	31:29	RESERVED	
		Format: MBZ	
	28	DPI_FIFO_EMPTY	
		Access: RO	
		Value	Name
		0	Disable
		1	Enable [Default]
	27	DBI_FIFO_EMPTY	
		Access: RO	
		Value	Name
		0	Disable
		1	Enable [Default]
	26	LP_CTRL_FIFO_EMPTY	
		Access: RO	



MIPI_GEN_FIFO_STAT_REGISTER

		Value	Name
		0	Disable
		1	Enable [Default]
	25	LP_CTRL_FIFO_HALF_EMPTY	
		Access:	RO
		Value	Name
		0	Disable
	24	LP_CTRL_FIFO_FULL	
		Access:	RO
		Value	Name
		0	Disable [Default]
	23:19	RESERVED_1	
		Format:	MBZ
	18	HS_CTRL_FIFO_EMPTY	
		Access:	RO
		Value	Name
		0	Disable
	17	HS_CTRL_FIFO_HALF_EMPTY	
		Access:	RO
		Value	Name
		0	Disable
	16	HS_CTRL_FIFO_FULL	
		Access:	RO
		Value	Name
		0	Disable [Default]
	15:11	RESERVED_2	

**MIPI_GEN_FIFO_STAT_REGISTER**

		Format:	MBZ
	10	LP_DATA_FIFO_EMPTY	
		Access:	RO
		Value	Name
		0	Disable
		1	Enable [Default]
	9	LP_DATA_FIFO_HALF_EMPTY	
		Access:	RO
		Value	Name
		0	Disable
		1	Enable [Default]
	8	LP_DATA_FIFO_FULL	
		Access:	RO
		Value	Name
		0	Disable [Default]
		1	Enable
	7:3	RESERVED_3	
		Format:	MBZ
	2	HS_DATA_FIFO_EMPTY	
		Access:	RO
		Value	Name
		0	Disable
		1	Enable [Default]
	1	HS_DATA_FIFO_HALF_EMPTY	
		Access:	RO
		Value	Name
		0	Disable
		1	Enable [Default]
	0	HS_DATA_FIFO_FULL	
		Access:	RO
		Value	Name



MIPI_GEN_FIFO_STAT_REGISTER			
		0	Disable [Default]
		1	Enable



MIPI_HIGH_LOW_SWITCH_COUNT

MIPI_HIGH_LOW_SWITCH_COUNT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B044h-6B047h	
Name:	MIPIA_HIGH_LOW_SWITCH_COUNT	
ShortName:	MIPIA_HIGH_LOW_SWITCH_COUNT	
Power:	PG1	
Reset:	soft	
Address:	6B844h-6B847h	
Name:	MIPIC_HIGH_LOW_SWITCH_COUNT	
ShortName:	MIPIC_HIGH_LOW_SWITCH_COUNT	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:0	HIGH_SPEED_TO_LOW_POWER_OR_LOW_POWER_TO_HIGH_SPEED_SWITCH_COUNT
		Access: R/W
		High speed to low power or Low power to high speed switching time in terms of txbyteclkhs



MIPI_HORIZ_ACTIVE_AREA_COUNT

MIPI_HORIZ_ACTIVE_AREA_COUNT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B034h-6B037h	
Name:	MIPIA_HORIZ_ACTIVE_AREA_COUNT	
ShortName:	MIPIA_HORIZ_ACTIVE_AREA_COUNT	
Power:	PG1	
Reset:	soft	
Address:	6B834h-6B837h	
Name:	MIPIC_HORIZ_ACTIVE_AREA_COUNT	
ShortName:	MIPIC_HORIZ_ACTIVE_AREA_COUNT	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:0	HORIZONTAL_ACTIVE_AREA_COUNT
		Access: R/W Shows the horizontal active area value in terms of txbyteclkhs



MIPI_HORIZ_BACK_PORCH_COUNT

MIPI_HORIZ_BACK_PORCH_COUNT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B02Ch-6B02Fh	
Name:	MIPIA_HORIZ_BACK_PORCH_COUNT	
ShortName:	MIPIA_HORIZ_BACK_PORCH_COUNT	
Power:	PG1	
Reset:	soft	
Address:	6B82Ch-6B82Fh	
Name:	MIPIC_HORIZ_BACK_PORCH_COUNT	
ShortName:	MIPIC_HORIZ_BACK_PORCH_COUNT	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:0	HORIZONTAL_BACK_PORCH_COUNT
		Access: R/W Shows the horizontal back porch value in terms of txbyteclkhs



MIPI_HORIZ_FRONT_PORCH_COUNT

MIPI_HORIZ_FRONT_PORCH_COUNT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B030h-6B033h	
Name:	MIPIA_HORIZ_FRONT_PORCH_COUNT	
ShortName:	MIPIA_HORIZ_FRONT_PORCH_COUNT	
Power:	PG1	
Reset:	soft	
Address:	6B830h-6B833h	
Name:	MIPIC_HORIZ_FRONT_PORCH_COUNT	
ShortName:	MIPIC_HORIZ_FRONT_PORCH_COUNT	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:0	HORIZONTAL_FRONT_PORCH_COUNT
		Access: R/W Shows the horizontal front porch value in terms of txbyteclkhs



MIPI_HORIZ_SYNC_PADDING_COUNT

MIPI_HORIZ_SYNC_PADDING_COUNT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B028h-6B02Bh	
Name:	MIPIA_HORIZ_SYNC_PADDING_COUNT	
ShortName:	MIPIA_HORIZ_SYNC_PADDING_COUNT	
Power:	PG1	
Reset:	soft	
Address:	6B828h-6B82Bh	
Name:	MIPIC_HORIZ_SYNC_PADDING_COUNT	
ShortName:	MIPIC_HORIZ_SYNC_PADDING_COUNT	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:0	HORIZONTAL_SYNC_PADDING_COUNT
		Access: R/W
		Shows the horizontal sync padding value in terms of txbyteclkhs



MIPI_HS_GEN_CTRL_REGISTER

MIPI_HS_GEN_CTRL_REGISTER		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B070h-6B073h	
Name:	MIPIA_HS_GEN_CTRL_REGISTER	
ShortName:	MIPIA_HS_GEN_CTRL_REGISTER	
Power:	PG1	
Reset:	soft	
Address:	6B870h-6B873h	
Name:	MIPIC_HS_GEN_CTRL_REGISTER	
ShortName:	MIPIC_HS_GEN_CTRL_REGISTER	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:24	RESERVED
		Format: MBZ
	23:8	WORD_COUNT
		Access: WO Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets.Note: Invalid parameters must be set to 00h
	7:6	VIRTUAL_CHANNEL
		Access: WO Used to specify the virtual channel for which the generic data transmission is intended
	5:0	DATA_TYPE
		Access: WO
		Used to specify the generic data types
		Value
03h		Generic short write no parameters
13h	Generic short write 1 parameter	

**MIPI_HS_GEN_CTRL_REGISTER**

	23h	Generic short write 2 parameters
	04h	Generic read no parameters
	14h	Generic read 1 parameter
	24h	Generic read 2 parameter
	29h	Generic long write
	05h	Manufacturer DCS short write no parameter
	15h	Manufacturer DCS short write 1 parameter
	06h	Manufacturer DCS read no parameter
	39h	Manufacturer DCS long write
	07h	Compression mode data type write , short write, 2 parameters
	0Ah	PPS long write



MIPI_HS_GEN_DATA_REGISTER

MIPI_HS_GEN_DATA_REGISTER		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B068h-6B06Bh	
Name:	MIPIA_HS_GEN_DATA_REGISTER	
ShortName:	MIPIA_HS_GEN_DATA_REGISTER	
Power:	PG1	
Reset:	soft	
Address:	6B868h-6B86Bh	
Name:	MIPIC_HS_GEN_DATA_REGISTER	
ShortName:	MIPIC_HS_GEN_DATA_REGISTER	
Power:	PG1	
Reset:	soft	
This register supports single byte, word, and Dword writes. It does not support 3 byte writes.		
DWord	Bit	Description
0	31:0	HS_GEN_DATA
		Access: R/W
		Data port register used for generic data transfers in high speed mode



MIPI_HS_LS_DBI_ENABLE_REG

MIPI_HS_LS_DBI_ENABLE_REG				
Register Space:	MMIO: 0/2/0			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
Address:	6B078h-6B07Bh			
Name:	MIPIA_HS_LS_DBI_ENABLE_REG			
ShortName:	MIPIA_HS_LS_DBI_ENABLE_REG			
Power:	PG1			
Reset:	soft			
Address:	6B878h-6B87Bh			
Name:	MIPIC_HS_LS_DBI_ENABLE_REG			
ShortName:	MIPIC_HS_LS_DBI_ENABLE_REG			
Power:	PG1			
Reset:	soft			
Note : dbi_hs_lp_switch_reg has to be written only if DBI FIFO is empty				
DWord	Bit	Description		
0	31:1	RESERVED		
		Format:	MBZ	
	0	DBI_HS_LS_SWITCH_RE		
		Access:	R/W	
		Value	Name	Description
		1	enable	DBI packets have to be transmitted in Low power mode
0	disable	DBI packets have to be transmitted in High speed mode		



MIPI_HS_READ_TRANSFER_COUNT

MIPI_HS_READ_TRANSFER_COUNT				
Register Space:		MMIO: 0/2/0		
Source:		BSpec		
Default Value:		0x00000000		
Size (in bits):		32		
Address:		6B07Ch-6B07Fh		
Name:		MIPIA_HS_READ_TRANSFER_COUNT		
ShortName:		MIPIA_HS_READ_TRANSFER_COUNT		
Power:		PG1		
Reset:		soft		
Address:		6B87Ch-6B87Fh		
Name:		MIPIC_HS_READ_TRANSFER_COUNT		
ShortName:		MIPIC_HS_READ_TRANSFER_COUNT		
Power:		PG1		
Reset:		soft		
Programming Notes				
AHB should program this register before start the high speed DCS/MCS/Generic read transfer.				
DWord	Bit	Description		
0	31:17	Spare 31 to 17		
		Access:	R/W	
		Reserved R/W for future use.		
	16	HS Read Defeature En		
		Access:	R/W	
		This field controls whether the HS read allow checking is enabled.		
		Value	Name	Description
		0	Disable	Disable the new HS read allow checking so the DSI Tx allows the HS read transfer based on the internally calculated value.
		1	Enable	Enable the new HS read allow checking so the DSI Tx allows the HS read transfer based on the programmed HS read count value.
	15:0	HS Read Count		
Access:		R/W		
This field gives the HS read transfer time in terms of txbyteclkhs clock. It is a time in-between the read command is transferred on the DSI PPI to stop state detection on the DSI Tx after the second BTA.				



MIPI_HS_TX_TIMEOUT_REG

MIPI_HS_TX_TIMEOUT_REG		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B010h-6B013h	
Name:	MIPIA_HS_TX_TIMEOUT_REG	
ShortName:	MIPIA_HS_TX_TIMEOUT_REG	
Power:	PG1	
Reset:	soft	
Address:	6B810h-6B813h	
Name:	MIPIC_HS_TX_TIMEOUT_REG	
ShortName:	MIPIC_HS_TX_TIMEOUT_REG	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:24	RESERVED
		Format: MBZ
	23:0	HIGH_SPEED_TX_TIMEOUT_COUNTER
		Access: R/W The maximum duration allowed for the DSI host to remain in high speed mode for a transmission. If the counter expires, HS mode is terminated with EOT and the lanes enter stop state



MIPI_INIT_COUNT_REGISTER

MIPI_INIT_COUNT_REGISTER		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B050h-6B053h	
Name:	MIPIA_INIT_COUNT_REGISTER	
ShortName:	MIPIA_INIT_COUNT_REGISTER	
Power:	PG1	
Reset:	soft	
Address:	6B850h-6B853h	
Name:	MIPIC_INIT_COUNT_REGISTER	
ShortName:	MIPIC_INIT_COUNT_REGISTER	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:0	MASTER_INIT_TIMER
		Access: R/W Counter value in terms of low power clock to initialise the DSI Host IP [TINT] that drives a stop state on the mipi's D-PHY bus



MIPI_INTR_EN_REG_1

MIPI_INTR_EN_REG_1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B094h-6B097h	
Name:	MIPIA_INTR_EN_REG_1	
ShortName:	MIPIA_INTR_EN_REG_1	
Power:	PG1	
Reset:	soft	
Address:	6B894h-6B897h	
Name:	MIPIC_INTR_EN_REG_1	
ShortName:	MIPIC_INTR_EN_REG_1	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:2	RESERVED
		Format: MBZ
	1	DPI Line Timeout
		Access: R/W Set to enable the interrupt for DPI line timeout.
	0	MIPI_ENABLE_RX_CONNECTION_DETECTED
		Access: R/W Set to enable the interrupt for contention detected error in the acknowledgement packet reports



MIPI_INTR_EN_REG

MIPI_INTR_EN_REG		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B008h-6B00Bh	
Name:	MIPIA_INTR_EN_REG	
ShortName:	MIPIA_INTR_EN_REG	
Power:	PG1	
Reset:	soft	
Address:	6B808h-6B80Bh	
Name:	MIPIC_INTR_EN_REG	
ShortName:	MIPIC_INTR_EN_REG	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31	TEARING_EFFECT Access: R/W Set to enable the tearing effect interrupt
	30	SPL_PKT_SENT_INTERRUPT Access: R/W Set to enable the confirmation of transmission of the DPI event specific commands set in the dpi control and dpi data register
	29	GEN_READ_DATA_AVAIL Access: R/W Set to enable Generic Read available interrupt
	28	LP_GENERIC_WR_FIFO_FULL Access: R/W Set to enable the LP generic write fifo full interrupt
	27	HS_GENERIC_WR_FIFO_FULL



MIPI_INTR_EN_REG						
		<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Set to enable the HS generic write fifo full interrupt</td></tr></table>	Access:	R/W	Set to enable the HS generic write fifo full interrupt	
Access:	R/W					
Set to enable the HS generic write fifo full interrupt						
26	RX_PROT_VIOLATION	<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Set to enable protocol violation error</td></tr></table>	Access:	R/W	Set to enable protocol violation error	
Access:	R/W					
Set to enable protocol violation error						
25	RX_INVALID_TX_LENGTH	<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Set to enable invalid transmission length error</td></tr></table>	Access:	R/W	Set to enable invalid transmission length error	
Access:	R/W					
Set to enable invalid transmission length error						
24	ACK_WITH_NO_ERROR	<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Set to enable acknowledge trigger message reception with out any error</td></tr></table>	Access:	R/W	Set to enable acknowledge trigger message reception with out any error	
Access:	R/W					
Set to enable acknowledge trigger message reception with out any error						
23	TURN_AROUND_ACK_TIMEOUT	<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Set to enable turn around acknowledgement sequence timeout</td></tr></table>	Access:	R/W	Set to enable turn around acknowledgement sequence timeout	
Access:	R/W					
Set to enable turn around acknowledgement sequence timeout						
22	LP_RX_TIMEOUT	<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Set to enable low power reception count timeouts</td></tr></table>	Access:	R/W	Set to enable low power reception count timeouts	
Access:	R/W					
Set to enable low power reception count timeouts						
21	HS_TX_TIMEOUT	<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Set to enable a high speed transmission timeout</td></tr></table>	Access:	R/W	Set to enable a high speed transmission timeout	
Access:	R/W					
Set to enable a high speed transmission timeout						
20	DPI_FIFO_UNDERRUN	<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Set to enable if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver</td></tr></table>	Access:	R/W	Set to enable if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver	
Access:	R/W					
Set to enable if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver						
19	LOW_CONTENTION	<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Set to enable a LP low fault interrupt</td></tr></table>	Access:	R/W	Set to enable a LP low fault interrupt	
Access:	R/W					
Set to enable a LP low fault interrupt						
18	HIGH_CONTENTION	<table><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Set to enable a LP high fault interrupt</td></tr></table>	Access:	R/W	Set to enable a LP high fault interrupt	
Access:	R/W					
Set to enable a LP high fault interrupt						



MIPI_INTR_EN_REG

	17	TXDSI_VC_ID_INVALID	Access:	R/W
		Set to enable the interrupt if the received packets virtual channel ID is invalid		
	16	TXDSI_DATA_TYPE_NOT_RECOGNISED	Access:	R/W
		Set to enable the interrupt if the received packets data type is not recognised		
	15	TXCHECKSUM_ERROR	Access:	R/W
		Set to enable the interrupt if the computed CRC differs from the received CRC value for the received packets		
	14	TXECC_MULTIBIT_ERROR	Access:	R/W
		Set to enable the interrupt if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan DSI host		
	13	TXECC_SINGLE_BIT_ERROR	Access:	R/W
		Set to enable the interrupt if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan DSIhost		
	12	TXFALSE_CONTROL_ERROR	Access:	R/W
		Set to enable the interrupt for the control error,observed on the lanes by the Arasan_DSI_host		
	11	RXDSI_VC_ID_INVALID	Access:	R/W
		Set to enable the interrupt for invalid virtual channel ID in the acknowledgment packet reports		
	10	RXDSI_DATA_TYPE_NOT_RECOGNISED	Access:	R/W
		Set to enable the interrupt for the un recognised data type in the acknowledgment packet reports		
	9	RXCHECKSUM_ERROR	Access:	R/W
		Set to enable the interrupt for the computed CRC differs from the received CRC value in the acknowledgment packet reports		

**MIPI_INTR_EN_REG**

	8	RXECC_MULTIBIT_ERROR	Access:	R/W
		Set to enable the interrupt for no ECC correction for the packet or there are more than 2 bit errors reported in the acknowledgment packet		
	7	RXECC_SINGLE_BIT_ERROR	Access:	R/W
		Set to enable the interrupt for ECC syndrome computation and one bit error correction for the acknowledgment packet		
	6	RXFALSE_CONTROL_ERROR	Access:	R/W
		Set to enable the interrupt for control error in the acknowledgment packet reports		
	5	RXHS_RECEIVE_TIMEOUT_ERROR	Access:	R/W
		Set to enable the interrupt for the high speed receive timeout Error in the acknowledgment packet reports		
	4	RX_LP_TX_SYNC_ERROR	Access:	R/W
		Set to enable the interrupt for Low power transmission sync error in the acknowledgment packet reports		
	3	RXESCAPE_MODE_ENTRY_ERROR	Access:	R/W
		Set to enable the interrupt for Escape Mode Entry command error in the acknowledgment packet reports		
	2	RXEOTSYNC_ERROR	Access:	R/W
		Set to enable the interrupt for End of transmission synchronisation Error in the acknowledgement packet reports		
	1	RXSOTSYNC_ERROR	Access:	R/W
		Set to enable the interrupt for start of transmission synchronisation error in the acknowledgement packet reports		



MIPI_INTR_EN_REG		
	0	RXSOT_ERROR
		Access: R/W
		Set to enable the interrupt for start of transmission error in the acknowledgment packet reports



MIPI_INTR_STAT_REG_1

MIPI_INTR_STAT_REG_1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/WC	
Size (in bits):	32	
Address:	6B090h-6B093h	
Name:	MIPIA_INTR_STAT_REG_1	
ShortName:	MIPIA_INTR_STAT_REG_1	
Power:	PG1	
Reset:	soft	
Address:	6B890h-6B893h	
Name:	MIPIC_INTR_STAT_REG_1	
ShortName:	MIPIC_INTR_STAT_REG_1	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:2	RESERVED
		Format: MBZ
	1	DPI Line Timeout
		Access: R/WC Set to 1'b1 by hardware when there is a DPI Line Timeout.
	0	MIPI_RX_CONNECTION_DETECTED
		Access: R/WC Set to 1'b1 by hardware if the contention detected in the display device and is reported in the Acknowledge packet by the display device.



MIPI_INTR_STAT_REG

MIPI_INTR_STAT_REG		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/WC	
Size (in bits):	32	
Address:	6B004h-6B007h	
Name:	MIPIA_INTR_STAT_REG	
ShortName:	MIPIA_INTR_STAT_REG	
Power:	PG1	
Reset:	soft	
Address:	6B804h-6B807h	
Name:	MIPIC_INTR_STAT_REG	
ShortName:	MIPIC_INTR_STAT_REG	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31	TEARING_EFFECT Access: R/WC Set to indicate that tearing effect trigger message is received
	30	SPL_PKT_SENT_INTERRUPT Access: R/WC Set to confirm the transmission of the DPI event specific commands set in the dpi control and dpi data register
	29	GEN_READ_DATA_AVAIL Access: R/WC Set to indicate that the requested data for a Generic Read request is available in the buffer i.e., generic read response data is available in the read FIFO
	28	LP_GENERIC_WR_FIFO_FULL Access: R/WC Set to indicate that the LP generic write fifo is full

**MIPI_INTR_STAT_REG**

	27	HS_GENERIC_WR_FIFO_FULL	Access:	R/WC
		Set to indicate that the HS generic write fifo is full		
	26	RX_PROT_VIOLATION	Access:	R/WC
		Set if DSI protocol violation error is reported in the acknowledge packet by the display device		
	25	RX_INVALID_TX_LENGTH	Access:	R/WC
		Set if invalid transmission length error is reported in the acknowledge packet by the display device		
	24	ACK_WITH_NO_ERROR	Access:	R/WC
		Set if acknowledge trigger message is received with out any error		
	23	TURN_AROUND_ACK_TIMEOUT	Access:	R/WC
		Set if a turn around acknowledgement sequence is not received from the display device		
	22	LP_RX_TIMEOUT	Access:	R/WC
		Set if a low power reception count expires this interrupt is generated		
	21	HS_TX_TIMEOUT	Access:	R/WC
		Set if a high speed transmission prevails for more than the expected count value this interrupt is raised		
	20	DPI_FIFO_UNDERRUN	Access:	R/WC
		Set to '1' if there is no data in the dpi fifo to make a in time delivery of the pixel data to the DSI receiver		
	19	LOW_CONTENTION	Access:	R/WC
		Set to '1' if a LP low fault is registered by at the D-PHY contention detector		



MIPI_INTR_STAT_REG

	18	HIGH_CONTENTION	Access:	R/WC
		Set to '1' if a LP high fault is registered by at the D-PHY contention detector		
	17	TXDSI_VC_ID_INVALID	Access:	R/WC
		Set to '1' if the received virtual channel ID is invalid		
	16	TXDSI_DATA_TYPE_NOT_RECOGNISED	Access:	R/WC
		Set to '1' if the received data type is not recognised		
	15	TXCHECKSUM_ERROR	Access:	R/WC
		Set to '1' if the computed checksum differs from the received checksum value during the reception of packets by Arasan_DSI host.		
	14	TXECC_MULTIBIT_ERROR	Access:	R/WC
		Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet received by Arasan_DSI_host		
	13	TXECC_SINGLE_BIT_ERROR	Access:	R/WC
		Set to '1' if ECC syndrome was computed and is corrected for one bit error during the reception of packets by the Arasan_DSI_host		
	12	TXFALSE_CONTROL_ERROR	Access:	R/WC
		Set to '1' if a control error is observed on the lanes by the Arasan_DSI_host		
	11	RXDSI_VC_ID_INVALID	Access:	R/WC
		Set to '1' if the virtual channel ID is invalid by the display device is reported in the Acknowledge packet by the display device		
	10	RXDSI_DATA_TYPE_NOT_RECOGNISED	Access:	R/WC
		Set to '1' if the data type is not recognised by the display device is reported in the Acknowledge packet by the display device		

**MIPI_INTR_STAT_REG**

	9	RXCHECKSUM_ERROR	Access:	R/WC
		Set to '1' if the computed CRC differs from the received CRC value and is reported in the Acknowledge packet by the display device		
	8	RXECC_MULTIBIT_ERROR	Access:	R/WC
		Set to '1' if there is no ECC correction for the packet or there are more than 2 bit errors in the packet is reported in the Acknowledge packet by the display device		
	7	RXECC_SINGLE_BIT_ERROR	Access:	R/WC
		Set to '1' if ECC syndrome was computed and corrected for one bit error is reported in the Acknowledge packet by the display device		
	6	RXFALSE_CONTROL_ERROR	Access:	R/WC
		Set to '1' if a control error is reported in the Acknowledge packet by the display device		
	5	RXHS_RECEIVE_TIMEOUT_ERROR	Access:	R/WC
		Set to '1' if the high speed receive timer value expires and data transfer lasts on the data lane is reported in the Acknowledge packet by the display device		
	4	RX_LP_TX_SYNC_ERROR	Access:	R/WC
		Set to '1' if Low power transmission sync error occurs in the display device and is reported in the Acknowledge packet by the display device		
	3	RXESCAPE_MODE_ENTRY_ERROR	Access:	R/WC
		Set to '1' if Escape Mode Entry command is not understandable by the display device and is reported in the Acknowledge packet by the display device		
	2	RXEOTSYNCERROR	Access:	R/WC
		Set to '1' if an end of transmission synchronisation error is reported in the Acknowledge packet by the display device		



MIPI_INTR_STAT_REG		
	1	RXSOTSYNCERROR Access:R/WC Set to '1' if a start of transmission synchronisation error is reported in the Acknowledge packet by the display device
	0	RXSOTERROR Access:R/WC Set to '1' if a start of transmission error is reported in the Acknowledge packet by the display device



MIPI_LP_BYTECLK_REGISTER

MIPI_LP_BYTECLK_REGISTER		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B060h-6B063h	
Name:	MIPIA_LP_BYTECLK_REGISTER	
ShortName:	MIPIA_LP_BYTECLK_REGISTER	
Power:	PG1	
Reset:	soft	
Address:	6B860h-6B863h	
Name:	MIPIC_LP_BYTECLK_REGISTER	
ShortName:	MIPIC_LP_BYTECLK_REGISTER	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:0	LP_BYTECLK
		Access: R/W
		Low power clock equivalence in terms of byte clock. The value programmed in this register is equal to the number of byte clocks occupied in one low power clock. This value is based on the byte clock (txbyteclkhs) and low power clock frequency (txclkesc)



MIPI_LP_GEN_CTRL_REGISTER

MIPI_LP_GEN_CTRL_REGISTER		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B06Ch-6B06Fh	
Name:	MIPIA_LP_GEN_CTRL_REGISTER	
ShortName:	MIPIA_LP_GEN_CTRL_REGISTER	
Power:	PG1	
Reset:	soft	
Address:	6B86Ch-6B86Fh	
Name:	MIPIC_LP_GEN_CTRL_REGISTER	
ShortName:	MIPIC_LP_GEN_CTRL_REGISTER	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:24	RESERVED
		Format: MBZ
	23:8	WORD_COUNT
		Access: WO Specifies the word count for generic long packet Specifies the accompanied parameters for generic short packets.Note: Invalid parameters must be set to 00h
	7:6	VIRTUAL_CHANNEL
		Access: WO Used to specify the virtual channel for which the generic data transmission is intended
	5:0	DATA_TYPE
		Access: WO
		Used to specify the generic data types
		Value
03h		Generic short write no parameters
13h	Generic short write 1 parameter	

**MIPI_LP_GEN_CTRL_REGISTER**

	23h	Generic short write 2 parameters
	04h	Generic read no parameters
	14h	Generic read 1 parameter
	24h	Generic read 2 parameter
	29h	Generic long write
	05h	Manufacturer DCS short write no parameter
	15h	Manufacturer DCS short write 1 parameter
	06h	Manufacturer DCS read no parameter
	39h	Manufacturer DCS long write
	07h	Compression mode data type write , short write, 2 parameters
	0Ah	PPS long write



MIPI_LP_GEN_DATA_REGISTER

MIPI_LP_GEN_DATA_REGISTER		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B064h-6B067h	
Name:	MIPIA_LP_GEN_DATA_REGISTER	
ShortName:	MIPIA_LP_GEN_DATA_REGISTER	
Power:	PG1	
Reset:	soft	
Address:	6B864h-6B867h	
Name:	MIPIC_LP_GEN_DATA_REGISTER	
ShortName:	MIPIC_LP_GEN_DATA_REGISTER	
Power:	PG1	
Reset:	soft	
This register supports single byte, word, and Dword writes. It does not support 3 byte writes.		
DWord	Bit	Description
0	31:0	LP_GEN_DATA
		Access: R/W
		Data port register used for generic data transfers in low power mode



MIPI_LP_RX_TIMEOUT_REG

MIPI_LP_RX_TIMEOUT_REG		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B014h-6B017h	
Name:	MIPIA_LP_RX_TIMEOUT_REG	
ShortName:	MIPIA_LP_RX_TIMEOUT_REG	
Power:	PG1	
Reset:	soft	
Address:	6B814h-6B817h	
Name:	MIPIC_LP_RX_TIMEOUT_REG	
ShortName:	MIPIC_LP_RX_TIMEOUT_REG	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:24	RESERVED
		Format: MBZ
	23:0	LOW_POWER_RECEPTION_TIMEOUT_COUNTER
		Access: R/W
		Timeout value to be checked for received short packets. If the timer expires the DSI Host enters stop state



MIPI_MAX_RETURN_PKT_SIZE_REGISTER

MIPI_MAX_RETURN_PKT_SIZE_REGISTER		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B054h-6B057h	
Name:	MIPIA_MAX_RETURN_PKT_SIZE_REGISTER	
ShortName:	MIPIA_MAX_RETURN_PKT_SIZE_REGISTER	
Power:	PG1	
Reset:	soft	
Address:	6B854h-6B857h	
Name:	MIPIC_MAX_RETURN_PKT_SIZE_REGISTER	
ShortName:	MIPIC_MAX_RETURN_PKT_SIZE_REGISTER	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:10	RESERVED
		Format: MBZ
	9:0	MAX_RETURN_PKT_SIZE Access: R/W Set the count value in bytes to collect the return data packet for reverse direction data flow in data lane0 in response to a DBI read operation



MIPI_PORT_CTRL

MIPI_PORT_CTRL				
Register Space: MMIO: 0/2/0				
Source: BSpec				
Default Value: 0x2010A060				
Access: R/W				
Size (in bits): 32				
Address: 6B0C0h-6B0C3h				
Name: MIPIA_PORT_CTRL				
ShortName: MIPIA_PORT_CTRL				
Power: PG1				
Reset: soft				
Address: 6B8C0h-6B8C3h				
Name: MIPIC_PORT_CTRL				
ShortName: MIPIC_PORT_CTRL				
Power: PG1				
Reset: soft				
DWord	Bit	Description		
0	31	EN		
		Access: R/W		
		When this bit is disabled the MIPI DPI (video mode) is inactive and in it's low power state. When it is enabled it starts to generate timing for this MIPI port.		
		Value	Name	Description
		0	Disable	The port is disabled and all MIPI DPI interface are disable (timing generator is off)
		1	Enable	The port is enabled
		Programming Notes		
		For MIPI dual-link in DPI mode, the port enable bits in both MIPI A control register and MIPI C control register shall be enabled.		
		30:27		ADJDLY_HSTX
Default Value: 0100b				
Access: R/W				
These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4 which is the equivalent of 1 buffer delay.				



MIPI_PORT_CTRL		
25:24	RESERVED	
	Format:	MBZ
23	SELFLOPPED_HSTX	
	Access:	R/W
	This bit muxes between the flopped (new) and unflopped (original) versions of the TX HS clock and data.	
	Value	Name Description
	0	Disable
1	Enable	Pass through the new flopped version of these signals
22	RESERVED	
	Format:	MBZ
21:18	FLISDSI_ADJDLY_HSTX_MIPIA	
	Default Value:	0100b
	Access:	R/W
	These bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4 which is the equivalent of 1 buffer delay.	
17	AFE_LATCHOUT	
	Access:	RO
	This bit reflects the value of the output latch of CLK A lane in DSI AFE b. The software driver can read this bit to see if the hold value (LP11 or LP00) to initialize from a sleep state (s0i1 or S0i3) correctly	
	Value	Name Description
	1	LP11
0	LP00	Current value of output latch is 0 (D-PHY is in LP00 state)
16	LPOUTPUT_HOLD	
	Access:	R/W
	Value	Name Description
	0	Disable
1	Enable	Enable transparent latch inside DSI AFE so data are driven by DSI DPHY
15	FLISDSI_ADJDLY_HSTX_MIPIC_HIGH_ORDER	
	Default Value:	1
	Access:	R/W
	The fourth bit of four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 1 which is the equivalent of 1 buffer delay.	



MIPI_PORT_CTRL		
14:11	MIPI4DPHY_AdjDly_HSTX_MIPI_C	
	Default Value:	0100b
	Access:	R/W
	These four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 4 which is the equivalent of 1 buffer delay.	
10:8	Spare 10 to 8	
	Access:	R/W
Reserved R/W for future use.		
7:5	FLISDSI_AdjDly_HSTX_MIPI_C_LOWER_ORDER	
	Default Value:	011b
	Access:	R/W
	The lower 3-bit of four bits act as an encoded count of the number of buffer delays to insert on the ckdsi2x clock going to the six flops that are storing the HS TX data and clock signals. Default is 3 which is the equivalent of 1 buffer delay.	
4	TE Counter Delay	
	Access:	R/W
	When enabled, DSI controller will start processing the subsequent frame only after the TE Delay Counter specified by bits 15:0 of the MIPI_TE_CTR register expires.	
	Value	Name
	0	Disable
	1	Enable
3:2	EFFECT	
	Access:	R/W
	Value	Name
	00b	No tearing effect required
	01b	TE trigger by MIPI DPHY and DSI protocol
	10b	TE trigger by GPIO pin
	11b	Reserved
	Description	Memory write start as soon as write data is available
1	Reserved	
	Format:	MBZ



MIPI_RD_DATA_RETURN

MIPI_RD_DATA_RETURN				
Register Space:	MMIO: 0/2/0			
Source:	BSpec			
Default Value:	0x00000000			
Access:	RO			
Size (in bits):	32			
Address:	6B118h-6B137h			
Name:	MIPIA_RD_DATA_RETURN			
ShortName:	MIPIA_RD_DATA_RETURN_*			
Power:	PG1			
Reset:	soft			
Address:	6B918h-6B937h			
Name:	MIPIC_RD_DATA_RETURN			
ShortName:	MIPIC_RD_DATA_RETURN_*			
Power:	PG1			
Reset:	soft			
There are multiple instances of this register format per MIPI port.				
DWord	Bit	Description		
0	31:0	RD_DATA_RETURN_PANEL		
		<table><tr><td>Access:</td><td>RO</td></tr></table>	Access:	RO
Access:	RO			
		This is the configuration data returned from the panel		



MIPI_RD_DATA_VALID

MIPI_RD_DATA_VALID		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Access: R/W		
Size (in bits): 32		
Address: 6B138h-6B13Bh		
Name: MIPIA_RD_DATA_VALID		
ShortName: MIPIA_RD_DATA_VALID		
Power: PG1		
Reset: soft		
Address: 6B938h-6B93Bh		
Name: MIPIC_RD_DATA_VALID		
ShortName: MIPIC_RD_DATA_VALID		
Power: PG1		
Reset: soft		
DWord	Bit	Description
0	31:8	RESERVED
		Format: MBZ
	7:0	READ_DATA_VALID
		Access: R/WC
		Each bit corresponds to presence of valid data in the registers above. When data is returned from the panel, H/W will write into these registers in sequence, and set the corresponding valid bit. SW must write a 1b to clear this bit.



MIPI_STATUS

MIPI_STATUS				
Register Space: MMIO: 0/2/0				
Source: BSpec				
Default Value: 0x00000000				
Access: R/W				
Size (in bits): 32				
Address: 6B0C4h-6B0C7h				
Name: MIPIA_STATUS				
ShortName: MIPIA_STATUS				
Power: PG1				
Reset: soft				
Address: 6B8C4h-6B8C7h				
Name: MIPIC_STATUS				
ShortName: MIPIC_STATUS				
Power: PG1				
Reset: soft				
DWord	Bit	Description		
0	31	Sideband TE		
		Access:	R/WC	
		This is a status bit which is set when a TE indication is received on the TE pin. Clear this bit by writing a 1b to it.		
		Value	Name	Description
		0b	No TE	No TE indication
		1b	TE	TE indication received.
	30	TE message in LP mode		
		Access:	R/WC	
		This is a status bit which is set when TE signaling in DSI mode is received in LP mode. Clear this bit by writing a 0b to it.		
		Value	Name	Description
		0b	No TE	No TE indication
		1b	TE	TE indication received.
	29	MIPI idle		
		Access:	R/WC	
		This is a status bit which is set when MIPI_AUTO_PWG_ENABLE (MIPI_AUTOPWG[0])is set and the DSI controller is done sending the last frame in Command Mode. Clear this bit by writing a 1b to		



MIPI_STATUS											
		it.									
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0b</td><td>MIPI Not Idle</td><td>DSI controller is not idle</td></tr><tr><td>1b</td><td>MIPI Idle</td><td>DSI Controller is idle.</td></tr></table>	Value	Name	Description	0b	MIPI Not Idle	DSI controller is not idle	1b	MIPI Idle	DSI Controller is idle.
		Value	Name	Description							
	0b	MIPI Not Idle	DSI controller is not idle								
	1b	MIPI Idle	DSI Controller is idle.								
28:0	RESERVED										
	Format:	MBZ									



MIPI_STOP_STATE_STALL

MIPI_STOP_STATE_STALL		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B08Ch-6B08Fh	
Name:	MIPIA_STOP_STATE_STALL	
ShortName:	MIPIA_STOP_STATE_STALL	
Power:	PG1	
Reset:	soft	
Address:	6B88Ch-6B88Fh	
Name:	MIPIC_STOP_STATE_STALL	
ShortName:	MIPIC_STOP_STATE_STALL	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:8	RESERVED
		Format: MBZ
	7:0	MIPI_STOP_STATE_STALL_COUNTER
		Access: R/W



MIPI_TE_CTR

MIPI_TE_CTR		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B108h-6B10Bh	
Name:	MIPIA_TE_CTR	
ShortName:	MIPIA_TE_CTR	
Power:	PG1	
Reset:	soft	
Address:	6B908h-6B90Bh	
Name:	MIPIC_TE_CTR	
ShortName:	MIPIC_TE_CTR	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:0	TE Delay Counter
		Default Value: 0 No Delay programmed
		Access: R/W
	This is the number of MIPI host clocks of delay from the TE trigger to when the DSI controller will start processing the subsequent frame. This counter is only valid if bit 4 of the MIPI_PORT_CTRL register is set.	



MIPI_TRANS_HACTIVE

MIPI_TRANS_HACTIVE		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B0F8h-6B0FBh	
Name:	MIPIA_TRANS_HACTIVE	
ShortName:	MIPIA_TRANS_HACTIVE	
Power:	PG1	
Reset:	soft	
Address:	6B8F8h-6B8FBh	
Name:	MIPIC_TRANS_HACTIVE	
ShortName:	MIPIC_TRANS_HACTIVE	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:13	RESERVED
		Format: MBZ
	12:0	Horizontal Active
		Access: R/W This field specifies Horizontal Active Display size.



MIPI_TRANS_VACTIVE

MIPI_TRANS_VACTIVE		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B0FCh-6B0FFh	
Name:	MIPIA_TRANS_VACTIVE	
ShortName:	MIPIA_TRANS_VACTIVE	
Power:	PG1	
Reset:	soft	
Address:	6B8FCh-6B8FFh	
Name:	MIPIC_TRANS_VACTIVE	
ShortName:	MIPIC_TRANS_VACTIVE	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:13	RESERVED
		Format: MBZ
	12:0	Vertical Active
		Access: R/W
		This field specifies Vertical Active Display size.



MIPI_TRANS_VTOTAL

MIPI_TRANS_VTOTAL		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B100h-6B103h	
Name:	MIPIA_TRANS_VTOTAL	
ShortName:	MIPIA_TRANS_VTOTAL	
Power:	PG1	
Reset:	soft	
Address:	6B900h-6B903h	
Name:	MIPIC_TRANS_VTOTAL	
ShortName:	MIPIC_TRANS_VTOTAL	
Power:	PG1	
Reset:	soft	
MIPI A Enable Delay Counter		
DWord	Bit	Description
0	31:13	RESERVED
		Format: MBZ
	12:0	Vertical Total
		Access: R/W
This field specifies Vertical Total size. This field is programmed to the number of lines desired minus one.		



MIPI_TURN_AROUND_TIMEOUT_REG

MIPI_TURN_AROUND_TIMEOUT_REG		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B018h-6B01Bh	
Name:	MIPIA_TURN_AROUND_TIMEOUT_REG	
ShortName:	MIPIA_TURN_AROUND_TIMEOUT_REG	
Power:	PG1	
Reset:	soft	
Address:	6B818h-6B81Bh	
Name:	MIPIC_TURN_AROUND_TIMEOUT_REG	
ShortName:	MIPIC_TURN_AROUND_TIMEOUT_REG	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:6	RESERVED
		Format: MBZ
	5:0	TURN_AROUND_TIMEOUT_REGISTER
		Access: R/W Timeout value to be checked after the DSI host makes a turn around in the direction of transfers. If the timer expires the DSI Host enters stop state



MIPI_VERT_BACK_PORCH_COUNT

MIPI_VERT_BACK_PORCH_COUNT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B03Ch-6B03Fh	
Name:	MIPIA_VERT_BACK_PORCH_COUNT	
ShortName:	MIPIA_VERT_BACK_PORCH_COUNT	
Power:	PG1	
Reset:	soft	
Address:	6B83Ch-6B83Fh	
Name:	MIPIC_VERT_BACK_PORCH_COUNT	
ShortName:	MIPIC_VERT_BACK_PORCH_COUNT	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:0	VERTICAL_BACK_PORCH_COUNT
		Access: R/W Shows the vertical back porch value in terms of lines



MIPI_VERT_FRONT_PORCH_COUNT

MIPI_VERT_FRONT_PORCH_COUNT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B040h-6B043h	
Name:	MIPIA_VERT_FRONT_PORCH_COUNT	
ShortName:	MIPIA_VERT_FRONT_PORCH_COUNT	
Power:	PG1	
Reset:	soft	
Address:	6B840h-6B843h	
Name:	MIPIC_VERT_FRONT_PORCH_COUNT	
ShortName:	MIPIC_VERT_FRONT_PORCH_COUNT	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:0	VERTICAL_FRONT_PORCH_COUNT
		Access: R/W Shows the vertical front porch value in terms of lines



MIPI_VERT_SYNC_PADDING_COUNT

MIPI_VERT_SYNC_PADDING_COUNT		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B038h-6B03Bh	
Name:	MIPIA_VERT_SYNC_PADDING_COUNT	
ShortName:	MIPIA_VERT_SYNC_PADDING_COUNT	
Power:	PG1	
Reset:	soft	
Address:	6B838h-6B83Bh	
Name:	MIPIC_VERT_SYNC_PADDING_COUNT	
ShortName:	MIPIC_VERT_SYNC_PADDING_COUNT	
Power:	PG1	
Reset:	soft	
DWord	Bit	Description
0	31:16	RESERVED
		Format: MBZ
	15:0	VERTICAL_SYNC_PADDING_COUNT
		Access: R/W Shows the vertical sync padding value in terms of lines



MIPI_VIDEO_MODE_FORMAT_REGISTER

MIPI_VIDEO_MODE_FORMAT_REGISTER				
Register Space:		MMIO: 0/2/0		
Source:		BSpec		
Default Value:		0x00000000		
Access:		R/W		
Size (in bits):		32		
Address:		6B058h-6B05Bh		
Name:		MIPIA_VIDEO_MODE_FORMAT_REGISTER		
ShortName:		MIPIA_VIDEO_MODE_FORMAT_REGISTER		
Power:		PG1		
Reset:		soft		
Address:		6B858h-6B85Bh		
Name:		MIPIC_VIDEO_MODE_FORMAT_REGISTER		
ShortName:		MIPIC_VIDEO_MODE_FORMAT_REGISTER		
Power:		PG1		
Reset:		soft		
DWord	Bit	Description		
0	31:6	RESERVED		
		Format:	MBZ	
	5	RESERVED		
		Format:	MBZ	
	4	De_feature		
		Access:	R/W	
		Set by the processor to support random DPI display resolution.		
		Value	Name	Description
		0	disabled	Random DPI display resolution support disabled.
		1	enabled	Random DPI display resolution support enabled.
	3	Video_BTA_Disable		
		Access:	R/W	
		Set by the processor to inform the DSI controller to disable the BTA sent at the last blanking line of VFP. By default, this bit is set to '0'.		
		Value	Name	Description
0		enable	BTA sending at the last blanking line of VFP is enabled.	
1	disable	BTA sending at the last blanking line of VFP is disabled.		



MIPI_VIDEO_MODE_FORMAT_REGISTER

MIPI_VIDEO_MODE_FORMAT_REGISTER				
	2	IP_TG_CONFIG		
		Access: R/W		
		Set by the processor to inform that the DSI controller should discontinue the DPI transfer after the last line of the VFP after ip_tg_enable deassertion. By default, this bit is set to 0.		
		Value	Name	Description
		0	disable	After ip_tg_enable deassertion, DSI Tx controller stops the DPI transfer immediately after the current packet is transmitted.
	1:0	1	enable	After ip_tg_enable deassertion, DSI Tx controller discontinues the DPI transfer after the last line of the VFP
		VIDEO_MODE_FMT		
		Access: R/W		
		Sets the Video mode format (packet sequence) to be supported in DSI. In Non Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed equal to RGB word count value In Burst Mode, in addition to programming this register the horizontal active area count register value should also be programmed greater than the RGB word count value, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.		
		Value	Name	
		00b	Reserved	
		01b	Non Burst Mode with Sync Pulse	
		10b	Non Burst Mode with Sync events	
		11b	Burst Mode	



MIPI_WR_COMMAND

MIPI_WR_COMMAND		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6B0ECh-6B0EFh	
Name:	MIPIA_WR_COMMAND	
ShortName:	MIPIA_WR_COMMAND	
Power:	PG1	
Reset:	soft	
Address:	6B8ECh-6B8EFh	
Name:	MIPIC_WR_COMMAND	
ShortName:	MIPIC_WR_COMMAND	
Power:	PG1	
Reset:	soft	
MIPI Write Data		
DWord	Bit	Description
0	31:8	RESERVED
		Format: MBZ
	7:0	MIPI_WR COMMAND
		Access: R/W
This register contains the command to be transferred to the panel in command mode.		



MIPI_WR_DATA

MIPI_WR_DATA			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	6B0CCh-6B0EBh		
Name:	MIPIA_WR_DATA		
ShortName:	MIPIA_WR_DATA_*		
Power:	PG1		
Reset:	soft		
Address:	6B8CCh-6B8EBh		
Name:	MIPIC_WR_DATA		
ShortName:	MIPIC_WR_DATA_*		
Power:	PG1		
Reset:	soft		
MIPI Write Data			
There are multiple instances of this register format per MIPI Port.			
DWord	Bit	Description	
0	31:0	WR_Data	
		Access:	R/W
		These registers contain the parameters for the command to be transferred to the panel in command mode.	



Mirror of Base Data of Stolen Memory

BDSM_0_2_0_PCI - Mirror of Base Data of Stolen Memory			
Register Space: PCI: 0/2/0			
Source: BSpec			
Default Value: 0x00000000			
Size (in bits): 32			
Address: 0005Ch			
Mirror of BSDM_0_0_0_PCI. This register contains the base address of graphics data stolen DRAM memory.			
DWord	Bit	Description	
0	31:20	Graphics Base of Stolen Memory	
		Default Value:	000000000000b
		Access:	RO Variant
		This register contains bits 31 to 20 of the base address of stolen DRAM memory. BIOS determines the base of graphics stolen memory by subtracting the graphics stolen memory size (PCI Device 0 offset 52 bits 6:4) from TOLUD (PCI Device 0 offset BC bits 31:20).	
	19:1	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	0	Lock	
		Default Value:	0b
		Access:	RO Variant
This bit will lock all writeable settings in this register, including itself.			



Mirror of Capabilities A

CAPID0_A_0_2_0_PCI - Mirror of Capabilities A		
Register Space: PCI: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 00044h		
Mirror of CAPID0_A_0_0_0_PCI.		
DWord	Bit	Description
0	31	Display HD Audio Disable
		Default Value: 0b
		Access: RO Variant
	30	PEG12 Disable
		Default Value: 0b
		Access: RO Variant
	29	PEG11 Disable
		Default Value: 0b
		Access: RO Variant
	28	PEG10 Disable
		Default Value: 0b
		Access: RO Variant
	27	PCI Express Link Width Upconfig Disable
		Default Value: 0b
		Access: RO Variant
	26	DMI Width
		Default Value: 0b
		Access: RO Variant
	25	ECC Disable
		Default Value: 0b
		Access: RO Variant
	24	Force DRAM ECC Enabled
		Default Value: 0b
		Access: RO Variant
	23	VTd Disable
		Default Value: 0b

**CAPID0_A_0_2_0_PCI - Mirror of Capabilities A**

		Access:	RO Variant
		0: Enable VTd 1: Disable VTd	
22	DMI Gen 2 Disable		
		Default Value:	0b
		Access:	RO Variant
21	PEG Gen 2 Disable		
		Default Value:	0b
		Access:	RO Variant
20:19	DDR Size		
		Default Value:	00b
		Access:	RO Variant
18	Bclk overclocking disable		
		Default Value:	0b
		Access:	RO Variant
17	Disable 1N Mode		
		Default Value:	0b
		Access:	RO Variant
16	Full ULT Fuse Read Disable		
		Default Value:	0b
		Access:	RO Variant
15	Camarillo Device Disable		
		Default Value:	0b
		Access:	RO Variant
14	2 DIMMS per Channel Disable		
		Default Value:	0b
		Access:	RO Variant
13	X2APIC Enabled		
		Default Value:	0b
		Access:	RO Variant
12	Performance Dual Channel Disable		
		Default Value:	0b
		Access:	RO Variant
11	Internal Graphics Disable		
		Default Value:	0b



CAPID0_A_0_2_0_PCI - Mirror of Capabilities A

		Access:	RO Variant
		0b: There is a graphics engine within this CPU. Internal Graphics Device (Device 2) is enabled and all of its memory and I/O spaces are accessible. Configuration cycles to Device 2 will be completed within the CPU. All non-SMM memory and IO accesses to VGA will be handled based on Memory and IO enables of Device 2 and IO registers within Device 2 and VGA Enable of the PCI to PCI bridge control (If PCI Express GFX attach is supported). A selected amount of Graphics Memory space is pre-allocated from the main memory based on Graphics Mode Select (GMS in the GGC Register). Graphics Memory is pre-allocated above TSEG Memory. 1b: There is no graphics engine within this CPU. Internal Graphics Device (Device 2) and all of its memory and I/O functions are disabled. Configuration cycle targeted to Device 2 will be passed on. All non-SMM memory and IO accesses to VGA will be handled based on VGA Enable of the PCI to PCI bridge control. Device 2 is disabled and hidden.	
10	Reserved		
9:8	Capability Device ID		
		Default Value:	00b
		Access:	RO Variant
7:4	Compatibility Rev ID		
		Default Value:	0000b
		Access:	RO Variant
3	DDR Overclocking		
		Default Value:	0b
		Access:	RO Variant
2	IA Overclocking Enabled by DSKU		
		Default Value:	0b
		Access:	RO Variant
1	DDR Write Vref Enable		
		Default Value:	0b
		Access:	RO Variant
0	DDR3L Enable		
		Default Value:	0b
		Access:	RO Variant



Mirror of Capabilities B

CAPID0_B_0_2_0_PCI - Mirror of Capabilities B			
Register Space:		PCI: 0/2/0	
Source:		BSpec	
Default Value:		0x00000000	
Size (in bits):		32	
Address:		00048h	
Mirror of CAPID0_B_0_0_0_PCI.			
DWord	Bit	Description	
0	31	Reserved_31	
		Default Value:	0b
		Access:	RO Variant
	30	IA Overclocking DSKU Control Disable	
		Default Value:	0b
		Access:	RO Variant
	29	IA Overclocking Enable	
		Default Value:	0b
		Access:	RO Variant
	28	SMT Capability	
		Default Value:	0b
		Access:	RO Variant
	27:25	Cache Size Capability	
		Default Value:	000b
		Access:	RO Variant
	24	SVMDIS	
		Default Value:	0b SVM mode enabled
		Access:	RO Variant
	23:21	DDR3 Maximum Frequency Capability with 100 Memory	
		Default Value:	000b
		Access:	RO Variant
	20	Gen3 Disable Fuse for PCIe PEG Controllers	
		Default Value:	0b
		Access:	RO Variant
	19	Package Type	
		Default Value:	0b



CAPID0_B_0_2_0_PCI - Mirror of Capabilities B

		Access:	RO Variant
18	Additive Graphics Enabled		
	Default Value:	0b	
	Access:	RO Variant	
	0 - Additive Graphics Disabled 1 - Additive Graphics Enabled		
17	Additive Graphics Capable		
	Default Value:	0b	
	Access:	RO Variant	
	0 - Capable of Additive Graphics 1 - Not capable of Additive Graphics		
16	Primary PEG Port x16 Disable		
	Default Value:	0b	
	Access:	RO Variant	
15:12	Reserved_15_12		
	Default Value:	0000b	
	Access:	RO Variant	
11	Reserved		
10:8	Reserved_10_8		
	Default Value:	000b	
	Access:	RO Variant	
7	Reserved		
6:4	DDR3 Maximum Frequency Capability		
	Default Value:	000b	
	Access:	RO Variant	
3	Reserved_3		
	Default Value:	0b	
	Access:	RO Variant	
2	DDR4 DSKU Enable		
	Default Value:	0b	
	Access:	RO	
1	Dual PEG Force x1 when VGA Enabled		
	Default Value:	0b	
	Access:	RO Variant	

**CAPID0_B_0_2_0_PCI - Mirror of Capabilities B**

	0	Single PEG Force x1 when VGA Enabled	
		Default Value:	0b
		Access:	RO Variant



Mirror of Device Enable

DEVEN0_0_2_0_PCI - Mirror of Device Enable			
Register Space:		PCI: 0/2/0	
Source:		BSpec	
Default Value:		0x000000BF	
Size (in bits):		32	
Address:		00054h	
Mirror of DEVEN_0_0_0_PCI.			
DWord	Bit	Description	
0	14	Chap Enable	
		Default Value:	0b
		Access:	RO Variant
	13	Device 6 Enable	
		Default Value:	0b
		Access:	RO
	12:11	RESERVED	
		Default Value:	000b
		Access:	RO
	10	Device 5 Enable	
		Default Value:	0b
		Access:	RO
	9:8	RESERVED	
		Default Value:	000b
		Access:	RO
	7	Device 4 Enable	
		Default Value:	1b
		Access:	RO Variant
	6	RESERVED	
		Default Value:	000b
		Access:	RO
	5	Device 3 enable for Display HD Audio	
		Default Value:	1b
		Access:	RO Variant
	4	Internal Graphics Engine	
		Default Value:	1b

**DEVEN0_0_2_0_PCI - Mirror of Device Enable**

		Access:	RO Variant
		0: Bus 0 Device 2 is disabled and hidden 1: Bus 0 Device 2 is enabled and visible This bit will be set to 0b and remain 0b if Device 2 capability is disabled.	
	3	PEG10 Enable	
		Default Value:	1b
		Access:	RO Variant
	2	PEG11 Enable	
		Default Value:	1b
		Access:	RO Variant
	1	PEG12 Enable	
		Default Value:	1b
		Access:	RO Variant
	0	Host Bridge	
		Default Value:	1b
		Access:	RO



Mirror of FUSE2 Control DW

FUSE2 - Mirror of FUSE2 Control DW		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address: 09120h		
FUSE2 Control DW		
DWord	Bit	Description
0	31:29	GT SKU Fuse
		Access: RO GT SKU Fuse Bits See project specific configuration table for possible values.
	28	Spares
		Access: RO
	27:25	GT Slice Enable Fuse
		Access: RO Slice Enables Bit25 - Slice0 Enable Bit26 - Slice1 Enable Bit27 - Slice2 Enable See project specific configuration table for possible values.
24	Spares1	
	Access: RO	
23:20	GT Subslice Disable Fuse	
	Access: RO Subslice Disable Bits Bit 20 - Subslice0 Disable Bit 21 - Subslice1 Disable Bit 22 - Subslice2 Disable Bit 23 - Subslice3 Disable See project specific configuration table for possible values.	
19:18	GT VDBox and VEBBox Configuration Fuse	
	Access: RO VDBox and VEbox Configurations: 00b = Both VDBOXes and VEBOXes enabled	



FUSE2 - Mirror of FUSE2 Control DW				
		01b = VDBOX1 and VEBOX1 enabled (GT1,2) 10b = VDBOX0 and VEBOX0 enabled (GT1,2) See project specific configuration table for possible values.		
	17:16	Spares3 <table><tr><td>Access:</td><td>RO</td></tr></table>	Access:	RO
	Access:	RO		
15:0	Capability Fuse Fixed Definitions within Capability Fuse: Bit 2: Pre-production/post-production fuse. 0b : Pre-Production. Pre or Post Production quality FW will run 1b : Post Production.only Production quality FW will run Other bits defined by SW PDT. Please refer to Project Specific SW PDT for definition/values for these bits.			



MMCD Misc Control

MMCD_MISC_CTRL - MMCD Misc Control			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x8000003C	
Size (in bits):		32	
Address:		04DDCh	
This register contains control bits for permute control line address, page faulting mode and cache control bits			
DWord	Bit	Description	
0	31	Permute Compressed Line Address	
		Default Value:	1b
		Access:	R/W
		Controls where the compressed line is written in memory 1'b0: Write to lower CL address, i.e bit[X]=0 1'b1: Write based on the hash selection as indicated by bit[27] (default)	
	30	Reserved	
	29	Reserved	
	28	Reserved	
	27	Hash Select for Compressed Read/Write Address calculation	
		Default Value:	0b
		Access:	R/W
		1'b0: Legacy mode : Read/Write address computation will be done using a hash of Virtual address bits 6 to 11 bit[X] = bit[X] XOR bit[11] XOR bit[10] XOR bit[9] XOR bit[8] XOR bit[7] XOR bit[6] 1'b1: LLC/eLLC hot spotting avoidance mode : Read/Write address computation will be done using a hash of Virtual address bits 17 to 21 bit[X] = bit[X+1] XOR bit[17] XOR bit[18] XOR bit[19] XOR bit[20] XOR bit[21] Software needs to guarantee that the base address of the resource is aligned to 4MB or ensure that the virtual address is not changed between the passes for compressed surface handling	
	26:14	Reserved_1	
Default Value:		0b	
Access:		R/W	
13:11	Page Faulting Mode		
	Default Value:	0b	
	Access:	R/W	
this field controls page faulting mode that will be used in the memory interface block for the			

**MMCD_MISC_CTRL - MMCD Misc Control**

		given request coming from this surface 3'b000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
10:7	Reserved_2		
		Default Value:	0b
		Access:	R/W
6	Don't allocate on Miss		
		Default Value:	0b
		Access:	R/W
		Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM) 1'b0: Allocate on miss 1'b1: Do Not allocate on miss	
5:4	Cache Replcement management		
		Default Value:	3h
		Access:	R/W
		This field allows the selection of AGE parameter for a given surface in LLC or eLLC. If a particular allocation is done at youngest age 3 it tends to stay longer in cache as compared to older age allocation - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches 2'b11: Good chance of generating hits 2'b10: Poor chance of generating hits 2'b01: Don't change the LRU if it is a HIT 2'b00: Reserved	
3:2	Target Cache		
		Default Value:	3h
		Access:	R/W
		This field allows the choice of LLC vs eLLC for caching 2'b00: eLLC only 2'b01: LLC only 2'b10: LLC/eLLC allowed 2'b11: LLC/eLLC allowed	
1:0	LLC/eDRAM Cacheability control		
		Default Value:	0b
		Access:	R/W
		Memory type information used in LLC/eDRAM 2'b00: Use cacheability controls from page table/ UC with fence (if coherent cycle)	



MMCD_MISC_CTRL - MMCD Misc Control		
		2'b01: Uncacheable(UC) - non-cacheable 2'b10: Writethrough (WT) 2'b11: Writeback (WB)



MMIO_INDEX

MMIO_INDEX - MMIO_INDEX			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	00000h		
Contains address and target. Punit cannot access IO space from message channel. A 32 bit IO write to this port loads the offset of the MMIO register or offsetinto the GTT that needs to be accessed. An IO Read returns the current value of this register. An 8/16 bit IO write to this register is completed but does not update this register. This mechanism to access internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports. This is used by SBIOS. It is not used by graphics driver. This register is only accessible through the IOSF Primary bus. The base register is defined by IOBAR.			
DWord	Bit	Description	
0	31:2	Register_offset	
		Default Value:	00000000h
		Access:	R/W
		This field selects GTT entry or any one of the Dword registers within the MMIO register space of this device.	
	1:0	Target	
		Default Value:	00b
		Access:	R/W
		00 = MMIO Registers, 01 = GTT, 1X = Reserved	



MMIO Mirror of GMCH Graphics Control Register

MGGC_ - MMIO Mirror of GMCH Graphics Control Register			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000500	
Access:		RO	
Size (in bits):		32	
Address:		108040h	
All the bits in this register are Intel TXT lockable.			
DWord	Bit	Description	
0	31:16	RESERVED	
		Default Value:	000h
		Access:	RO
		Reserved	
	15:8	GMS	
		Default Value:	05h
		Access:	RO
		This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. It corresponds to DSM (Data Stolen Memory region) region. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.	
		Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled.	
		BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0.	
BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions.			
00h:0MB			
01h:32MB			
02h:64MB			
03h:96MB			
04h:128MB			
05h:160MB			
06h:192MB			
07h:224MB			
08h:256MB			
09h:288MB			
0Ah:320MB			
0Bh:352MB			
0Ch:384MB			

**MGGC_ - MMIO Mirror of GMCH Graphics Control Register**

0Dh:416MB
0Eh:448MB
0Fh:480MB
10h:512MB
11h - 1Fh: Reserved
20h:1024MB
21h - 2Fh: Reserved
30h:1536MB
31h - 3Fh: Reserved
40h: 2048MB
41h - EFh: Reserved
F0h: 4MB
F1h: 8MB
F2h: 12MB
F3h: 16MB
F4h: 20MB
F5h: 24MB
F6h: 28MB
F7h: 32MB
F8h: 36MB
F9h: 40MB
FAh: 44MB
FBh: 48MB
FCh: 52MB
FDh: 56MB
FEh: 60MB
FFh: Reserved
Hardware functionality in case of programming this value to Reserved is not guaranteed.

7:6 GGMS

Default Value:	00b

Access:	RO

This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled.

GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register.

Hardware functionality in case of programming this value to Reserved is not guaranteed.

0x0:No Preallocated Memory

0x1:2MB of Preallocated Memory

0x2:4MB of Preallocated Memory

0x3:8MB of Preallocated Memory



MGGC_ - MMIO Mirror of GMCH Graphics Control Register

5:3	RESERVED	
	Default Value:	000b
	Access:	RO
	Enables the use of the iGFX enbines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.	
2	VAMEN	
	Default Value:	0b
	Access:	RO
	Reserved	
1	IVD	
	Default Value:	0b
	Access:	RO
	0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field (bits 7:3 of this register) pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0). This register is locked by Intel TXT lock. 0:Enable 1:Disable	
0	GGCLCK	
	Default Value:	0b
	Access:	RO
	When set to 1b, this bit will lock all bits in this register.	



MTOLUD

MTOLUD - MTOLUD			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00100000		
Size (in bits):	32		
Address:	108000h		
This 32 bit register defines the Top of Low Usable DRAM. TSEG, GTT Graphics memory and Graphics Stolen Memory are within the DRAM space defined. From the top, the Host optionally claims 1 to 64MBs of DRAM for internal graphics if enabled, 1or 2MB of DRAM for GTT Graphics Stolen Memory (if enabled) and 1, 2, or 8 MB of DRAM for TSEG if enabled. Programming Example: C1DRB3 is set to 4GB TSEG is enabled and TSEG size is set to 1MB Internal Graphics is enabled, and Graphics Mode Select is set to 32MB GTT Graphics Stolen Memory Size set to 2MB BIOS knows the OS requires 1G of PCI space. BIOS also knows the range from 0_FEC0_0000h to 0_FFFF_FFFFh is not usable by the system. This 20MB range at the very top of addressable memory space is lost to APIC and LT. According to the above equation, TOLUD is originally calculated to: 4GB = 1_0000_0000h The system memory requirements are: 4GB (max addressable space) - 1GB (pci space) - 35MB (lost memory) = 3GB - 35MB (minimum granularity) = 0_ECB0_0000h Since 0_ECB0_0000h (PCI and other system requirements) is less than 1_0000_0000h, TOLUD should be programmed to ECBh. These bits are Intel TXT lockable.			
DWord	Bit	Description	
0	31:20	TOLUD	
		Default Value:	001h
		Access:	RO Variant
		This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory below 4G that is usable by the operating system. Address bits 31 down to 20 programmed to 01h implies a minimum memory size of 1MB. Configuration software must set this value to the smaller of the following 2 choices: maximum amount memory in the system minus ME stolen memory plus one byte or the minimum address allocated for PCI memory. Address bits 19:0 are assumed to be 0_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register. The Top of Low Usable DRAM is the lowest address above both Graphics Stolen memory and Tseg. BIOS determines the base of Graphics Stolen Memory by subtracting the Graphics Stolen Memory Size from TOLUD and further decrements by Tseg size to determine base of Tseg. All	



MTOLUD - MTOLUD			
		the Bits in this register are locked in LT mode. This register must be 1MB aligned when reclaim is enabled.	
	19:1	RESERVED	
		Default Value:	000h
		Access:	RO Variant
		Reserved	
	0	LOCK	
		Default Value:	0b
		Access:	RO Variant
		This bit will lock all writeable settings in this register, including itself.	



MTOUUD_LSB

MTOUUD_LSB - MTOUUD_LSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00100000		
Size (in bits):	32		
Address:	108080h		
This 64 bit register defines the Top of Upper Usable DRAM. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit + 1byte, 1MB aligned, since reclaim limit is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB. BIOS Restriction: Minimum value for TOUUD is 4GB. These bits are Intel TXT lockable.			
DWord	Bit	Description	
0	31:20	TOUUD	
		Default Value:	001h
		Access:	RO
		This register contains bits 38 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system.	
	Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 1MB aligned since reclaim limit + 1byte is 1MB aligned.		
	Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB.		
	All the bits in this register are locked in Intel TXT mode.		
	19:1	RESERVED	
		Default Value:	000h
		Access:	RO
		Reserved	
	0	LOCK	
Default Value:		0b	
Access:		RO	
This bit will lock all writeable settings in this register, including itself.			



MTOUUD_MSB

MTOUUD_MSB - MTOUUD_MSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	108084h		
This 64 bit register defines the Top of Upper Usable DRAM. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit + 1byte, 1MB aligned, since reclaim limit is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than or equal to 4GB. BIOS Restriction: Minimum value for TOUUD is 4GB. These bits are Intel TXT lockable.			
DWord	Bit	Description	
0	31:7	RESERVED	
		Default Value:	0000000h
		Access:	RO
		Reserved	
	6:0	TOUUD	
		Default Value:	00h
Access:		RO	
This register contains bits 38 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. Configuration software must set this value to TOM minus all ME stolen memory if reclaim is disabled. If reclaim is enabled, this value must be set to reclaim limit 1MB aligned since reclaim limit + 1byte is 1MB aligned. Address bits 19:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards DRAM if the incoming address is less than the value programmed in this register and greater than 4GB. All the bits in this register are locked in Intel TXT mode.			



Multi Size Aperture Control

MSAC_0_2_0_PCI - Multi Size Aperture Control

Register Space: PCI: 0/2/0
Source: BSpec
Default Value: 0x00000001
Size (in bits): 8

Address: 00062h

This register determines the size of the graphics memory aperture (GMADR) in function 0 and in the trusted space, and affects certain bits of the GMADR register.

Bits [4:0] 00000b: 128MB, GMADR[26:4] is hardwired to all 0

Bits [4:0] 00001b: 256MB, GMADR[27:4] overridden to all 0

Bits [4:0] 00010b: illegal (hardware will treat this as 00011b)

Bits [4:0] 00011b: 512MB, GMADR[28:27] overridden to all 0

Bits [4:0] 00100-00110b: illegal (hardware will treat this as 00111b)

Bits [4:0] 00111b: 1024MB, GMADR[29:27] overridden to all 0

Bits [4:0] 01000-01110b: illegal (hardware will treat this as 01111b)

Bits [4:0] 01111b: 2048MB, GMADR[30:27] overridden to all 0

Bits [4:0] 10000-11110b: illegal (hardware will treat this as 11111b)

Bits [4:0] 11111b: 4096MB, GMADR[31:27] overridden to all 0

DWord	Bit	Description
0	7:5	Reserved R/W
		Default Value: 000b
		Access: R/W
		Scratch Bits
	4	Untrusted Aperture Size Bit 4
		Default Value: 0b
		Access: R/W Key
	3	Untrusted Aperture Size Bit 3
		Default Value: 0b
		Access: R/W Key
	2	Untrusted Aperture Size Bit 2
		Default Value: 0b
		Access: R/W Key
	1	Untrusted Aperture Size Bit 1
		Default Value: 0b
		Access: R/W Key



MSAC_0_2_0_PCI - Multi Size Aperture Control			
	0	Untrusted Aperture Size Bit 0	
		Default Value:	1b
		Access:	R/W Key



NDE_RSTWRN_OPT

NDE_RSTWRN_OPT			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	46408h-4640Bh		
Name:	North Display Reset Warn Options		
ShortName:	NDE_RSTWRN_OPT		
Power:	PG0		
Reset:	global		
This register is used to control the display behavior on receiving a Reset Warning.			
DWord	Bit	Description	
0	31:7	Reserved	
		Format: MBZ	
	6	Reserved	
		Format: MBZ	
	5	Reserved	
	4	RST PCH Handshake En	
		This field enables the handshake with PCH display when processing the reset. This applies to all types of DE resets.	
		By default it is disabled and the north display will not wait for south display to acknowledge the reset.	
		Value	Name
		0b	Disable
1b		Enable	
Programming Notes			
This field must never be programmed to 1b.			
3:0	Reserved		



Observation Architecture Control per Context

OACTXCONTROL - Observation Architecture Control per Context			
Register Space:		MMIO: 0/2/0	
Source:		RenderCS	
Default Value:		0x00000000	
Access:		R/W	
Size (in bits):		32	
Address:		02360h	
This register is implemented in render command streamer and render context save/restored. This register should be initialized by SW appropriately on the very first submission of a context when OA is enabled.			
DWord	Bit	Description	
0	31	Reserved	
		Format:	PBC
	30:8	Reserved	
		Format:	PBC
	7:2	Timer Period	
Format:		Select	
Specifies the period of the timer strobe as a function of the minimum TIME_STAMP resolution. The period is determined by selecting a specified bit from the TIME_STAMP register as follows: StrobePeriod = MinimumTimeStampPeriod * 2 (TimerPeriod + 1) The exponent is defined by this field.			
Note: The TIME_STAMP is not reset at start time so the phase of the strobe is not synchronized with the enable of the OA unit. This could result in approximately a full StrobePeriod elapsing prior to the first trigger. Usage for this mechanism should be time based periodic triggering, typically.			
1	Timer Enable		
	Format:	Enable	
	Description This field enables the timer logic to output a periodic strobe, as defined by the Timer Period. When disabled the timer output is not asserted. Users should be aware that the timer-based report logic and the Boolean report trigger logic are logically OR'd together with no buffering of report triggers. This implies that only one performance counter report will be generated for clocks where both the timer-based report logic and the Boolean report trigger logic trigger a performance counter report. When "Specific Context Enable" bit is set to '1' in OACONTROL register, Timer based report		

**OACTXCONTROL - Observation Architecture Control per Context**

trigger function gets enabled only for the selected context.
When "Specific Context Enable" bit is set to '0' in OACONTROL register, Timer based report trigger function gets enabled for all contexts.

Value	Name	Description
0h	Disable [Default]	Counter does not get written out on regular interval
1h	Enable	Counter gets written out on regular intervals, defined by the Timer Period

0 Counter Stop-Resume Mechanism

Format:	Select

Value	Name	Description
1h		resume counting for all counters



Outstanding Page Request Allocation

OPRA_0_2_0_PCI - Outstanding Page Request Allocation		
Register Space: PCI: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 0030Ch		
DWord	Bit	Description
0	31:0	Outstanding Page Request Allocation
		Default Value: 00000000000000000000000000000000b
		Access: R/W
		This register contains the number of outstanding page request messages the associated Page Request Interface is allowed to issue.



Outstanding Page Request Capacity

OPRC_0_2_0_PCI - Outstanding Page Request Capacity			
Register Space:		PCI: 0/2/0	
Source:		BSpec	
Default Value:		0x00008000	
Size (in bits):		32	
Address:		00308h	
DWord	Bit	Description	
0	31:0	Outstanding Page Request Capacity	
		Default Value:	00000000000000000100000000000000b
		Access:	RO
		This register contains the number of outstanding page request messages the associated Page Request Interface physically supports. This is the upper limit on the number of pages that can be usefully allocated to the Page Request Interface. Hardwired to 32,768 requests.	



Page Request Control

PR_CTRL_0_2_0_PCI - Page Request Control		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	16	
Address:	00304h	
DWord	Bit	Description
0	15:2	RESERVED
		Default Value: 000b
		Access: RO
		Reserved
	1	Reset
		Default Value: 0b
	0	Page-Request Enable
		Default Value: 0b
		Access: R/W
		When Set, indicates that the page request interface on the endpoint is allowed to make page requests. If both this field and the Stopped field in Page Request Status register are Clear, then the Page request interface will not issue new page requests, but has outstanding page requests for which page responses is not yet received. When this field transitions from 0 to 1, all the status fields in the Page-Request Status register are cleared. Enabling a page request interface that has not successfully stopped has indeterminate results.



Page Request Extended Capability Header

PR_EXTCAP_0_2_0_PCI - Page Request Extended Capability Header			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00010013		
Size (in bits):	32		
Address:	00300h		
Page Request Extended Capability reports support for page-faults on Device-2, compliant to PCI-Express ATS 1.1 Specification			
DWord	Bit	Description	
0	31:20	Next Capability Offset	
		Default Value:	000000000000b
		Access:	RO
		This is a hardwired pointer to the next item in the capabilities list. Value 000h indicates that this is the end of the PCI-Express Extended capability Linked List.	
	19:16	Version	
		Default Value:	0001b
		Access:	RO
		Hardwired to capability version 1.	
	15:0	Capability ID	
		Default Value:	0000000000010011b
		Access:	RO
		Hardwired to the Page Request Extended Capability ID	



Page Request Status

PR_STATUS_0_2_0_PCI - Page Request Status			
Register Space:		PCI: 0/2/0	
Source:		BSpec	
Default Value:		0x00008000	
Size (in bits):		16	
Address:		00306h	
DWord	Bit	Description	
0	15	PRG Response PASID Required	
		Default Value:	1b
		Access:	RO
		If set, the Function expects a PASID TLP Prefix on PRG Response Messages when the corresponding page requests had a PASID TLP Prefix. If Clear, the function does not expect PASID TLP Prefixes on any PRG Response Message. Function behavior is undefined if this bit is Clear and the Function receives a PRG Response Message with a PASID TLP Prefix. Function behavior is undefined if this bit is Set and the Function receives a PRG Response Message with no PASID TLP Prefix when the corresponding Page Requests had a PASID TLP Prefix. This bit is RsvdZ if the Function does not support the PASID TLP Prefix.	
	14:9	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	8	Stopped	
		Access:	RO
		When this field is Set, the associated page request interface has stopped issuing additional Page requests and that all previously issued Page requests have completed. When this field is clear the associate Page request interface either has not stopped or has stopped issuing new Page requests but has outstanding Page requests.	
		Value	Name
0b		[Default]	
7:2	RESERVED		
	Default Value:	000b	
	Access:	RO	
	Reserved		

**PR_STATUS_0_2_0_PCI - Page Request Status**

1	Unexpected Page Request Group Index			
	<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W One Clear</td></tr></table> When Set, indicates the function received a PRG response message containing a PRG index that has no matching request, a response failure. This field is Set by the Function and cleared when a 1b is written to the field.	Default Value:	0b	Access:
Default Value:	0b			
Access:	R/W One Clear			
0	Response Failure			
	<table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W One Clear</td></tr></table> When Set, indicates the function received a PRG response message indicating a response failure. The function expects no further response from the host (any received are ignored). This field is Set by the Function and cleared when a 1b is written to this field.	Default Value:	0b	Access:
Default Value:	0b			
Access:	R/W One Clear			



PAK_Stream-Out Report (Errors)

PAK_ERR - PAK_Stream-Out Report (Errors)		
Register Space:	MMIO: 0/2/0	
Source:	VideoCS	
Default Value:	0x00000000	
Access:	RO	
Size (in bits):	32	
Trusted Type:	1	
Address:	128E8h	
DWord	Bit	Description
0	31:22	Reserved
		Format: MBZ
	21	Incorrect IntraMBFlag in I-slice(AVCf)
	20	Out of Range Symbol Code(AVC/mpeg2)
	19	Incorrect MBType(AVC/mpeg2)
	18	Motion Vectors are not inside the frame boundary(mpeg2)
	17	Scale code is zero(mpeg2)
	16	Incorrect DCTtype for given motionType(mpeg2)
	15:8	MB Y-position
		Description This field indicates Macro Block(MB) Y- position where an error occurred while encoding.
	7:0	MB X-position
		Description This field indicates Macro Block(MB) X- position where an error occurred while encoding.



PASID Capability

PASID_CAP_0_2_0_PCI - PASID Capability			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00001402		
Size (in bits):	16		
Address:	00104h		
PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.			
DWord	Bit	Description	
0	15:13	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	12:8	Maximum PASID Width	
		Default Value:	10100b
		Access:	RO
		Indicates the width of the PASID field supported by the Endpoint. Hardwired to 14h to indicate support for all PASID values (20 bits).	
	7:3	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	2	Privilege Mode Supported	
		Default Value:	0b
		Access:	RO
		Hardwired to 0, the Endpoint supports operating in Non-privileged mode only, and will never request privileged mode in requests-with-PASID.	
1	Execute Permission Supported		
	Access:	RO	
	Description		
	Hardwired to 1, the Endpoint supports requests-with-PASID that requests execute permission.		



PASID_CAP_0_2_0_PCI - PASID Capability			
		Value	Name
		1b	[Default]
	0	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	



PASID Control

PASID_CTRL_0_2_0_PCI - PASID Control			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	00106h		
Process Address Space ID (PASID) control for Device-2.			
DWord	Bit	Description	
0	15:3	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
		2	Privileged Mode Enable
			Default Value:
	Access:		RO
	Hardwired to 0, the Endpoint is not permitted to request privileged mode in requests-with-PASID.		
	1		Execute Permission Enable
			Default Value:
		Access:	R/W
		If Set, the Endpoint is permitted to request execute permission in requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with the Execute Request Enable field Set.	
		0	PASID Enable
			Default Value:
	Access:		R/W
	If Set, the Endpoint is permitted to generate requests-with-PASID. If Clear, the Endpoint is not permitted to do so. Behavior is undefined if this bit changes value when ATS Enable field in ATS Capability is Set. If Privileged Mode Supported field in PASID Capability register is Clear, then this field is treated as Reserved(0). Processor graphics does not use this field. Software is expected to Set this field before configuring extended-context-entry for Device-2 with Supervisor Request Enable field Set. For compatibility reasons, this field is implemented as RW.		



PASID Extended Capability Header

PASID_EXTCAP_0_2_0_PCI - PASID Extended Capability Header			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x2001001B		
Size (in bits):	32		
Address:	00100h		
PASID capability reports support for Process Address Space ID(PASID) on Device-2, compliant to PCI-Express PASID ECN.			
DWord	Bit	Description	
0	31:20	Next Capability Offset	
		Default Value:	001000000000b
		Access:	RO
		This is a hardwired pointer to the next item in the capabilities list.	
	19:16	Version	
		Default Value:	0001b
		Access:	RO
		Hardwired to capability version 1.	
	15:0	Capability ID	
		Default Value:	0000000000011011b
		Access:	RO
		Hardwired to the PASID Extended Capability ID	



PAT Index High

PAT_INDEX_H - PAT Index High			
Register Space:		MMIO: 0/2/0	
Default Value:		0x03030303	
Size (in bits):		32	
Address:		040E4h	
DWord	Bit	Description	
0	31:0	PAT Index High	
		Default Value:	03030303h
		Access:	R/W



PAT Index Low

PAT_INDEX_L - PAT Index Low		
Register Space:	MMIO: 0/2/0	
Default Value:	0x03030303	
Size (in bits):	32	
Address:	040E0h	
DWord	Bit	Description
0	31:0	PAT Index Low
		Default Value: 03030303h
		Access: R/W
		Bit[31:24]: PAT Index#3: Index#3 definition for page tables. (See bit[7:0] for definition.) Bit[23:16]: PAT Index#2: Index#2 definition for page tables. (See bit[7:0] for definition.) Bit[15:8]: PAT Index#1: Index#1 definition for page tables. (See bit[7:0] for definition.) Bit[7:0]: PAT Index#0: Index#0 definition for page tables. Bit[7]: Reserved. Bit[6]: Snoop Control. Note: S/W should NOT set this field in client platforms Bit[5:4]: (See below.) 00b: Age is 0. 01b: Age is 1. 10b: Age is 2. 11b: Age is 3. Bit[3:2]: (See below.) 00b: Override to eLLC Only. (This setting overrides the memory_object_control_state via surface state to be eLLC target only.) 01b: eLLC only. 10b: LLC only. 11b: eLLC/LLC. Bit[1:0]: (see below): 00b: Uncached with fence. 01b: Write Combining (traditional UC). 10b: Write Through. 11b: Write Back.



PCI Command

PCICMD_0_2_0_PCI - PCI Command			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	16		
Address:	00004h		
This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.			
DWord	Bit	Description	
0	15:11	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	10	Interrupt Disable	
		Default Value:	0b
		Access:	R/W
		This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.	
	9	Fast Back-to-Back	
		Default Value:	0b
		Access:	RO
		Not Implemented. Hardwired to 0.	
	8	SERR Enable	
		Default Value:	0b
		Access:	RO
		Not Implemented. Hardwired to 0.	
	7	Wait Cycle Control	
		Default Value:	0b
		Access:	RO
		Not Implemented. Hardwired to 0.	



PCICMD_0_2_0_PCI - PCI Command

	6	Parity Error Enable	
		Default Value:	0b
		Access:	RO
		Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.	
	5	Video Palette Snooping	
		Default Value:	0b
		Access:	RO
		This bit is hardwired to 0 to disable snooping.	
	4	Memory Write and Invalidate Enable	
		Default Value:	0b
		Access:	RO
		Hardwired to 0. The IGD does not support memory write and invalidate commands.	
	3	Special Cycle Enable	
		Default Value:	0b
		Access:	RO
		This bit is hardwired to 0. The IGD ignores Special cycles.	
	2	Bus Master Enable	
		Default Value:	0b
		Access:	R/W
		0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master.	
	1	Memory Access Enable	
		Default Value:	0b
		Access:	R/W
		This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.	



PCICMD_0_2_0_PCI - PCI Command		
	0	I/O Access Enable Default Value: 0b Access: R/W This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable. This field is RO 1'b0 if DEV2CTL[0] IOBARDIS at offset 0x58 is 1b.



PCI Express Capability

PCIECAP_0_2_0_PCI - PCI Express Capability			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000092		
Size (in bits):	16		
Address:	00072h		
PCI Express Capability			
DWord	Bit	Description	
0	15:14	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	13:9	Interrupt Message Number	
		Default Value:	00000b
		Access:	RO
		This field indicates which MSI vector is used for the interrupt message generated in association with any of the status bits of this Capability structure. Since this device only supports one MSI vector, this field is hardwired to 0.	
	8	Slot Implemented	
		Default Value:	0b
		Access:	RO
		This field is hardwired to 0 for an endpoint device.	
	7:4	Device Type	
		Default Value:	1001b
		Access:	RO
		This field is hardwired to 9h to indicate a Root Complex Integrated Endpoint.	
	3:0	Capability Version	
		Default Value:	0010b
		Access:	RO
		This field is hardwired to 2h to indicate Functions compliant to PCI Express 3.0 Base Specification.	



PCI Express Capability Header

PCIECAPHDR_0_2_0_PCI - PCI Express Capability Header		
Register Space: PCI: 0/2/0		
Source: BSpec		
Default Value: 0x0000AC10		
Size (in bits): 16		
Address: 00070h		
PCI Express Capability Header		
DWord	Bit	Description
0	15:8	Next Capability Pointer
		Default Value: 10101100b
		Access: RO
		This field is hardwired to point to the next PCI Capability structure, the MSI Capabilities at ACh.
	7:0	Capability Identifier
		Default Value: 00010000b
		Access: RO
		This field is hardwired to 10h to indicate that this is a PCI Express Capability structure.



PCI Express Capability Structure

DEVICESTS_0_2_0_PCI - PCI Express Capability Structure			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	16		
Address:	0007Ah		
PCI Express Capability Structure			
DWord	Bit	Description	
0	15:6	RESERVED	
		Default Value:	0000000000b
		Access:	RO
		Reserved	
	5	Transactions Pending	
		Default Value:	0b
		Access:	RO
		When Set, this bit indicates that the Function has issued Non-Posted Requests that have not been completed. A Function reports this bit is cleared only when all outstanding Non-Posted Requests have completed or have been terminated by the Completion Timeout mechanism. This bit must also be cleared upon the completion of an FLR.	
	4	Aux Power Detected	
		Default Value:	0b
		Access:	RO
		Functions that require Aux power report this bit as Set if Aux power is detected by the Function. Hardwired to 0b, the integrated graphics device does not require Aux power.	
	3	Unsupported Request Detected	
		Default Value:	0b
		Access:	RO
		This bit indicates the Function received an Unsupported Request. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.	
	2	Fatal Error Detected	
		Default Value:	0b
		Access:	RO

**DEVICESTS_0_2_0_PCI - PCI Express Capability Structure**

		This bit indicates the status of Fatal errors detected. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.	
	1	Non-Fatal Error Detected	
		Default Value:	0b
		Access:	RO
		This bit indicates the status of Non-Fatal errors detected. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.	
	0	Correctable Error Detected	
		Default Value:	0b
		Access:	RO
		This bit indicates the status of Correctable errors detected. Hardwired to 0b, the Root Complex Integrated Endpoint graphics device does not use the PCI Express error reporting mechanism.	



PCI Express Device Control

DEVICECTL_0_2_0_PCI - PCI Express Device Control			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	16		
Address:	00078h		
PCI Express Device Control			
DWord	Bit	Description	
0	15	Initiate Function Level Reset	
		Default Value:	0b
		Access:	R/W
		A write of 1b initiates Function Level Reset to the Function. During FLR, a read will return 1b since device 2 reads abort. If a local panel is powered on and configured to power down on reset, the FLR will typically take several hundred milliseconds to complete. The worst possible, although unrealistic, delay is 5 seconds.	
	14:12	Max Read Request Size	
		Default Value:	000b
		Access:	RO
		Functions that do not generate Read Requests larger than 128 bytes and Functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b.	
	11	Enable No Snoop	
		Default Value:	0b
		Access:	RO
		This bit is permitted to be hardwired to 0b if a Function would never Set the No Snoop attribute in transactions it initiates. The graphics device never generates a PCI Express TLP.	
	10	Aux Power PM Enable	
		Default Value:	0b
		Access:	RO
		Functions that do not implement this capability hardwire this bit to 0b.	

**DEVICECTL_0_2_0_PCI - PCI Express Device Control**

	9	Phantom Functions Enable	
		Default Value:	0b
		Access:	RO
	Functions that do not implement this capability hardwire this bit to 0b.		
	8	Extended Tag field Enable	
		Default Value:	0b
		Access:	RO
	Functions that do not implement this capability hardwire this bit to 0b.		
	7:5	Max Payload Size	
		Default Value:	000b
		Access:	RO
	Functions that support only the 128-byte max payload size are permitted to hardwire this field to 000b.		
	4	Enable Relaxed Ordering	
		Default Value:	0b
		Access:	RO
	A Function is permitted to hardwire this bit to 0b if it never sets the Relaxed Ordering attribute in transactions it initiates as a Requester. The graphics device never generates a PCI Express TLP.		
	3	Unsupported Request Response Enable	
		Default Value:	0b
		Access:	RO
	A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.		
	2	Fatal Error Enable	
		Default Value:	0b
		Access:	RO
	A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.		
	1	Non-Fatal Error Enable	
		Default Value:	0b
		Access:	RO
	A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.		



DEVICECTL_0_2_0_PCI - PCI Express Device Control			
	0	Correctable Error Enable	
		Default Value:	0b
		Access:	RO
		A Root Complex Integrated Endpoint that is not associated with a Root Complex Event Collector is permitted to hardwire this bit to 0b.	



PCI Mirror of GMCH Graphics Control

MGGC0_0_2_0_PCI - PCI Mirror of GMCH Graphics Control			
Register Space:		PCI: 0/2/0	
Source:		BSpec	
Default Value:		0x00000500	
Size (in bits):		16	
Address:		00050h	
Mirror of GGC_0_0_0_PCI.			
DWord	Bit	Description	
0	15:8	Graphics Mode Select	
		Default Value:	00000101b
		Access:	RO Variant
		This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. Hardware does not clear or set any of these bits automatically based on IGD being disabled/enabled. BIOS Requirement: BIOS must not set this field to 0h if IVD (bit 1 of this register) is 0. BIOS Requirement: Given new sizes allow down to 8MB allocation, BIOS has to ensure there is sufficient space for WOPCM and basic GFX Stolen functions. 00h:0MB 01h:32MB 02h:64MB 03h:96MB 04h:128MB 05h:160MB (default) 06h:192MB 07h:224MB 08h:256MB 09h:288MB 0Ah:320MB 0Bh:352MB 0Ch:384MB 0Dh:416MB 0Eh:448MB 0Fh:480MB 10h:512MB 11h - 1Fh: Reserved 20h:1024MB 21h - 2Fh: Reserved 30h:1536MB 31h - 3Fh: Reserved 40h: 2048MB	



MGGC0_0_2_0_PCI - PCI Mirror of GMCH Graphics Control

	41h - EFh: Reserved F0h: 4MB F1h: 8MB F2h: 12MB F3h: 16MB F4h: 20MB F5h: 24MB F6h: 28MB F7h: 32MB F8h: 36MB F9h: 40MB FAh: 44MB FBh: 48MB FCh: 52MB FDh: 56MB FEh: 60MB FFh: Reserved Hardware functionality in case of programming this value to Reserved is not guaranteed.															
7:6	GTT Graphics Memory Size Access:RO Variant This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics Translation Table. The BIOS ensures that memory is pre-allocated only when Internal graphics is enabled. GSM is assumed to be a contiguous physical DRAM space with DSM, and BIOS needs to allocate a contiguous memory chunk. Hardware will derive the base of GSM from DSM only using the GSM size programmed in the register. Hardware functionality in case of programming this value to Reserved is not guaranteed. 0x0: No Preallocated Memory 0x1: 2MB of Preallocated Memory 0x2: 4MB of Preallocated Memory 0x3: 8MB of Preallocated Memory <table><thead><tr><th>Value</th><th>Name</th><th>Description</th></tr></thead><tbody><tr><td>00b</td><td>[Default]</td><td>No Preallocated Memory</td></tr><tr><td>01b</td><td></td><td>2MB of Preallocated Memory</td></tr><tr><td>10b</td><td></td><td>4MB of Preallocated Memory</td></tr><tr><td>11b</td><td></td><td>8MB of Preallocated Memory</td></tr></tbody></table>	Value	Name	Description	00b	[Default]	No Preallocated Memory	01b		2MB of Preallocated Memory	10b		4MB of Preallocated Memory	11b		8MB of Preallocated Memory
Value	Name	Description														
00b	[Default]	No Preallocated Memory														
01b		2MB of Preallocated Memory														
10b		4MB of Preallocated Memory														
11b		8MB of Preallocated Memory														
5:3	RESERVED Default Value:000b Access:RO Reserved															
2	Versatile Acceleration Mode Enable															

**MGGC0_0_2_0_PCI - PCI Mirror of GMCH Graphics Control**

		Default Value:	0b
		Access:	RO Variant
	Enables the use of the iGFX engines for Versatile Acceleration. 1 - iGFX engines are in Versatile Acceleration Mode. Device 2 Class Code is 048000h. 0 - iGFX engines are in iGFX Mode. Device 2 Class Code is 030000h.		
	1	IGD VGA Disable	
		Default Value:	0b
		Access:	RO Variant
	0: Enable. Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. 1: Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub- Class Code field within Device 2 function 0 Class Code register is 80. BIOS Requirement: BIOS must not set this bit to 0 if the GMS field pre-allocates no memory. This bit MUST be set to 1 if Device 2 is disabled either via a fuse or fuse override (CAPID0_A[IGD] = 1) or via a register (DEVEN[3] = 0).		
	0	GGC Lock	
		Default Value:	0b
		Access:	RO Variant
		Description	
		When set to 1b, this bit will lock all bits in this register.	



PCI Status

PCISTS2_0_2_0_PCI - PCI Status			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000010		
Size (in bits):	16		
Address:	00006h		
PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.			
DWord	Bit	Description	
0	15	Detected Parity Error	
		Default Value:	0b
		Access:	RO
		Since the IGD does not detect parity, this bit is always hardwired to 0.	
	14	Signaled System Error	
		Default Value:	0b
		Access:	RO
		The IGD never asserts SERR#, therefore this bit is hardwired to 0.	
	13	Received Master Abort Status	
		Default Value:	0b
		Access:	RO
		The IGD never gets a Master Abort, therefore this bit is hardwired to 0.	
	12	Received Target Abort Status	
		Default Value:	0b
		Access:	RO
		The IGD never gets a Target Abort, therefore this bit is hardwired to 0.	
	11	Signaled Target Abort Status	
		Default Value:	0b
		Access:	RO
Hardwired to 0. The IGD does not use target abort semantics.			
10:9	DEVSEL Timing		
	Default Value:	00b	
	Access:	RO	

**PCISTS2_0_2_0_PCI - PCI Status**

PCISTS2_0_2_0_PCI - PCI Status			
		Hardwired to 00.	
	8	Master Data Parity Error Detected	
		Default Value:	0b
		Access:	RO
		Since Parity Error Response is hardwired to disabled, and the IGD does not do any parity detection, this bit is hardwired to 0.	
	7	Fast Back-to-Back	
		Default Value:	0b
		Access:	RO
		Hardwired to 0 to be compliant to PCI Express Base Spec (rev 3.0).	
	6	User Defined Format	
		Default Value:	0b
		Access:	RO
		Hardwired to 0.	
	5	66 MHz PCI Capable	
		Default Value:	0b
		Access:	RO
		Hardwired to 0.	
	4	Capability List	
Default Value:		1b	
Access:		RO	
This bit is hardwired to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.			
3	Interrupt Status		
	Default Value:	0b	
	Access:	RO Variant	
	This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted.		
2:0	RESERVED		
	Default Value:	000b	
	Access:	RO	
	Reserved		



PCU Interrupt Definition

PCU Interrupt Definition		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	444E0h-444EFh	
Name:	PCU Interrupts	
ShortName:	PCU_INTERRUPT	
Power:	PG0	
Reset:	soft	
This table indicates which events are mapped to each bit of the PCU Interrupt registers. 0x444E0 = ISR 0x444E4 = IMR 0x444E8 = IIR 0x444EC = IER		
DWord	Bit	Description
0	31	DDIA DC9 HPD This field indicates DDIA hotplug activity was detected during DC9.
	30	DDIB DC9 HPD This field indicates DDIB hotplug activity was detected during DC9.
	29	DDIC DC9 HPD This field indicates DDIC hotplug activity was detected during DC9.
	28:26	Unused_Int_28_26 These interrupts are currently unused.
	25	PCU_Pcode2driver_Mailbox_Event
	24	PCU_Thermal_Event
	23:0	Unused_Int_23_0 These interrupts are currently unused.



PHY_CTL_DDI

PHY_CTL_DDI		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	64C00h-64C03h	
Name:	PHY_CTL_DDI_A	
ShortName:	PHY_CTL_DDI_A	
Power:	PG0	
Reset:	global	
Address:	64C10h-64C13h	
Name:	PHY_CTL_DDI_B	
ShortName:	PHY_CTL_DDI_B	
Power:	PG0	
Reset:	global	
Address:	64C20h-64C23h	
Name:	PHY_CTL_DDI_C	
ShortName:	PHY_CTL_DDI_C	
Power:	PG0	
Reset:	global	
This register is on the ungated clock and the chip reset, not the FLR. Writes to this register will not trigger PSR exit.		
DWord	Bit	Description
0	31:30	Reserved
	29:28	Reserved
	27:26	Reserved
	25:24	Reserved
	23:22	Reserved
	21:20	Reserved
	19:18	Reserved
	17:16	Reserved
	15	Spare 15
14	Spare 14	



PHY_CTL_DDI								
	13	Spare 13						
	12	Spare 12						
	11	Spare 11						
	10	Common Lane Powerdown Acknowledge						
	Access: RO							
	9	Lane Powerdown Acknowledge						
	Access: RO							
	8	Lane Status						
	Access: RO							
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Disable</td></tr><tr><td>1b</td><td>Enable</td></tr></table>		Value	Name	0b	Disable	1b	Enable
	Value	Name						
	0b	Disable						
1b	Enable							
7	Spare 7							
6	Spare 6							
5	Spare 5							
4	Reserved							
3:0	Reserved							



PHY_CTL_FAMILY

PHY_CTL_FAMILY								
Register Space:	MMIO: 0/2/0							
Source:	BSpec							
Default Value:	0x00000000							
Access:	R/W							
Size (in bits):	32							
Address:	64C80h-64C83h							
Name:	PHY_CTL_FAMILY_EDP							
ShortName:	PHY_CTL_FAMILY_EDP							
Power:	PG0							
Reset:	global							
Address:	64C90h-64C93h							
Name:	PHY_CTL_FAMILY_DDI							
ShortName:	PHY_CTL_FAMILY_DDI							
Power:	PG0							
Reset:	global							
This register is on the ungated clock and the chip reset, not the FLR. Writes to this register will not trigger PSR exit.								
DWord	Bit	Description						
0	31	Common Reset This field controls the reset_b (active low reset) which enables the PHY.						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Disable</td></tr><tr><td>1b</td><td>Enable</td></tr></table>	Value	Name	0b	Disable	1b	Enable
		Value	Name					
		0b	Disable					
	1b	Enable						
	30	Powergood Access: RO This field indicates that the PHY is powered up.						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Not good</td></tr><tr><td>1b</td><td>Good</td></tr></table>	Value	Name	0b	Not good	1b	Good
		Value	Name					
		0b	Not good					
		1b	Good					
	29	Spare 29						
	28	Spare 28						
	27	Spare 27						
	26	Spare 26						
25	Spare 25							



PHY_CTL_FAMILY		
	24	Spare 24
	23	Spare 23
	22	Spare 22
	21	Spare 21
	20	Spare 20
	19	Spare 19
	18	Spare 18
	17	Spare 17
	16	Spare 16
	15	Spare 15
	14	Spare 14
	13	Spare 13
	12	Spare 12
	11	Spare 11
	10	Spare 10
	9	Spare 9
	8	Spare 8
	7	Spare 7
	6	Spare 6
	5:4	Reserved
	3:0	Reserved



PIPE_SCANLINE

PIPE_SCANLINE			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000000	
Access:		RO	
Size (in bits):		32	
This register enables the read back of the pipe vertical line counter. The value increments at the leading edge of HSYNC. The value resets to line zero at the first active line of the display. In interlaced display timings, the scan line counter provides the current line in the field. One field can have a total number of lines that is one greater than the other field.			
Restriction			
Restriction : Not supported with MIPI DSI.			
DWord	Bit	Description	
0	31	Current Field	
		This is an indication of the current display field.	
		Value	Name
		Description	
	0b	Odd	First field (odd field)
1b	Even	Second field (even field)	
30:13	Reserved		
12:0	Line Counter for Display		
	This is an indication of the current display scan line.		
	Programming Notes		
The line count value is from the display output timing generator, representing the scan line currently being output to a receiver.			
Due to buffering within the display engine, the line being fetched (read) from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line.			



PIPE_SCANLINECOMP

PIPE_SCANLINECOMP								
Register Space:	MMIO: 0/2/0							
Source:	BSpec							
Default Value:	0x00000000							
Access:	R/W							
Size (in bits):	32							
This register is used to initiate a display scan line compare. This MMIO driven scan line compare can not be used at the same time as the command streamer driven scan line compare on the same pipe. When this register is written with the Initiate Compare bit set to 1b, the Display Engine (DE) will start comparing the display pipe or plane (selectable) current scan line value (current scan line) with the start scan line value (current scan line >= start scan line) and the end scan line value (current scan line <= end scan line) to decide if the pipe scan line is inside or outside the scan line window of interest. DE will wait until the current scan line is either outside (Inclusive mode) or inside (Exclusive mode) the scan line window, then trigger a scan line event and stop any further comparing. The scan line event can cause display to send a scan line compare response to the command streamer, (used for releasing a MI_WAIT_FOR_EVENT on scan line window), if unmasked in the DERRMR mask register 0x44050. The scan line event can also cause display to generate a scan line compare interrupt, if the interrupt registers are configured for that. The value programmed should be the desired value - 1, so for scan line 0, the value programmed is vertical total, and for scan line 1, the value programmed is 0. The programmable range can include the vertical blank. In interlaced display timings, the current scan line is the current line of the current interlaced field. Either MMIO or a MI_LOAD_REGISTER_IMM command can be used to unmask the scan line render response 0x44050. That can be done anytime before programming this register. There is one instance of this register per pipe.								
Restriction								
Restriction : A new scan line compare must not be started until after the previous compare has finished. The end scan line value must be greater than or equal to the start scan line value. When using LRI care must be taken to follow all the programming rules for LRI targetting the display engine.								
Restriction : Not supported with MIPI DSI.								
DWord	Bit	Description						
0	31	Initiate Compare This field initiates the scan line compare. When this register is written with this bit set to 1b, the display engine will do one complete comparison cycle, trigger a scan line event, then stop comparing. <table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Do nothing</td></tr><tr><td>1b</td><td>Initiate compare</td></tr></table>	Value	Name	0b	Do nothing	1b	Initiate compare
Value	Name							
0b	Do nothing							
1b	Initiate compare							
Restriction								
Restriction : Do not write this register again until after any previous scan line compare has completed.								

PIPE_SCANLINECOMP												
	30	Inclusive Exclusive Select This field selects whether the scan line compare is done in inclusive mode, where display triggers the scan line event when outside the scan line window, or inclusive mode, where display triggers when inside the window.										
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0b</td><td>Exclusive</td><td>Exclusive mode: trigger scan line event when inside the scan line window</td></tr><tr><td>1b</td><td>Inclusive</td><td>Inclusive mode: trigger scan line event when outside the scan line window</td></tr></table>	Value	Name	Description	0b	Exclusive	Exclusive mode: trigger scan line event when inside the scan line window	1b	Inclusive	Inclusive mode: trigger scan line event when outside the scan line window	
	Value	Name	Description									
	0b	Exclusive	Exclusive mode: trigger scan line event when inside the scan line window									
1b	Inclusive	Inclusive mode: trigger scan line event when outside the scan line window										
29	Counter Select This field selects whether the scan line compare is done using the pipe timing generator scanline counter or a plane scanline counter. The pipe timing generator counts the scanlines being output from display. The plane counts the scan lines being fetched from the frame buffer.											
	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0b</td><td>Timing generator</td><td>Use the scanline count from the pipe timing generator</td></tr><tr><td>1b</td><td>Plane 1</td><td>Use the scanline count from plane 1</td></tr></table>	Value	Name	Description	0b	Timing generator	Use the scanline count from the pipe timing generator	1b	Plane 1	Use the scanline count from plane 1		
Value	Name	Description										
0b	Timing generator	Use the scanline count from the pipe timing generator										
1b	Plane 1	Use the scanline count from plane 1										
	<table><tr><th colspan="3">Programming Notes</th></tr><tr><td colspan="3">Due to buffering within the display engine, the line being fetched from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line. The plane scan line count more closely represents what data is currently being fetched by the plane.</td></tr></table>		Programming Notes			Due to buffering within the display engine, the line being fetched from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line. The plane scan line count more closely represents what data is currently being fetched by the plane.						
Programming Notes												
Due to buffering within the display engine, the line being fetched from the frame buffer is not directly linked to the line being output. It is possible for the fetched line to be hundreds of lines ahead of the timing generator output line. The plane scan line count more closely represents what data is currently being fetched by the plane.												
28:16	Start Scan Line This field specifies the starting scan line number of the scan line window.											
15	Render Response Destination This bit indicates what destination to send the scan line event render response to.											
	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0b</td><td>CS</td><td>Send scan line event response to CS</td></tr><tr><td>1b</td><td>BCS</td><td>Send scan line event response to BCS</td></tr></table>	Value	Name	Description	0b	CS	Send scan line event response to CS	1b	BCS	Send scan line event response to BCS		
Value	Name	Description										
0b	CS	Send scan line event response to CS										
1b	BCS	Send scan line event response to BCS										
14:13	Reserved											
12:0	End Scan Line This field specifies the ending scan line number of the scan line window.											



PLANE_AUX_DIST

PLANE_AUX_DIST		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer	Start of vertical blank or pipe not enabled; after armed	
Update Point:		
Double Buffer Armed Write to PLANE_SURF or plane not enabled		
By:		
This register is used to specify the distance from the main surface base address and the stride of the auxiliary surface.		
Unlike the surface base address, this register value cannot be updated through flips.		
DWord	Bit	Description
0	31:12	Auxiliary Surface Distance
		Description
		This offset specifies the distance (in multiple of 4K bytes) of the Auxiliary surface from the main surface. When using YUV planar formats this field represents the distance of UV surface. When using compressed surface this field represents the distance of control surface. In the graphics address space, the auxiliary surface should always be allocated after the main surface, and the programmed auxiliary surface distance must not be negative.
		Restriction
	It must be 4K page aligned. Allocate an extra 136 Page Table Entries (PTEs) beyond the end of the displayed surface. If 180 or 270 plane rotation capability is required, allocate an extra 136 PTEs before the beginning of the surface. When address range limits are reached, wrap around to finish allocating the extra PTEs. Only the PTEs will be used, not the pages themselves. The end of the surface cannot be within 136 PTEs of the end of the graphics memory.	
	11:10	Reserved
9:0	Auxiliary Surface Stride	
	Description	
	This field specifies the stride of the auxiliary surface. Refer to PLANE_STRIDE register for stride programming details. When using YUV planar formats this field represents the stride of UV surface. When using compressed surface this field represents the stride of the control surface.	
		Restriction : When using render compressed surfaces, the programmed auxiliary surface stride should not exceed 8 (8 * 128 = 1024 bytes).



PLANE_KEYMAX

PLANE_KEYMAX		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer	Start of vertical blank, pipe not enabled, or plane not enabled	
Update Point:		
When plane source is YUV, this register specifies the maximum YUV key value to be used together with the minimum YUV key value and the channel enables to determine if the plane matches the key. When plane source is RGB, this register is not used.		
DWord	Bit	Description
0	31:24	Plane Alpha Value Specifies the plane alpha value when plane alpha is enabled in PLANE_KEYMSK register.
	23:16	V Key Max Value Specifies the maximum key value for the V channel.
	15:8	Y Key Max Value Specifies the maximum key value for the Y channel.
	7:0	U Key Max Value Specifies the maximum key value for the U channel.



PLANE_KEYMSK

PLANE_KEYMSK				
Register Space:	MMIO: 0/2/0			
Source:	BSpec			
Default Value:	0x00000000			
Access:	Double Buffered			
Size (in bits):	32			
Double Buffer	Start of vertical blank, pipe not enabled, or plane not enabled			
Update Point:				
DWord	Bit	Description		
0	31	Plane Alpha Enable		
		Description		
		Enables the plane alpha. Color channels will be pre-multiplied by hardware with the plane alpha value from PLANE_KEYMAX register. Per-pixel alpha is defined in the PLANE_CTL register.		
		Value	Name	
		0b	Disable	
	30:27		1b	Enable
			Reserved	
			Format:	MBZ
	26		V or R Key Channel Enable	
			Enables the V/Red channel for key comparison. A disabled channel will be ignored when determining a key match.	
			Value	Name
			0b	Disable
			1b	Enable
	25		Y or G Key Channel Enable	
			Enables the Y/Green channel for key comparison. A disabled channel will be ignored when determining a key match.	
			Value	Name
			0b	Disable
			1b	Enable
24		U or B Key Channel Enable		
		Enables the U/Blue channel for key comparison. A disabled channel will be ignored when determining a key match.		
		Value	Name	
		0b	Disable	
		1b	Enable	



PLANE_KEYMSK		
	23:16	R Key Mask Value Specifies the key mask for the Red channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.
	15:8	G Key Mask Value Specifies the key mask for the Green channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.
	7:0	B Key Mask Value Specifies the key mask for the Blue channel. A zero bit in the mask indicates that the corresponding bit will be ignored when determining a key match.



PLANE_KEYVAL

PLANE_KEYVAL		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer	Start of vertical blank, pipe not enabled, or plane not enabled	
Update Point:		
When plane source is YUV, this register specifies the minimum YUV key value to be used together with the maximum YUV key value and the channel enables to determine if the plane matches the key. When plane source is RGB, this register specifies the RGB key value to be used together with the channel masks to determine if the plane matches the key. RGB key matches can only occur for positive pixel values in the 0 to 1 range. Extended range pixel values will not match. MSB bits are used for comparison.		
DWord	Bit	Description
0	31:24	Reserved
		Format: MBZ
	23:16	V Min or R Key Value Specifies the minimum key value for the V channel or the compare value for Red channel.
	15:8	Y Min or G Key Value Specifies the minimum key value for the Y channel or the compare value for Green channel.
	7:0	U Min or B Key Value Specifies the minimum key value for the U channel or the compare value for Blue channel.



PLANE_LEFT_SURF

PLANE_LEFT_SURF			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	Double Buffered		
Size (in bits):	32		
Double Buffer	Start of left or right eye vertical blank (selectable), pipe not enabled. or plane not enabled;		
Update Point:	after armed		
Double Buffer Armed	Write to PLANE_SURF or plane not enabled		
By:			
Restriction			
Restriction : This register must be programmed with a valid address prior to enabling stereo 3D on this pipe.			
DWord	Bit	Description	
0	31:12	Left Surface Base Address	
		Format:	GraphicsAddress[31:12]
		This address specifies the stereo 3D left eye surface base address bits 31:12.	
		Restriction	
	Restriction : This surface must have the same stride, tiling, and panning offset parameters as the right eye surface and meet all the same restrictions.		
	11:0	Reserved	



PLANE_OFFSET

PLANE_OFFSET						
Register Space:	MMIO: 0/2/0					
Source:	BSpec					
Default Value:	0x00000000					
Access:	Double Buffered					
Size (in bits):	32					
Double Buffer	Start of vertical blank, pipe not enabled, or plane not enabled					
Update Point:						
This register specifies the panning for the plane surface. The start position is specified in this register as a (x, y) offset from the beginning of the surface. When performing 180 rotation, hardware will internally add the plane size to the offsets so the plane will start displaying from the bottom right corner of the image. When performing 90 rotation, the offset programmed should take the rotation in to consideration. X offset = (Surface height in tiles * tile height) - Y offset - Y Size, Y offset = X offset When performing 270 rotation, use the same programming as 90 rotation. For YUV planar format non-rotate cases, the UV surface offsets should be half of the Y surface offsets when the UV surface is tile row aligned. When the UV surface is not tile row aligned, the UV surface Y offset should also include the lines from the previous nearest tile row aligned address.						
Restriction						
Restriction : The plane size + offset must not exceed the maximum supported plane size.						
DWord	Bit	Description				
0	31:29	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ		
	Format:	MBZ				
	28:16	Start Y Position The Start Y Position or the Y Offset is the vertical offset in lines of the beginning of the active display plane relative to the display surface. <table><tr><td colspan="2">Restriction</td></tr><tr><td colspan="2">Restriction : In 90/270 rotation modes, this offset must be even lines aligned for YUV 4:2:2, YUV 4:2:0 formats.</td></tr></table>	Restriction		Restriction : In 90/270 rotation modes, this offset must be even lines aligned for YUV 4:2:2, YUV 4:2:0 formats.	
	Restriction					
	Restriction : In 90/270 rotation modes, this offset must be even lines aligned for YUV 4:2:2, YUV 4:2:0 formats.					
15:13	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ			
Format:	MBZ					
12:0	Start X Position The Start X Position or the X Offset is the horizontal offset in pixels of the beginning of the active display plane relative to the display surface. <table><tr><td colspan="2">Restriction</td></tr><tr><td colspan="2">Restriction : In 0/180 rotation modes, this offset must be even pixel aligned for YUV 4:2:2, YUV 4:2:0 formats.</td></tr></table>	Restriction		Restriction : In 0/180 rotation modes, this offset must be even pixel aligned for YUV 4:2:2, YUV 4:2:0 formats.		
Restriction						
Restriction : In 0/180 rotation modes, this offset must be even pixel aligned for YUV 4:2:2, YUV 4:2:0 formats.						



PLANE_POS

PLANE_POS		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer	Start of vertical blank or pipe not enabled; after armed	
Update Point:		
Double Buffer Armed Write to PLANE_SURF or plane not enabled		
By:		
This register specifies the screen position of the plane. The origin of the plane position is always the upper left corner of the display pipe source image area. When plane scaling is not enabled on this plane, this is the position of the plane when blended with other planes on this pipe. When plane scaling is enabled on this plane, the scaler window position is the position of the plane when blended with other planes on this pipe. When performing rotation, the plane image is rotated by hardware, but the position is not, so it must be adjusted if it is desired to maintain the same apparent position on a physically rotated display.		
Restriction		
Restriction : When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size >= plane position + plane size.		
When plane scaling is enabled on this plane, the X and Y positions must be programmed to 0.		
DWord	Bit	Description
0	31:28	Reserved Format: MBZ
	27:16	Y Position This specifies the vertical position of the plane upper left corner in lines.
	15:13	Reserved Format: MBZ
	12:0	X Position This specifies the horizontal position of the plane upper left corner in pixels.



PLANE_SIZE

PLANE_SIZE		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer	Start of vertical blank or pipe not enabled; after armed	
Update Point:		
Double Buffer Armed Write to PLANE_SURF or plane not enabled		
By:		
This register specifies the plane source size, the size of the image fetched from the frame buffer. When plane scaling is not enabled on this plane, this is the size of the plane when blended with other planes on this pipe. When plane scaling is enabled on this plane, the scaler window size is the size of the plane when blended with other planes on this pipe.		
Restriction		
Restriction : When plane scaling is not enabled on this plane, the plane must be completely contained within the pipe source area. Pipe source size >= plane position + plane size.		
DWord	Bit	Description
0	31:28	Reserved
		Format: MBZ
	27:16	Height
		This specifies the height of the plane in lines. The value in the register is the height minus one.
		Restriction
Restriction : The height must be at least one line. The height is limited to maximum of 4096 lines. When plane scaling is enabled, the height must be atleast 8 lines.		
15:13	Reserved	
	Format: MBZ	
12:0	Width	
		This specifies the width of the plane in pixels. The value in the register is the width minus one.
		Restriction
Restriction : The width must be even (programmed value odd) when YUV 4:2:2 or YUV 4:2:0 source pixel format is used. The width must be at least one pixel. The width should be less than or equal to the stride in pixels.		

**PLANE_SIZE**

PLANE_SIZE				
		Tiling format	Bytes per pixel	Max Width supported in pixels (with no horizontal panning)
		Linear, X Tiling	1,2,4,8	4096
		Y Tiling	8	2048
			1,2,4	4096
		Yf Tiling	8	Not supported
			1,2,4	4096



PLANE_STRIDE

PLANE_STRIDE															
Register Space:	MMIO: 0/2/0														
Source:	BSpec														
Default Value:	0x00000000														
Access:	Double Buffered														
Size (in bits):	32														
Double Buffer	Start of vertical blank or pipe not enabled; after armed														
Update Point:															
Double Buffer Armed Write to PLANE_SURF or plane not enabled															
By:															
DWord	Bit	Description													
0	31:10	Reserved													
	9:0	Stride This field specifies the stride for the plane. The field is used to determine the line to line increment for the plane. For Linear memory, this field specifies the stride in chunks of 64 bytes (1 cache line). If the programmed value is 100, the actual stride = 100 * 64 = 6400 bytes. For X-Tiled & Y-Tiled memory, this field specifies the stride in number of tiles. For Tile X, if the programmed value is 10, the actual stride = 10 * 512 (X tile width) = 5120 bytes. For Tile Y legacy, if the programmed value is 10, the actual stride = 10 * 128 (Y tile width) = 1280 bytes. This register may be updated through MMIO writes or through command streamer initiated synchronous flips. <table><tr><th>Tile Format</th><th>Width in bytes</th></tr><tr><td>Tile X</td><td>512</td></tr><tr><td>Tile Y (legacy)</td><td>128</td></tr><tr><td>Tile YF (8 bpp)</td><td>64</td></tr><tr><td>Tile YF (16 bpp, 32 bpp, 64 bpp)</td><td>128</td></tr></table> <table><tr><th>Programming Notes</th></tr><tr><td>For YUV planar (NV12 or P0xx) source fomats, the Auxiliary surface (UV surface) stride should be programmed seperately in the PLANE_AUX_DIST register.</td></tr></table> <table><tr><th>Restriction</th></tr><tr><td>Restriction : For YUV planar (NV12 or P0xx) plane pixel formats, the stride calculated in bytes should be equal for the Y and UV surfaces. In Tile Yf format, the stride value programmed for YUV planar - Y surface should be an even number of tiles in the non-rotate mode. The stride in bytes must not exceed the of the size of 8K pixels and 32K bytes</td></tr></table>	Tile Format	Width in bytes	Tile X	512	Tile Y (legacy)	128	Tile YF (8 bpp)	64	Tile YF (16 bpp, 32 bpp, 64 bpp)	128	Programming Notes	For YUV planar (NV12 or P0xx) source fomats, the Auxiliary surface (UV surface) stride should be programmed seperately in the PLANE_AUX_DIST register.	Restriction
Tile Format	Width in bytes														
Tile X	512														
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Tile YF (8 bpp)	64														
Tile YF (16 bpp, 32 bpp, 64 bpp)	128														
Programming Notes															
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PLANE_STRIDE						
		Tile Format	Pixel Format	Maximum Stride	YUV Planar Maximum Auxiliary surface stride in tiles	Render Decompression Maximum Auxiliary surface stride in tiles
		Linear Stride in cache-lines	64 bpp pixel format	512	NA	NA
			32 bpp pixel format	512	NA	NA
			16 bpp pixel format	256	NA	NA
			8 bpp pixel format	128	128	NA
		X Tiling Stride in tiles	64 bpp pixel format	64	NA	NA
			32 bpp pixel format	64	NA	NA
			16 bpp pixel format	32	NA	NA
			8 bpp pixel format	16	16	NA
		Y Tiling (Legacy) Stride in tiles	64 bpp pixel format	256	NA	NA
			32 bpp pixel format	256	NA	8
			16 bpp pixel format	128	NA	NA
			8 bpp pixel format	64	64	NA
		YF Tiling Stride in	32 bpp pixel	256	NA	8



PLANE_STRIDE				
		tiles	format	
			16 bpp Pixel format	128 NA NA
			8 bpp pixel format	128 64 NA



PLANE_SURF

PLANE_SURF			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	Double Buffered		
Size (in bits):	32		
Double Buffer	Start of left or right eye vertical blank (selectable), pipe not enabled, or plane not enabled		
Update Point:			
Writes to this register arm primary registers for this pipe. A write to this register is considered a flip and can cause a flip done interrupt if the interrupt registers are configured for that. The values in this register may be updated through MMIO writes or through command streamer initiated flips. Synchronous updates (synchronous command streamer flips or synchronous MMIO writes) will update the plane surface values at the start of the next vertical blank. Asynchronous updates (asynchronous command streamer flips or asynchronous MMIO writes) will update the plane surface values at the next TLB request or at the start of the next vertical blank. Stereo 3D synchronous updates (stereo 3D command streamer flips or synchronous MMIO writes while stereo 3D is enabled) will update at the start of either the left or right eye vertical blank, selectable by the plane control register stereo surface vblank mask. Asynchronous flip completion time depends greatly on how much data has been prefetched for power savings, and can take up to 1 full frame to complete. For faster flip completion, disable FBC and render compression and allocate a small amount of data buffer for the plane.			
DWord	Bit	Description	
0	31:12	Surface Base Address	
		Format:	GraphicsAddress[31:12]
		This address specifies the surface base address bits 31:12. In stereo 3D mode this is the right eye base address. In non-stereo 3D mode this is the only base address. It represents an offset from the graphics memory aperture base and is mapped to physical pages through the global GTT.	
		Restriction	
	The surface base address must be at least 256KB aligned in the Linear or X-tiling modes and must be at least 1MB aligned in the Y-tiling mode. Allocate an extra 136 Page Table Entries (PTEs) beyond the end of the displayed surface. If 180 or 270 plane rotation capability is required, allocate an extra 136 PTEs before the begining of the surface. When address range limits are reached, wrap around to finish allocating the extra PTEs. Only the PTEs will be used, not the pages themselves. For render compression, the padding must be added for both the main surface and the compression control surface. There must be padding between the main and the control surfaces. For planar YUV 420 formats, the padding must be added for both Y and UV surfaces. There must be padding between the Y and UV surfaces.		
11	Reserved		
10	Reserved		



PLANE_SURF								
	9	Reserved						
	8:7	Reserved						
	6:4	Reserved						
	3	Ring Flip Source This bit indicates if the source of the last ring flip was CS or BCS. This will determine where the flip done response is sent. <table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>CS</td></tr><tr><td>1b</td><td>BCS</td></tr></table>	Value	Name	0b	CS	1b	BCS
	Value	Name						
	0b	CS						
	1b	BCS						
2	Reserved							
1:0	Reserved							



PLANE_SURFLIVE

PLANE_SURFLIVE		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
There is one instance of this register for each plane.		
DWord	Bit	Description
0	31:12	Live Surface Base Address
		Access: RO This gives the live value of the surface base address as being currently used for the plane.
	11	Reserved
		Format: MBZ
	10:9	Reserved
	8:6	Reserved
	5	Reserved
4	Reserved	
3:0	Reserved	
	Format: MBZ	



PLANE_WM

PLANE_WM	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00004007
Access:	Double Buffered
Size (in bits):	32
Double Buffer	Start of vertical blank, plane not enabled, or pipe not enabled
Update Point:	
Double Buffer Armed	Write to PLANE_SURF or plane not enabled
By:	
Address:	70140h-7015Fh
Name:	Cursor A Watermarks
ShortName:	CUR_WM_A_*
Power:	PG1
Reset:	soft
Address:	71140h-7115Fh
Name:	Cursor B Watermarks
ShortName:	CUR_WM_B_*
Power:	PG2
Reset:	soft
Address:	72140h-7215Fh
Name:	Cursor C Watermarks
ShortName:	CUR_WM_C_*
Power:	PG2
Reset:	soft
Address:	70240h-7025Fh
Name:	Plane 1 A Watermarks
ShortName:	PLANE_WM_1_A_*
Power:	PG1
Reset:	soft
Address:	70340h-7035Fh
Name:	Plane 2 A Watermarks
ShortName:	PLANE_WM_2_A_*
Power:	PG1
Reset:	soft



PLANE_WM	
Address:	70440h-7045Fh
Name:	Plane 3 A Watermarks
ShortName:	PLANE_WM_3_A_*
Power:	PG1
Reset:	soft
Address:	70540h-7055Fh
Name:	Plane 4 A Watermarks
ShortName:	PLANE_WM_4_A_*
Power:	PG1
Reset:	soft
Address:	71240h-7125Fh
Name:	Plane 1 B Watermarks
ShortName:	PLANE_WM_1_B_*
Power:	PG2
Reset:	soft
Address:	71340h-7135Fh
Name:	Plane 2 B Watermarks
ShortName:	PLANE_WM_2_B_*
Power:	PG2
Reset:	soft
Address:	71440h-7145Fh
Name:	Plane 3 B Watermarks
ShortName:	PLANE_WM_3_B_*
Power:	PG2
Reset:	soft
Address:	71540h-7155Fh
Name:	Plane 4 B Watermarks
ShortName:	PLANE_WM_4_B_*
Power:	PG2
Reset:	soft
Address:	72240h-7225Fh
Name:	Plane 1 C Watermarks
ShortName:	PLANE_WM_1_C_*
Power:	PG2
Reset:	soft



PLANE_WM

Address: 72340h-7235Fh
 Name: Plane 2 C Watermarks
 ShortName: PLANE_WM_2_C_*
 Power: PG2
 Reset: soft

Address: 72440h-7245Fh
 Name: Plane 3 C Watermarks
 ShortName: PLANE_WM_3_C_*
 Power: PG2
 Reset: soft

Programming Notes

There are eight regular watermarks and a transition watermark per plane/cursor. For YUV planar source formats, only the Y surface watermark value should be programmed. Watermark programming instructions are documented separately.

Restriction

Restriction : For minimum watermark requirements refer to Display Watermark Programming section.

DWord	Bit	Description	
0	31	Enable This field enables this watermark. All the watermarks at this level for all enabled planes must be enabled before the level will be used.	
		Value	Name
		1b	Enable
		0b	Disable
	30	Reserved	
	29:19	Reserved	
		Format:	MBZ
	18:14	Lines	
		Default Value:	01h
		Description	
This field contains the watermark value in lines. Hardware ignores the lines for the the transition watermark.			
Hardware ignores the lines for the level 0 watermark.			
13:10	Reserved		



PLANE_WM				
	9:0	Blocks		
		<table><tr><td>Default Value:</td><td>007h</td></tr></table>	Default Value:	007h
		Default Value:	007h	
This field contains the watermark value in blocks of 8 cachelines.				



PORT_CL1CM_DW0

PORT_CL1CM_DW0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000707	
Access:	R/W	
Size (in bits):	32	
Address:	162000h-162003h	
Name:	PORT_CL1CM_DW0_A	
ShortName:	PORT_CL1CM_DW0_A	
Power:	PG0	
Reset:	global	
Address:	6C000h-6C003h	
Name:	PORT_CL1CM_DW0_BC	
ShortName:	PORT_CL1CM_DW0_BC	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:20	Preserve Default 31 20
		Default Value: 000000000000b The values in this field must not be changed.
	19	ialdl_powerdown
		Access: RO status bit to indicate all data lanes are powered down
	18	ianydl_powerdown
		Access: RO status bit to indicate any data lane is powered down
	17	iphypwrgack
		Access: RO PHY power ack status
	16	iphypwrgood
		Access: RO PHY power good status



PORT_CL1CM_DW0		
	15:0	Preserve Default 15 0
		Default Value: 000001110000011b
		The values in this field must not be changed.
		Programming Notes
		Bit 7 is reserved and defaults to 0, but the DDI PHY Initialization sequence specifies a read to it as part of determining when this register is accessible.



PORT_CL1CM_DW9

PORT_CL1CM_DW9		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x80800080	
Access:	R/W	
Size (in bits):	32	
Address:	162024h-162027h	
Name:	PORT_CL1CM_DW9_A	
ShortName:	PORT_CL1CM_DW9_A	
Power:	PG0	
Reset:	global	
Address:	6C024h-6C027h	
Name:	PORT_CL1CM_DW9_BC	
ShortName:	PORT_CL1CM_DW9_BC	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:16	Preserve Default 31 16
		Default Value: 1000000010000000b The values in this field must not be changed.
	15:8	iref0rcoffset
	7:0	Preserve Default 7 0
		Default Value: 10000000b The values in this field must not be changed.



PORT_CL1CM_DW10

PORT_CL1CM_DW10		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x80800080	
Access:	R/W	
Size (in bits):	32	
Address:	162028h-16202Bh	
Name:	PORT_CL1CM_DW10_A	
ShortName:	PORT_CL1CM_DW10_A	
Power:	PG0	
Reset:	global	
Address:	6C028h-6C02Bh	
Name:	PORT_CL1CM_DW10_BC	
ShortName:	PORT_CL1CM_DW10_BC	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:16	Preserve Default 31 16
		Default Value: 1000000010000000b The values in this field must not be changed.
	15:8	iref1rcoffset
	7:0	Preserve Default 7 0
		Default Value: 10000000b The values in this field must not be changed.



PORT_CL1CM_DW28

PORT_CL1CM_DW28			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x330B0040		
Access:	R/W		
Size (in bits):	32		
Address:	162070h-162073h		
Name:	PORT_CL1CM_DW28_A		
ShortName:	PORT_CL1CM_DW28_A		
Power:	PG0		
Reset:	global		
Address:	6C070h-6C073h		
Name:	PORT_CL1CM_DW28_BC		
ShortName:	PORT_CL1CM_DW28_BC		
Power:	PG0		
Reset:	global		
DWord	Bit	Description	
0	31:24	Preserve Default 31 24	
		<table><tr><td>Default Value:</td><td>00110011b</td></tr></table> The values in this field must not be changed.	Default Value:
	Default Value:	00110011b	
	23	ocl1powerdownen Dynamic Power Down Enable for Channel 0	
	22	oldo_dynpwrdownen	
	21:7	Preserve Default 21 7	
<table><tr><td>Default Value:</td><td>0010110000000000b</td></tr></table> The values in this field must not be changed.		Default Value:	0010110000000000b
Default Value:	0010110000000000b		
6:2	susclkdisable_delay		
	<table><tr><td>Default Value:</td><td>10000b 16 Cycle Delay</td></tr></table> This register will control the number of cycles to delay the susclk enable de-assertion, in addition to the de-assertion of the CLKREQ signal sent to the SOC. The crclk enable must be continuously de-asserted for the duration of this delay in order for the de-asserted state to be captured by the clock gating controller. 5'b00000 – 0 Cycle Delay 5'b00001 – 1 Cycle Delay 5'b00010 – 2 Cycle Delay	Default Value:	10000b 16 Cycle Delay
Default Value:	10000b 16 Cycle Delay		



PORT_CL1CM_DW28		
		5'b11110 – 30 Cycle Delay 5'b11111 – 31 Cycle Delay
	1:0	sus_clk_config



PORT_CL1CM_DW30

PORT_CL1CM_DW30			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x3E000010		
Access:	RO		
Size (in bits):	32		
Address:	162078h-16207Bh		
Name:	PORT_CL1CM_DW30_A		
ShortName:	PORT_CL1CM_DW30_A		
Power:	PG0		
Reset:	global		
Address:	6C078h-6C07Bh		
Name:	PORT_CL1CM_DW30_BC		
ShortName:	PORT_CL1CM_DW30_BC		
Power:	PG0		
Reset:	global		
DWord	Bit	Description	
0	31:7	Preserve Default 31 7	
		<table><tr><td>Default Value:</td><td>00111110000000000000000000b</td></tr></table> The values in this field must not be changed.	Default Value:
	Default Value:	00111110000000000000000000b	
	6	ocl2_Idofuse_pwrenb	
5:0	Preserve Default 5 0		
	<table><tr><td>Default Value:</td><td>010000b</td></tr></table> The values in this field must not be changed.	Default Value:	010000b
Default Value:	010000b		



PORT_CL2CM_DW6

PORT_CL2CM_DW6		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	6C358h-6C35Bh	
Name:	PORT_CL2CM_DW6_BC	
ShortName:	PORT_CL2CM_DW6_BC	
Power:	PG0	
Reset:	global	
PHY CL2 Common Dword 6 Instances per PHY dual/single DDIB/C: PHY dual, base 0x6C000 CL2 common config base 0x340		
DWord	Bit	Description
0	31:29	Reserved
		Format: PBC The values in this field must not be changed. Use read/modify/write to update this register.
	28	oldo_dynpwrdownen Dynamic Power Down Enable for Channel 1
	27:0	Reserved
		Format: PBC The values in this field must not be changed. Use read/modify/write to update this register.



PORT_PCS_DW10

PORT_PCS_DW10	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162428h-16242Bh
Name:	PORT_PCS_DW10_LN01_A
ShortName:	PORT_PCS_DW10_LN01_A
Power:	PG0
Reset:	global
Address:	162628h-16262Bh
Name:	PORT_PCS_DW10_LN23_A
ShortName:	PORT_PCS_DW10_LN23_A
Power:	PG0
Reset:	global
Address:	162C28h-162C2Bh
Name:	PORT_PCS_DW10_GRP_A
ShortName:	PORT_PCS_DW10_GRP_A
Power:	PG0
Reset:	global
Address:	6C428h-6C42Bh
Name:	PORT_PCS_DW10_LN01_B
ShortName:	PORT_PCS_DW10_LN01_B
Power:	PG0
Reset:	global
Address:	6C628h-6C62Bh
Name:	PORT_PCS_DW10_LN23_B
ShortName:	PORT_PCS_DW10_LN23_B
Power:	PG0
Reset:	global
Address:	6CC28h-6CC2Bh
Name:	PORT_PCS_DW10_GRP_B
ShortName:	PORT_PCS_DW10_GRP_B
Power:	PG0



PORT_PCS_DW10		
Reset:	global	
Address:	6C828h-6C82Bh	
Name:	PORT_PCS_DW10_LN01_C	
ShortName:	PORT_PCS_DW10_LN01_C	
Power:	PG0	
Reset:	global	
Address:	6CA28h-6CA2Bh	
Name:	PORT_PCS_DW10_LN23_C	
ShortName:	PORT_PCS_DW10_LN23_C	
Power:	PG0	
Reset:	global	
Address:	6CE28h-6CE2Bh	
Name:	PORT_PCS_DW10_GRP_C	
ShortName:	PORT_PCS_DW10_GRP_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31	reg_tx2swingcalcinit
	30	reg_tx1swingcalcinit
	29:26	Reserved
		Format: MBZ
	25	reg_tx1deemp
	24	reg_tx2deemp
	23:0	Reserved
		Format: MBZ



PORT_PCS_DW12

PORT_PCS_DW12	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162430h-162433h
Name:	PORT_PCS_DW12_LN01_A
ShortName:	PORT_PCS_DW12_LN01_A
Power:	PG0
Reset:	global
Address:	162630h-162633h
Name:	PORT_PCS_DW12_LN23_A
ShortName:	PORT_PCS_DW12_LN23_A
Power:	PG0
Reset:	global
Address:	162C30h-162C33h
Name:	PORT_PCS_DW12_GRP_A
ShortName:	PORT_PCS_DW12_GRP_A
Power:	PG0
Reset:	global
Address:	6C430h-6C433h
Name:	PORT_PCS_DW12_LN01_B
ShortName:	PORT_PCS_DW12_LN01_B
Power:	PG0
Reset:	global
Address:	6C630h-6C633h
Name:	PORT_PCS_DW12_LN23_B
ShortName:	PORT_PCS_DW12_LN23_B
Power:	PG0
Reset:	global
Address:	6CC30h-6CC33h
Name:	PORT_PCS_DW12_GRP_B
ShortName:	PORT_PCS_DW12_GRP_B
Power:	PG0



PORT_PCS_DW12			
Reset:	global		
Address:	6C830h-6C833h		
Name:	PORT_PCS_DW12_LN01_C		
ShortName:	PORT_PCS_DW12_LN01_C		
Power:	PG0		
Reset:	global		
Address:	6CA30h-6CA33h		
Name:	PORT_PCS_DW12_LN23_C		
ShortName:	PORT_PCS_DW12_LN23_C		
Power:	PG0		
Reset:	global		
Address:	6CE30h-6CE33h		
Name:	PORT_PCS_DW12_GRP_C		
ShortName:	PORT_PCS_DW12_GRP_C		
Power:	PG0		
Reset:	global		
DWord	Bit	Description	
0	31:23	Reserved	
		Format: MBZ	
	22:20	reg_tx2_stagger_mult These bits set the lane staggering multiplier for the transmitter based on the linkclk period.	
		Value	Name
		000b	0x
		001b	1x
		010b	2x
		011b	4x
		100b	8x
		101b	16x
		110b	32x
	111b	64x	
	19	reg_lanestagger_by_group	
	18:16	reg_tx1_stagger_mult These bits set the lane staggering multiplier for the transmitter based on the linkclk period.	
		Value	Name
		000b	0x
		001b	1x



PORT_PCS_DW12			
		010b	2x
		011b	4x
		100b	8x
		101b	16x
		110b	32x
		111b	64x
	15:7	Reserved	
		Format:	MBZ
	6	reg_lanestagger_strap_ovrd	
	5	Reserved	
		Format:	MBZ
	4:0	reg_lanestagger_strap	
		Value	Name
			Description
		02h	2
		04h	4
		07h	7
		0Dh	13
		18h	24



PORT_PLL_0

PORT_PLL_0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x0000001B	
Access:	R/W	
Size (in bits):	32	
Address:	162100h-162103h	
Name:	PORT_PLL_0_A	
ShortName:	PORT_PLL_0_A	
Power:	PG0	
Reset:	global	
Address:	6C100h-6C103h	
Name:	PORT_PLL_0_B	
ShortName:	PORT_PLL_0_B	
Power:	PG0	
Reset:	global	
Address:	6C380h-6C383h	
Name:	PORT_PLL_0_C	
ShortName:	PORT_PLL_0_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:8	Reserved
	7:0	i_fbdivratio
		Default Value: 00011011b
		m2 divider. Second stage of feedback divider



PORT_PLL_1

PORT_PLL_1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000100	
Access:	R/W	
Size (in bits):	32	
Address:	162104h-162107h	
Name:	PORT_PLL_1_A	
ShortName:	PORT_PLL_1_A	
Power:	PG0	
Reset:	global	
Address:	6C104h-6C107h	
Name:	PORT_PLL_1_B	
ShortName:	PORT_PLL_1_B	
Power:	PG0	
Reset:	global	
Address:	6C384h-6C387h	
Name:	PORT_PLL_1_C	
ShortName:	PORT_PLL_1_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:18	Reserved Format: MBZ
	17	i_divretimeren
	16	i_fbdivdutycysel
	15:12	Reserved Format: MBZ
	11:8	i_ndivratio Default Value: 0001b
	7:3	Reserved Format: MBZ
	2:0	i_fbpredivratio



PORT_PLL_2

PORT_PLL_2		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	162108h-16210Bh	
Name:	PORT_PLL_2_A	
ShortName:	PORT_PLL_2_A	
Power:	PG0	
Reset:	global	
Address:	6C108h-6C10Bh	
Name:	PORT_PLL_2_B	
ShortName:	PORT_PLL_2_B	
Power:	PG0	
Reset:	global	
Address:	6C388h-6C38Bh	
Name:	PORT_PLL_2_C	
ShortName:	PORT_PLL_2_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:22	Reserved
		Format: MBZ
	21:0	i_fracdiv Fractional divider



PORT_PLL_3

PORT_PLL_3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000002	
Access:	R/W	
Size (in bits):	32	
Address:	16210Ch-16210Fh	
Name:	PORT_PLL_3_A	
ShortName:	PORT_PLL_3_A	
Power:	PG0	
Reset:	global	
Address:	6C10Ch-6C10Fh	
Name:	PORT_PLL_3_B	
ShortName:	PORT_PLL_3_B	
Power:	PG0	
Reset:	global	
Address:	6C38Ch-6C38Fh	
Name:	PORT_PLL_3_C	
ShortName:	PORT_PLL_3_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:17	Reserved Format: MBZ
	16	i_fracnen_h Fractional Modulator Enable
	15:9	Reserved Format: MBZ
	8	i_fracmodorder
	7:4	Reserved Format: MBZ
	3:0	i_feedfwrddgain Default Value: 0010b



PORT_PLL_4

PORT_PLL_4		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	162110h-162113h	
Name:	PORT_PLL_4_A	
ShortName:	PORT_PLL_4_A	
Power:	PG0	
Reset:	global	
Address:	6C110h-6C113h	
Name:	PORT_PLL_4_B	
ShortName:	PORT_PLL_4_B	
Power:	PG0	
Reset:	global	
Address:	6C390h-6C393h	
Name:	PORT_PLL_4_C	
ShortName:	PORT_PLL_4_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:0	Reserved
		Format: MBZ



PORT_PLL_6

PORT_PLL_6		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00010803	
Access:	R/W	
Size (in bits):	32	
Address:	162118h-16211Bh	
Name:	PORT_PLL_6_A	
ShortName:	PORT_PLL_6_A	
Power:	PG0	
Reset:	global	
Address:	6C118h-6C11Bh	
Name:	PORT_PLL_6_B	
ShortName:	PORT_PLL_6_B	
Power:	PG0	
Reset:	global	
Address:	6C398h-6C39Bh	
Name:	PORT_PLL_6_C	
ShortName:	PORT_PLL_6_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:19	Reserved Format: MBZ
	18:16	i_gainctrl Default Value: 001b Gain for loop filter
	15:13	Reserved Format: MBZ
	12:8	i_int_coeff Default Value: 01000b integral coefficient = $2^{(-\text{int\_coeff})}$, targeting up to 2^{-16}
	7:4	Reserved Format: MBZ



PORT_PLL_6			
	3:0	i_prop_coeff	
		Default Value:	0011b
		proportional coefficient = 2 ^(-prop_coeff)	



PORT_PLL_8

PORT_PLL_8		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x0007000D	
Access:	R/W	
Size (in bits):	32	
Address:	162120h-162123h	
Name:	PORT_PLL_8_A	
ShortName:	PORT_PLL_8_A	
Power:	PG0	
Reset:	global	
Address:	6C120h-6C123h	
Name:	PORT_PLL_8_B	
ShortName:	PORT_PLL_8_B	
Power:	PG0	
Reset:	global	
Address:	6C3A0h-6C3A3h	
Name:	PORT_PLL_8_C	
ShortName:	PORT_PLL_8_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:19	Reserved
		Format: MBZ
	18	i_tdcalssetupdeten_h
		Default Value: 1b
		Programming Notes
		Display software must not change this field.
	17:16	i_tdcsel
		Default Value: 11b
		Programming Notes
		Display software must not change this field.
	15:10	Reserved



PORT_PLL_8			
	9:0	Format:	MBZ
		i_tdctargetcnt	
		Default Value:	0000001101b
		TDC Target Count	



PORT_PLL_9

PORT_PLL_9		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00040305	
Access:	R/W	
Size (in bits):	32	
Address:	162124h-162127h	
Name:	PORT_PLL_9_A	
ShortName:	PORT_PLL_9_A	
Power:	PG0	
Reset:	global	
Address:	6C124h-6C127h	
Name:	PORT_PLL_9_B	
ShortName:	PORT_PLL_9_B	
Power:	PG0	
Reset:	global	
Address:	6C3A4h-6C3A7h	
Name:	PORT_PLL_9_C	
ShortName:	PORT_PLL_9_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:19	Reserved
		Format: MBZ
	18:16	i_pllwait_cntr
		Default Value: 100b
		Display software must not change this field.
	15:11	Reserved
		Format: MBZ
	10	i_useidvdata_h
		Display software must not change this field.
	9	i_dcoditheren_h
Default Value: 1b		
Display software must not change this field.		



PORT_PLL_9		
	8	i_afcctltsel
		Default Value: 1b
		Display software must not change this field.
	7:4	Reserved
		Format: MBZ
	3:1	i_lockthresh
		Default Value: 010b
		Lock threshold
	0	i_lockthreshsel
		Default Value: 1b
		Display software must not change this field.



PORT_PLL_10

PORT_PLL_10		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x70000000	
Access:	R/W	
Size (in bits):	32	
Address:	162128h-16212Bh	
Name:	PORT_PLL_10_A	
ShortName:	PORT_PLL_10_A	
Power:	PG0	
Reset:	global	
Address:	6C128h-6C12Bh	
Name:	PORT_PLL_10_B	
ShortName:	PORT_PLL_10_B	
Power:	PG0	
Reset:	global	
Address:	6C3A8h-6C3ABh	
Name:	PORT_PLL_10_C	
ShortName:	PORT_PLL_10_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:28	i_pllpwrmode
		Default Value: 0111b Display software must not change this field.
	27	i_dcoampovrden_h DCO amplitude override enable
	26	i_dcocoarse_ovrd_h Display software must not change this field.
	25:24	i_dcofinesel Display software must not change this field.
	23:16	i_dcocoarse Display software must not change this field.



PORT_PLL_10			
	15:14	Reserved	
		Format:	MBZ
	13:10	i_dcoamp DCO amplitude override value	
	9:0	i_dcofine Display software must not change this field.	



PORT_PLL_11

PORT_PLL_11		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	16212Ch-16212Fh	
Name:	PORT_PLL_11_A	
ShortName:	PORT_PLL_11_A	
Power:	PG0	
Reset:	global	
Address:	6C12Ch-6C12Fh	
Name:	PORT_PLL_11_B	
ShortName:	PORT_PLL_11_B	
Power:	PG0	
Reset:	global	
Address:	6C3ACh-6C3AFh	
Name:	PORT_PLL_11_C	
ShortName:	PORT_PLL_11_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:0	Reserved
		Format: MBZ



PORT_PLL_12

PORT_PLL_12		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	162130h-162133h	
Name:	PORT_PLL_12_A	
ShortName:	PORT_PLL_12_A	
Power:	PG0	
Reset:	global	
Address:	6C130h-6C133h	
Name:	PORT_PLL_12_B	
ShortName:	PORT_PLL_12_B	
Power:	PG0	
Reset:	global	
Address:	6C3B0h-6C3B3h	
Name:	PORT_PLL_12_C	
ShortName:	PORT_PLL_12_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:0	Reserved
		Format: MBZ



PORT_PLL_EBB_0

PORT_PLL_EBB_0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	162034h-162037h	
Name:	PORT_PLL_EBB_0_A	
ShortName:	PORT_PLL_EBB_0_A	
Power:	PG0	
Reset:	global	
Address:	6C034h-6C037h	
Name:	PORT_PLL_EBB_0_B	
ShortName:	PORT_PLL_EBB_0_B	
Power:	PG0	
Reset:	global	
Address:	6C340h-6C343h	
Name:	PORT_PLL_EBB_0_C	
ShortName:	PORT_PLL_EBB_0_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:16	Reserved
		Format: MBZ
	15:13	o_dtp1divsel P1-Divider to divide VCO clock from PLL before P2 divider
	12:8	o_dtp2divsel P2-Divider to divide VCO clock from PLL after P1 divider
	7:2	Reserved
		Format: MBZ
	1	i_pllfreqlock
Access: RO		
Value		Name
0b		Not lock



PORT_PLL_EBB_0			
	0	1b	Lock
		i_plllock	
		Access:	RO
		Value	Name
		0b	Not lock
		1b	Lock



PORT_PLL_EBB_4

PORT_PLL_EBB_4			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	162038h-16203Bh		
Name:	PORT_PLL_EBB_4_A		
ShortName:	PORT_PLL_EBB_4_A		
Power:	PG0		
Reset:	global		
Address:	6C038h-6C03Bh		
Name:	PORT_PLL_EBB_4_B		
ShortName:	PORT_PLL_EBB_4_B		
Power:	PG0		
Reset:	global		
Address:	6C344h-6C347h		
Name:	PORT_PLL_EBB_4_C		
ShortName:	PORT_PLL_EBB_4_C		
Power:	PG0		
Reset:	global		
DWord	Bit	Description	
0	31:15	Reserved	
		Format: PBC	
	14	o_dtafcrecal	
		Access: R/WC	
		AFC Recalibration	
		This bit is required to be set if the N-div, M1div, M2div, or PLL reference clocks are updated.	
		This bit clears when the PLL transitions from the disabled to enabled state.	
		Value	Name
		0b	disable
	1b	enable	
	13	o_dtdclkpen_h	
		Enable 10 bit clock to display controller.	
Value		Name	
0b	disable		



PORT_PLL_EBB_4			
		1b	enable
	12:0	Reserved	
		Format:	PBC



PORT_PLL_ENABLE

PORT_PLL_ENABLE			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Access:	R/W		
Size (in bits):	32		
Address:	46074h-46077h		
Name:	Port PLL Enable A		
ShortName:	PORT_PLL_ENABLE_A		
Power:	Always on		
Reset:	soft		
Address:	46078h-4607Bh		
Name:	Port PLL Enable B		
ShortName:	PORT_PLL_ENABLE_B		
Power:	Always on		
Reset:	soft		
Address:	4607Ch-4607Fh		
Name:	Port PLL Enable C		
ShortName:	PORT_PLL_ENABLE_C		
Power:	Always on		
Reset:	soft		
DWord	Bit	Description	
0	31	PLL Enable	
		This field enables or disables the port PLL.	
		Value	Name
		0b	Disable
	1b	Enable	
	30	PLL Lock	
		Access: RO	
This fields indicates the status of the port PLL Lock.			
Value		Name	
0b		Not locked or not enabled	
1b	Locked		



PORT_PLL_ENABLE			
	29:28	Reserved	
		Format:	MBZ
	27	Reference Select	
		Select between PLL references.	
		Value	Name
		1b	Non-SSC
		0b	SSC
	26:25	Reserved	
		Format:	MBZ
	24:0	Reserved	



PORT_PLL_PCS_0

PORT_PLL_PCS_0	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162400h-162403h
Name:	PORT_PLL_PCS_0_TX01_A
ShortName:	PORT_PLL_PCS_0_TX01_A
Power:	PG0
Reset:	global
Address:	162600h-162603h
Name:	PORT_PLL_PCS_0_TX23_A
ShortName:	PORT_PLL_PCS_0_TX23_A
Power:	PG0
Reset:	global
Address:	6C400h-6C403h
Name:	PORT_PLL_PCS_0_TX01_B
ShortName:	PORT_PLL_PCS_0_TX01_B
Power:	PG0
Reset:	global
Address:	6C600h-6C603h
Name:	PORT_PLL_PCS_0_TX23_B
ShortName:	PORT_PLL_PCS_0_TX23_B
Power:	PG0
Reset:	global
Address:	6C800h-6C803h
Name:	PORT_PLL_PCS_0_TX01_C
ShortName:	PORT_PLL_PCS_0_TX01_C
Power:	PG0
Reset:	global
Address:	6CA00h-6CA03h
Name:	PORT_PLL_PCS_0_TX23_C
ShortName:	PORT_PLL_PCS_0_TX23_C
Power:	PG0



PORT_PLL_PCS_0								
Reset: global								
DWord	Bit	Description						
0	31:17	Reserved						
		Format: PBC						
	16	reg_tx2_soft_reset_n Active low reset to independently reset Tx lane2 in Display Port. reg_softreset_enable is the override enable for this reset to take effect						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Lane 2 Reset</td></tr><tr><td>1b</td><td>Lane 2 Active</td></tr></table>	Value	Name	0b	Lane 2 Reset	1b	Lane 2 Active
		Value	Name					
		0b	Lane 2 Reset					
	1b	Lane 2 Active						
	15:8	Reserved						
		Format: PBC						
	7	reg_tx1_soft_reset_n Active low reset to independently reset Tx lane1 in Display Port. reg_softreset_enable is the override enable for this reset to take effect						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Lane 1 Reset</td></tr><tr><td>1b</td><td>Lane 1 Active</td></tr></table>	Value	Name	0b	Lane 1 Reset	1b	Lane 1 Active
		Value	Name					
0b		Lane 1 Reset						
1b	Lane 1 Active							
6:0	Reserved							
	Format: PBC							



PORT_REF_DW3

PORT_REF_DW3		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	16218Ch-16218Fh	
Name:	PORT_REF_DW3_A	
ShortName:	PORT_REF_DW3_A	
Power:	PG0	
Reset:	global	
Address:	6C18Ch-6C18Fh	
Name:	PORT_REF_DW3_BC	
ShortName:	PORT_REF_DW3_BC	
Power:	PG0	
Reset:	global	
PHY Ref Dword 3		
Instances per PHY dual/single		
DDIA: PHY single, base 0x162000		
DDIB/C: PHY dual, base 0x6C000		
CL1 Ref base 0x180		
DWord	Bit	Description
0	31:23	Reserved
		Format: PBC The values in this field must not be changed. Use read/modify/write to update this register.
	22	grc_done
		Access: RO
	21:0	Reserved
		Format: PBC The values in this field must not be changed. Use read/modify/write to update this register.



PORT_REF_DW6

PORT_REF_DW6		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00808080	
Access:	R/W	
Size (in bits):	32	
Address:	162198h-16219Bh	
Name:	PORT_REF_DW6_A	
ShortName:	PORT_REF_DW6_A	
Power:	PG0	
Reset:	global	
Address:	6C198h-6C19Bh	
Name:	PORT_REF_DW6_BC	
ShortName:	PORT_REF_DW6_BC	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:24	grccode Access: RO
	23:16	ogrccode_fast Default Value: 0x80
	15:8	ogrccode_slow Default Value: 0x80
	7:0	ogrccode_nom Default Value: 0x80



PORT_REF_DW8

PORT_REF_DW8								
Register Space:	MMIO: 0/2/0							
Source:	BSpec							
Default Value:	0x30000000							
Access:	R/W							
Size (in bits):	32							
Address:	1621A0h-1621A3h							
Name:	PORT_REF_DW8_A							
ShortName:	PORT_REF_DW8_A							
Power:	PG0							
Reset:	global							
Address:	6C1A0h-6C1A3h							
Name:	PORT_REF_DW8_BC							
ShortName:	PORT_REF_DW8_BC							
Power:	PG0							
Reset:	global							
DWord	Bit	Description						
0	31	fcomprefsel GRC Flash Comparator Ref Select						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0</td><td>400 ohm</td></tr><tr><td>1</td><td>100 ohm</td></tr></table>	Value	Name	0	400 ohm	1	100 ohm
		Value	Name					
		0	400 ohm					
	1	100 ohm						
	30:16	Preserve Default 30 16						
		<table><tr><td>Default Value:</td><td>0110000000000000b</td></tr></table> The values in this field must not be changed.	Default Value:	0110000000000000b				
		Default Value:	0110000000000000b					
	15	grcdis						
14:2	Preserve Default 14 2							
	<table><tr><td>Default Value:</td><td>000000000000000b</td></tr></table> The values in this field must not be changed.	Default Value:	000000000000000b					
	Default Value:	000000000000000b						
1	grc_rdy_ovrd							
0	cfg_usegrcaslrc							



PORT_TX_DW2

PORT_TX_DW2	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00809800
Access:	R/W
Size (in bits):	32
Address:	162508h-16250Bh
Name:	PORT_TX_DW2_LN0_A
ShortName:	PORT_TX_DW2_LN0_A
Power:	PG0
Reset:	global
Address:	162588h-16258Bh
Name:	PORT_TX_DW2_LN1_A
ShortName:	PORT_TX_DW2_LN1_A
Power:	PG0
Reset:	global
Address:	162708h-16270Bh
Name:	PORT_TX_DW2_LN2_A
ShortName:	PORT_TX_DW2_LN2_A
Power:	PG0
Reset:	global
Address:	162788h-16278Bh
Name:	PORT_TX_DW2_LN3_A
ShortName:	PORT_TX_DW2_LN3_A
Power:	PG0
Reset:	global
Address:	162D08h-162D0Bh
Name:	PORT_TX_DW2_GRP_A
ShortName:	PORT_TX_DW2_GRP_A
Power:	PG0
Reset:	global
Address:	6C508h-6C50Bh
Name:	PORT_TX_DW2_LN0_B
ShortName:	PORT_TX_DW2_LN0_B



PORT_TX_DW2	
Power:	PG0
Reset:	global
Address:	6C588h-6C58Bh
Name:	PORT_TX_DW2_LN1_B
ShortName:	PORT_TX_DW2_LN1_B
Power:	PG0
Reset:	global
Address:	6C708h-6C70Bh
Name:	PORT_TX_DW2_LN2_B
ShortName:	PORT_TX_DW2_LN2_B
Power:	PG0
Reset:	global
Address:	6C788h-6C78Bh
Name:	PORT_TX_DW2_LN3_B
ShortName:	PORT_TX_DW2_LN3_B
Power:	PG0
Reset:	global
Address:	6CD08h-6CD0Bh
Name:	PORT_TX_DW2_GRP_B
ShortName:	PORT_TX_DW2_GRP_B
Power:	PG0
Reset:	global
Address:	6C908h-6C90Bh
Name:	PORT_TX_DW2_LN0_C
ShortName:	PORT_TX_DW2_LN0_C
Power:	PG0
Reset:	global
Address:	6C988h-6C98Bh
Name:	PORT_TX_DW2_LN1_C
ShortName:	PORT_TX_DW2_LN1_C
Power:	PG0
Reset:	global
Address:	6CB08h-6CB0Bh
Name:	PORT_TX_DW2_LN2_C
ShortName:	PORT_TX_DW2_LN2_C



PORT_TX_DW2		
Power:	PG0	
Reset:	global	
Address:	6CB88h-6CB8Bh	
Name:	PORT_TX_DW2_LN3_C	
ShortName:	PORT_TX_DW2_LN3_C	
Power:	PG0	
Reset:	global	
Address:	6CF08h-6CF0Bh	
Name:	PORT_TX_DW2_GRP_C	
ShortName:	PORT_TX_DW2_GRP_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:24	Reserved Format: MBZ
	23:16	omargin000 Default Value: 10000000b
	15:8	ouniqtranscale Default Value: 10011000b
	7:0	Reserved Format: MBZ



PORT_TX_DW3

PORT_TX_DW3	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	16250Ch-16250Fh
Name:	PORT_TX_DW3_LN0_A
ShortName:	PORT_TX_DW3_LN0_A
Power:	PG0
Reset:	global
Address:	16258Ch-16258Fh
Name:	PORT_TX_DW3_LN1_A
ShortName:	PORT_TX_DW3_LN1_A
Power:	PG0
Reset:	global
Address:	16270Ch-16270Fh
Name:	PORT_TX_DW3_LN2_A
ShortName:	PORT_TX_DW3_LN2_A
Power:	PG0
Reset:	global
Address:	16278Ch-16278Fh
Name:	PORT_TX_DW3_LN3_A
ShortName:	PORT_TX_DW3_LN3_A
Power:	PG0
Reset:	global
Address:	162D0Ch-162D0Fh
Name:	PORT_TX_DW3_GRP_A
ShortName:	PORT_TX_DW3_GRP_A
Power:	PG0
Reset:	global
Address:	6C50Ch-6C50Fh
Name:	PORT_TX_DW3_LN0_B
ShortName:	PORT_TX_DW3_LN0_B



PORT_TX_DW3	
Power:	PG0
Reset:	global
Address:	6C58Ch-6C58Fh
Name:	PORT_TX_DW3_LN1_B
ShortName:	PORT_TX_DW3_LN1_B
Power:	PG0
Reset:	global
Address:	6C70Ch-6C70Fh
Name:	PORT_TX_DW3_LN2_B
ShortName:	PORT_TX_DW3_LN2_B
Power:	PG0
Reset:	global
Address:	6C78Ch-6C78Fh
Name:	PORT_TX_DW3_LN3_B
ShortName:	PORT_TX_DW3_LN3_B
Power:	PG0
Reset:	global
Address:	6CD0Ch-6CD0Fh
Name:	PORT_TX_DW3_GRP_B
ShortName:	PORT_TX_DW3_GRP_B
Power:	PG0
Reset:	global
Address:	6C90Ch-6C90Fh
Name:	PORT_TX_DW3_LN0_C
ShortName:	PORT_TX_DW3_LN0_C
Power:	PG0
Reset:	global
Address:	6C98Ch-6C98Fh
Name:	PORT_TX_DW3_LN1_C
ShortName:	PORT_TX_DW3_LN1_C
Power:	PG0
Reset:	global
Address:	6CB0Ch-6CB0Fh
Name:	PORT_TX_DW3_LN2_C
ShortName:	PORT_TX_DW3_LN2_C



PORT_TX_DW3		
Power:	PG0	
Reset:	global	
Address:	6CB8Ch-6CB8Fh	
Name:	PORT_TX_DW3_LN3_C	
ShortName:	PORT_TX_DW3_LN3_C	
Power:	PG0	
Reset:	global	
Address:	6CF0Ch-6CF0Fh	
Name:	PORT_TX_DW3_GRP_C	
ShortName:	PORT_TX_DW3_GRP_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:28	Reserved Format: MBZ
	27	ouniqetrangenmethod
	26	oscaledcompmethod
	25:0	Reserved Format: MBZ



PORT_TX_DW4

PORT_TX_DW4	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162510h-162513h
Name:	PORT_TX_DW4_LN0_A
ShortName:	PORT_TX_DW4_LN0_A
Power:	PG0
Reset:	global
Address:	162590h-162593h
Name:	PORT_TX_DW4_LN1_A
ShortName:	PORT_TX_DW4_LN1_A
Power:	PG0
Reset:	global
Address:	162710h-162713h
Name:	PORT_TX_DW4_LN2_A
ShortName:	PORT_TX_DW4_LN2_A
Power:	PG0
Reset:	global
Address:	162790h-162793h
Name:	PORT_TX_DW4_LN3_A
ShortName:	PORT_TX_DW4_LN3_A
Power:	PG0
Reset:	global
Address:	162D10h-162D13h
Name:	PORT_TX_DW4_GRP_A
ShortName:	PORT_TX_DW4_GRP_A
Power:	PG0
Reset:	global
Address:	6C510h-6C513h
Name:	PORT_TX_DW4_LN0_B
ShortName:	PORT_TX_DW4_LN0_B



PORT_TX_DW4	
Power:	PG0
Reset:	global
Address:	6C590h-6C593h
Name:	PORT_TX_DW4_LN1_B
ShortName:	PORT_TX_DW4_LN1_B
Power:	PG0
Reset:	global
Address:	6C710h-6C713h
Name:	PORT_TX_DW4_LN2_B
ShortName:	PORT_TX_DW4_LN2_B
Power:	PG0
Reset:	global
Address:	6C790h-6C793h
Name:	PORT_TX_DW4_LN3_B
ShortName:	PORT_TX_DW4_LN3_B
Power:	PG0
Reset:	global
Address:	6CD10h-6CD13h
Name:	PORT_TX_DW4_GRP_B
ShortName:	PORT_TX_DW4_GRP_B
Power:	PG0
Reset:	global
Address:	6C910h-6C913h
Name:	PORT_TX_DW4_LN0_C
ShortName:	PORT_TX_DW4_LN0_C
Power:	PG0
Reset:	global
Address:	6C990h-6C993h
Name:	PORT_TX_DW4_LN1_C
ShortName:	PORT_TX_DW4_LN1_C
Power:	PG0
Reset:	global
Address:	6CB10h-6CB13h
Name:	PORT_TX_DW4_LN2_C
ShortName:	PORT_TX_DW4_LN2_C



PORT_TX_DW4		
Power:	PG0	
Reset:	global	
Address:	6CB90h-6CB93h	
Name:	PORT_TX_DW4_LN3_C	
ShortName:	PORT_TX_DW4_LN3_C	
Power:	PG0	
Reset:	global	
Address:	6CF10h-6CF13h	
Name:	PORT_TX_DW4_GRP_C	
ShortName:	PORT_TX_DW4_GRP_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31:24	ow2tapdeemph9p5
	23:0	Reserved
		Format: MBZ



PORT_TX_DW5

PORT_TX_DW5	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00780000
Access:	R/W
Size (in bits):	32
Address:	162514h-162517h
Name:	PORT_TX_DW5_LN0_A
ShortName:	PORT_TX_DW5_LN0_A
Power:	PG0
Reset:	global
Address:	162594h-162597h
Name:	PORT_TX_DW5_LN1_A
ShortName:	PORT_TX_DW5_LN1_A
Power:	PG0
Reset:	global
Address:	162714h-162717h
Name:	PORT_TX_DW5_LN2_A
ShortName:	PORT_TX_DW5_LN2_A
Power:	PG0
Reset:	global
Address:	162794h-162797h
Name:	PORT_TX_DW5_LN3_A
ShortName:	PORT_TX_DW5_LN3_A
Power:	PG0
Reset:	global
Address:	162D14h-162D17h
Name:	PORT_TX_DW5_GRP_A
ShortName:	PORT_TX_DW5_GRP_A
Power:	PG0
Reset:	global
Address:	6C514h-6C517h
Name:	PORT_TX_DW5_LN0_B
ShortName:	PORT_TX_DW5_LN0_B
Power:	PG0



PORT_TX_DW5	
Reset:	global
Address:	6C594h-6C597h
Name:	PORT_TX_DW5_LN1_B
ShortName:	PORT_TX_DW5_LN1_B
Power:	PG0
Reset:	global
Address:	6C714h-6C717h
Name:	PORT_TX_DW5_LN2_B
ShortName:	PORT_TX_DW5_LN2_B
Power:	PG0
Reset:	global
Address:	6C794h-6C797h
Name:	PORT_TX_DW5_LN3_B
ShortName:	PORT_TX_DW5_LN3_B
Power:	PG0
Reset:	global
Address:	6CD14h-6CD17h
Name:	PORT_TX_DW5_GRP_B
ShortName:	PORT_TX_DW5_GRP_B
Power:	PG0
Reset:	global
Address:	6C914h-6C917h
Name:	PORT_TX_DW5_LN0_C
ShortName:	PORT_TX_DW5_LN0_C
Power:	PG0
Reset:	global
Address:	6C994h-6C997h
Name:	PORT_TX_DW5_LN1_C
ShortName:	PORT_TX_DW5_LN1_C
Power:	PG0
Reset:	global
Address:	6CB14h-6CB17h
Name:	PORT_TX_DW5_LN2_C
ShortName:	PORT_TX_DW5_LN2_C
Power:	PG0



PORT_TX_DW5		
Reset:	global	
Address:	6CB94h-6CB97h	
Name:	PORT_TX_DW5_LN3_C	
ShortName:	PORT_TX_DW5_LN3_C	
Power:	PG0	
Reset:	global	
Address:	6CF14h-6CF17h	
Name:	PORT_TX_DW5_GRP_C	
ShortName:	PORT_TX_DW5_GRP_C	
Power:	PG0	
Reset:	global	
DWord	Bit	Description
0	31	ocalcinit
	30	ocalccont
	29:23	Reserved Format: MBZ
	22	ovrd_setdata_h Default Value: 1b
	21	ovrd_resetdata_h Default Value: 1b
	20	ovrd_setdata_l Default Value: 1b
	19	ovrd_resetdata_l Default Value: 1b
	18	ovrd_dcc1010en
	17	ovrd_dfxbypassen
	16	ovrd_dccmode
	15:12	Reserved Format: MBZ
	11	otxclkspare
	10	DCC compout polarity Invert the DCC compout polarity
	9	DCC Delay Range 1 Adjust DCC delay range to 1st setting
	8	DCC Delay Range 2 Adjust DCC delay range to 2nd setting



PORT_TX_DW5			
	7:0	Reserved	
		Format:	MBZ



PORT_TX_DW14

PORT_TX_DW14	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000000
Access:	R/W
Size (in bits):	32
Address:	162538h-16253Bh
Name:	PORT_TX_DW14_LN0_A
ShortName:	PORT_TX_DW14_LN0_A
Power:	PG0
Reset:	global
Address:	1625B8h-1625BBh
Name:	PORT_TX_DW14_LN1_A
ShortName:	PORT_TX_DW14_LN1_A
Power:	PG0
Reset:	global
Address:	162738h-16273Bh
Name:	PORT_TX_DW14_LN2_A
ShortName:	PORT_TX_DW14_LN2_A
Power:	PG0
Reset:	global
Address:	1627B8h-1627BBh
Name:	PORT_TX_DW14_LN3_A
ShortName:	PORT_TX_DW14_LN3_A
Power:	PG0
Reset:	global
Address:	162D38h-162D3Bh
Name:	PORT_TX_DW14_GRP_A
ShortName:	PORT_TX_DW14_GRP_A
Power:	PG0
Reset:	global
Address:	6C538h-6C53Bh
Name:	PORT_TX_DW14_LN0_B
ShortName:	PORT_TX_DW14_LN0_B
Power:	PG0



PORT_TX_DW14	
Reset:	global
Address:	6C5B8h-6C5BBh
Name:	PORT_TX_DW14_LN1_B
ShortName:	PORT_TX_DW14_LN1_B
Power:	PG0
Reset:	global
Address:	6C738h-6C73Bh
Name:	PORT_TX_DW14_LN2_B
ShortName:	PORT_TX_DW14_LN2_B
Power:	PG0
Reset:	global
Address:	6C7B8h-6C7BBh
Name:	PORT_TX_DW14_LN3_B
ShortName:	PORT_TX_DW14_LN3_B
Power:	PG0
Reset:	global
Address:	6CD38h-6CD3Bh
Name:	PORT_TX_DW14_GRP_B
ShortName:	PORT_TX_DW14_GRP_B
Power:	PG0
Reset:	global
Address:	6C938h-6C93Bh
Name:	PORT_TX_DW14_LN0_C
ShortName:	PORT_TX_DW14_LN0_C
Power:	PG0
Reset:	global
Address:	6C9B8h-6C9BBh
Name:	PORT_TX_DW14_LN1_C
ShortName:	PORT_TX_DW14_LN1_C
Power:	PG0
Reset:	global
Address:	6CB38h-6CB3Bh
Name:	PORT_TX_DW14_LN2_C
ShortName:	PORT_TX_DW14_LN2_C
Power:	PG0



PORT_TX_DW14			
Reset:	global		
Address:	6CBB8h-6CBBBh		
Name:	PORT_TX_DW14_LN3_C		
ShortName:	PORT_TX_DW14_LN3_C		
Power:	PG0		
Reset:	global		
Address:	6CF38h-6CF3Bh		
Name:	PORT_TX_DW14_GRP_C		
ShortName:	PORT_TX_DW14_GRP_C		
Power:	PG0		
Reset:	global		
DWord	Bit	Description	
0	31	Reserved	
		<table><tr><td>Format:</td><td>PBC</td></tr></table> The values in this field must not be changed. Use read/modify/write to update this register.	Format:
	Format:	PBC	
	30	latency_optim	
29:0	Reserved		
	<table><tr><td>Format:</td><td>PBC</td></tr></table> The values in this field must not be changed. Use read/modify/write to update this register.	Format:	PBC
Format:	PBC		



Power Clock State Register

PWR_CLK_STATE - Power Clock State Register	
Register Space:	MMIO: 0/2/0
Source:	BSpec
Default Value:	0x00000066 0x00000466
Access:	R/W
Size (in bits):	32
Address:	020C8h
Name:	Render Power Clock State Register
ShortName:	R_PWR_CLK_STATE
Address:	220C8h
Name:	BCS Power Clock State Register
ShortName:	BCS_PWR_CLK_STATE
Address:	120C8h
Name:	VCS Power Clock State Register
ShortName:	VCS_PWR_CLK_STATE
Address:	1A0C8h
Name:	VECS Power Clock State Register
ShortName:	VECS_PWR_CLK_STATE
This register contains the mode selection for configuring render engine to attain desired performance and power requirements for a given context. This register is render context save/restored. This register must be initialized correctly when the context is submitted for the first time. This register is context save/restored as part of Exec-List context image in both Exec-List and Ring-Buffer mode of scheduling. This register contents are valid only when "Enable" bit [31] of the register is set.	
Programming Notes	
This register is only functional for RenderCS. This register must not be exercised in VideoCS, BlitterCS and VideoEnhancementCS.	
This register must not be programmed directly through CPU MMIO cycle. Exec-List Scheduling Mode: Every context can have its own required render engine configuration by programming this register appropriately in the logical render context image in memory (LRCA) before submitting the context to the execlist submit port. This register must not be programmed using MI_LOAD_REGISTER_IMM command in ring buffer or in batch buffer, however programming "NON-SLM Indication" field through MI_LOAD_REGISTER_IMM is an exception defined below. If a need arises to change the render configuration for a context being executed in HW, Scheduler must preempt the context and update the desired render configuration in the logical render context image in memory and resubmit the context. Only "NON-SLM Indictaion" field in R_PWR_CLK_STATE register is allowed to be modified through MI_LOAD_REGISTER_IMM command in ring_buffer or privileged_batch_buffer. SW must modify only "NON-SLM Indication" field and must ensure to program other fields with the same value as in LRCA. SW must ensure to	



PWR_CLK_STATE - Power Clock State Register

program PIPECONTROL flush command with CS Stall and HDC Flush prior to programming MI_LOAD_REGISTER_IMM command to modify "NON-SLM Indication" in R_PWR_CLK_STATE register.
 Example: //R_PWR_CLK_STATE register value in LRCA configured with two slices and NON-SLM indication reset: 0x80005_0000 //SW desires to set NON-SLM Indication filed in ring buffer MI_LOAD_REGISTER_IMM 0x20C8, 0x8005_0100

Ring Buffer Scheduling: This register must be programmed using MI_LOAD_REGISTER_IMM command in the ring buffer. When this register is being programmed to re-configure the number of slices, SW must context save the state before programming this register and restore the state after programming the register via dummy MI_SET_CONTEXT command, this will ensure the existing state is programmed to all the new slices that are powered up, in case of slice shutdown (slice power down) this is not required.

Example:

MI_SET_CONTEXT -> CXTA

MI_BATCH_BUFFER_START

MI_BATCH_BUFFER_START

MI_SET_CONTEXT -> CXTB //Dummy Context to save existing render state to be restored latter.

MI_LOAD_REGISTER_IMM : R_PWR_CLK_STATE (1 Slice to 3 Slices) // Slice configuration done.

MI_STORE_DATA_IMM (Update R_PWR_CLK_STATE value in CXTA context image to modified value)

MI_SET_CONTEXT -> CXTA // Context restore of valid state to all the slices powered up with R_PWR_CLK_STATE restored with modified value.

Power Clock State Enable must be always set with Render Power Clock state properly configured upon exercising Slice Shutdown or when "Render Power Gate Enabled" via POWERGATE_ENABLE register.

DWord	Bit	Description
0	31	Power Clock State Enable
		Format: U1
	30:0	Power Clock State
		Format: Power Clock State Format

Value	Name	Description
0h	Power Clock State Disabled	No specific power state set, bits[30:0] are ignored.
1h	Power Clock State Enabled	Power Clock is set and bit[30:0] are valid and have the desired state.



Power Management Capabilities

PMCAP_0_2_0_PCI - Power Management Capabilities			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000022		
Size (in bits):	16		
Address:	000D2h		
This register provides information on the capabilities of the function related to powermanagement.			
DWord	Bit	Description	
0	15:11	PME Support	
		Default Value:	00000b
		Access:	RO
		This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.	
	10	D2 Support	
		Default Value:	0b
		Access:	RO
		Hardwired to 0 to indicate the D2 power management state is not supported.	
	9	D1 Support	
		Default Value:	0b
		Access:	RO
		Hardwired to 0 to indicate that the D1 power management state is not supported.	
	8:6	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	5	Device Specific Initialization	
		Default Value:	1b
		Access:	RO
		Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.	
	4	RESERVED	
		Default Value:	000b



PMCAP_0_2_0_PCI - Power Management Capabilities

		Access:	RO
		Reserved	
	3	PME Clock	
		Default Value:	0b
		Access:	RO
		Hardwired to 0 to indicate IGD does not support PME# generation.	
	2:0	Version	
		Default Value:	010b
		Access:	RO
		Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification.	



Power Management Capabilities ID

PMCAPID_0_2_0_PCI - Power Management Capabilities ID			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000001		
Size (in bits):	16		
Address:	000D0h		
This register contains the PCI Power Management Capability ID and the next capability pointer.			
DWord	Bit	Description	
0	15:8	Next Capability Pointer	
		Default Value:	00000000b
		Access:	RO
		This is a hardwired pointer to the next item in the capabilities list.	
	7:0	Capability Identifier	
		Default Value:	00000001b
		Access:	RO
Hardwired to 01h for power management.			



Power Management Control and Status

PMCS_0_2_0_PCI - Power Management Control and Status		
Register Space: PCI: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 16		
Address: 000D4h		
DWord	Bit	Description
0	15	PME Status
		Default Value: 0b
		Access: RO
		This bit is hardwired to 0 to indicate that IGD does not support PME# generation from D3 (cold).
	14:13	Data Scale
		Default Value: 00b
		Access: RO
		This field is hardwired to 00 to indicate IGD does not support data register.
	12:9	Data Select
		Default Value: 0000b
		Access: RO
		This field is hardwired to 0h to indicate IGD does not support data register.
	8	PME Enable
		Default Value: 0b
		Access: RO
		This bit is hardwired to 0 to indicate that PME# assertion from D3 (cold) is disabled.
	7:2	RESERVED
		Default Value: 000b
		Access: RO
		Reserved
	1:0	Power State
		Default Value: 00b
		Access: RO Variant

**PMCS_0_2_0_PCI - Power Management Control and Status**

This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. Behavior of the graphics controller in supported states is detailed in the power management section of the Bspec.

Bits[1:0] Power state

00: D0 Default

01: D1 Not Supported

10: D2 Not Supported

11: D3



PP_CONTROL

PP_CONTROL								
Register Space:	MMIO: 0/2/0							
Source:	BSpec							
Default Value:	0x00000002							
Access:	R/W							
Size (in bits):	32							
Address:	C7204h-C7207h							
Name:	Panel Power 1 Control							
ShortName:	PP_CONTROL_1							
Power:	PG0							
Reset:	soft							
Address:	C7304h-C7307h							
Name:	Panel Power 2 Control							
ShortName:	PP_CONTROL_2							
Power:	PG0							
Reset:	soft							
DWord	Bit	Description						
0	31:9	Reserved						
		Format: MBZ						
	8:4	Power Cycle Delay						
		This field provides the delay for the eDP T12 time; the shortest time from panel power disable to power enable.						
		If panel power power state target is set to on during this delay, the power on sequence will not commence until the delay is complete.						
		The value should be programmed to (desired delay / 100 milliseconds) + 1.						
		Writing a value of 0 selects no delay or is used to abort the delay if it is active.						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>00000b</td><td>No delay</td></tr><tr><td>00101b</td><td>400 mS</td></tr></table>	Value	Name	00000b	No delay	00101b	400 mS
	Value	Name						
	00000b	No delay						
00101b	400 mS							
	Restriction							
	Restriction : A correct value must be programmed before enabling panel power.							
3	VDD Override							
	This field forces VDD on. This is intended for panels that require VDD to be asserted before accessing AUX channel.							
	<table><tr><th>Value</th><th>Name</th></tr></table>	Value	Name					
Value	Name							



PP_CONTROL						
		<table><tr><td>0b</td><td>Not Force</td></tr><tr><td>1b</td><td>Force</td></tr></table>	0b	Not Force	1b	Force
	0b	Not Force				
	1b	Force				
		Restriction				
	Restriction : When software clears this bit from '1' to '0' (stop forcing VDD on) it must ensure that T4 power cycle delay is met before setting this bit to '1' again.					
2	Backlight Enable This field enables the backlight when hardware is in the correct panel power sequence state.					
	Value	Name				
	0b	Disable				
	1b	Enable				
1	Power Down on Reset This field selects whether the panel will run the power down sequence when a reset is detected.					
	Value	Name				
	0b	Do not run power down on reset				
	1b	Run power down on reset [Default]				
	Programming Notes					
	Running power down on reset is recommended for panel protection.					
0	Power State Target This field sets the panel power state target. It can be written at any time and takes effect at the completion of any current power cycle.					
	Value	Name				
	Description					
	0b	Off	If panel power is currently on, the power off sequence starts immediately. If a power on sequence is currently in progress, the power off sequence starts after the power on state is reached, which may include a power cycle delay.			
1b	On	If panel power is currently off, the power on sequence starts immediately. If a power off sequence is currently in progress, the power on sequence starts after the power off state is reached and the power cycle delay is met.				



PP_OFF_DELAYS

PP_OFF_DELAYS		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	C720Ch-C720Fh	
Name:	Panel Power 1 Off Delays	
ShortName:	PP_OFF_DELAYS_1	
Power:	PG0	
Reset:	soft	
Address:	C730Ch-C730Fh	
Name:	Panel Power 2 Off Delays	
ShortName:	PP_OFF_DELAYS_2	
Power:	PG0	
Reset:	soft	
DWord	Bit	Description
0	31:29	Reserved Format: <table border="1">MBZ</table>
	28:16	Power Down Delay This fields provides the delay during power down. Software programs this field with the time delay for the eDP T10 time value; the time from source ending valid video data to source disabling panel power. Software controls the source valid video data output. The time unit is 100us.
	15:13	Reserved Format: <table border="1">MBZ</table>
	12:0	Backlight Off to Power Down This field provides the backlight off to power down delay. Software programs this field with the time delay for the eDP T9 time value; the time from backlight disable to source ending valid video data. Software controls the backlight disable and source valid video data output. The time unit is 100us.



PP_ON_DELAYS

PP_ON_DELAYS		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	C7208h-C720Bh	
Name:	Panel Power 1 On Delays	
ShortName:	PP_ON_DELAYS_1	
Power:	PG0	
Reset:	soft	
Address:	C7308h-C730Bh	
Name:	Panel Power 2 On Delays	
ShortName:	PP_ON_DELAYS_2	
Power:	PG0	
Reset:	soft	
DWord	Bit	Description
0	31:29	Reserved Format: MBZ
	28:16	Power Up Delay This field provides the delay during panel power up. Software programs this field with the delay for eDP T3; the time from enabling panel power to when the sink HPD and AUX channel should be ready. Software controls when AUX channel transactions start. The time unit is 100us.
	15:13	Reserved Format: MBZ
	12:0	Power On to Backlight On This field provides the power on to backlight enable delay. Software controls the source valid video data output and can enable backlight after this delay has been met. Hardware will not allow the backlight to enable until after the power up delay (eDP T3) and this delay have passed. The time unit is 100us.



PP_STATUS

PP_STATUS				
Register Space:		MMIO: 0/2/0		
Source:		BSpec		
Default Value:		0x00000000		
Access:		RO		
Size (in bits):		32		
Address:		C7200h-C7203h		
Name:		Panel Power 1 Status		
ShortName:		PP_STATUS_1		
Power:		PG0		
Reset:		soft		
Address:		C7300h-C7303h		
Name:		Panel Power 2 Status		
ShortName:		PP_STATUS_2		
Power:		PG0		
Reset:		soft		
DWord	Bit	Description		
0	31	Panel Power On Status		
		Value	Name	Description
		0b	Off	Panel power down has completed. A power cycle delay may be currently active.
		1b	On	Panel power up has completed or power down sequence in progress.
		Programming Notes		
		Software is responsible for enabling the embedded panel display only at the correct point as defined in the mode set sequence.		
	30	Reserved		
		Format: MBZ		
	29:28	Power Sequence Progress		
		Value	Name	Description
		00b	None	Panel is not in a power sequence
		01b	Power Up	Panel is in a power up sequence (may include power cycle delay)
10b		Power Down	Panel is in a power down sequence	
11b		Reserved	Reserved	
27	Power Cycle Delay Active			
Power cycle delays occur after a panel power down sequence or after a hardware reset.				



PP_STATUS			
		Value	Name
		0b	Not Active [Default]
		1b	Active
	26:4	Reserved	
		Format:	MBZ
	3:0	Reserved	



PPPR

PPPR - PPPR			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	124824h		
GT uses this register to post pending page requests to software, such as x86 page faults. A write to this register triggers an MSI per the registers PRESTS, PRECTL, PREDATA, PREADR, and PREUADR.			
DWord	Bit	Description	
0	31:1	RESERVED	
		Default Value:	0000000h
		Access:	RO
		Reserved	
	0	POST PENDING PAGE REQUEST	
		Default Value:	0h
		Access:	WO
Post Pending Page Request			

**PPRO**

PPRO - PPRO			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	124820h		
GT uses this register to post Page Request Queue overflow faults			
DWord	Bit	Description	
0	31:1	RESERVED	
		Default Value:	0000000h
		Access:	RO
		Reserved	
	0	POST PAGE REQUEST OVERFLOW FAULT	
		Default Value:	0h
		Access:	WO
Post Page Request overflow fault			



PRMRR_BASE_LSB

PRMRR_BASE_LSB - PRMRR_BASE_LSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04CD8h		
The PMRR range is used to protect Xucode memory from unauthorized reads and writes. This register controls the location of the PRMRR range by indicating its starting address. It functions in tandem with the PRMRR mask register. This register is a LOCAL CR register and not an MMIO register			
DWord	Bit	Description	
0	31:12	RANGE_BASE	
		Default Value:	00000h
		Access:	R/W Lock
		This field corresponds to bits 38:12 of the base address memory range which is allocated to EMRR memory.	
	11:0	RESERVED	
		Default Value:	000h
		Access:	RO
		Reserved	



PRMRR_BASE_MSB

PRMRR_BASE_MSB - PRMRR_BASE_MSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	04CDCh		
The PMRR range is used to protect Xucode memory from unauthorized reads and writes. This register controls the location of the PRMRR range by indicating its starting address. It functions in tandem with the PRMRR mask register. This register is a LOCAL CR register and not an MMIO register			
DWord	Bit	Description	
0	6:0	RANGE_BASE	
		Default Value:	00h
		Access:	R/W Lock
		This field corresponds to bits 38:12 of the base address memory range which is allocated to EMRR memory.	



PRMRR_MASK_LSB

PRMRR_MASK_LSB - PRMRR_MASK_LSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	04CE0h		
This register controls the size of the PRMRR range by indicating which address bits must match the PRMRR base register value.			
This register is a LOCAL CR register and not an MMIO register			
DWord	Bit	Description	
0	31:12	RANGE_MASK	
		Default Value:	00000h
		Access:	R/W Lock
		This field indicates which address bits must match PRMRR base in order to qualify as an PRMRR access.	
	11	RANGE_EN	
		Default Value:	0b
		Access:	R/W Lock
		Indicates whether the EMRR range is enabled and valid.	
	10	LOCK	
		Default Value:	0b
		Access:	R/W Lock
		Setting this bit locks all writeable settings in this register, including itself.	
	9	IWB_EN	
		Default Value:	0b
		Access:	R/W Lock
		Implicit Writeback enable. Used by the System agent with memory tracing.	
	8	TRACE_EN	
		Default Value:	0b
		Access:	R/W Lock
		Trace enable. Used by the System agent to enable memory tracing.	



PRMRR_MASK_LSB - PRMRR_MASK_LSB		
	7:0	RESERVED
		Default Value: 00h
		Access: RO
		Reserved



PRMRR_MASK_MSB

PRMRR_MASK_MSB - PRMRR_MASK_MSB			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	04CE4h		
This register controls the size of the PRMRR range by indicating which address bits must match the PRMRR base register value.			
This register is a LOCAL CR register and not an MMIO register			
DWord	Bit	Description	
0	6:0	RANGE_MASK	
		Default Value:	00h
		Access:	R/W Lock
		This field indicates which address bits must match PRMRR base in order to qualify as an PRMRR access.	



PS_WIN_SZ

PS_WIN_SZ		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	Double Buffered	
Size (in bits):	32	
Double Buffer	Start of vertical blank	
Update Point:		
This register specifies the size in pixels of the scaled output window. A programmed value of (100, 100) will result in scaled output window of size 100x100 pixels. Writes to this register arm PS registers on this pipe. After arming, any write to other PS registers will disarm all PS registers. Subsequent write to this register will arm them again.		
Restriction		
Restriction : When scaling a pipe, the scaled output must fit inside the pipe active area, so Pipe active size >= PS window position + PS window size. When scaling a plane, the scaled output must fit inside the pipe source area, so Pipe source size >= PS window position + PS window size.		
DWord	Bit	Description
0	31:29	Reserved
		Format: MBZ
	28:16	XSIZE This field specifies the horizontal size in pixels of the scaled output window.
	15:13	Reserved
		Format: MBZ
	12:0	YSIZE
This field specifies the vertical size in scan lines of the scaled output window.		
Restriction : Bit 0 must be zero for interlaced modes.		



PS Depth Count

PS_DEPTH_COUNT - PS Depth Count		
Register Space:	MMIO: 0/2/0	
Source:	RenderCS	
Default Value:	0x00000000, 0x00000000	
Access:	R/W	
Size (in bits):	64	
Trusted Type:	1	
Address:	02350h	
This register stores the value of the count of samples that have passed the depth test. This register is part of the context save and restore. Note that the value of this register can be obtained in a pipeline-synchronous fashion without a pipeline flush by using the 3DCONTROL command. See 3D Overview in the 3D volume. More details about the precise event counted by this register are located here.		
Restriction		
Restriction: Due to known HW issue this register doesn't reflect correct value and hence not dependable.		
DWord	Bit	Description
0..1	63:32	Depth Count UDW This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.
	31:0	Depth Count LDW This register reflects the total number of samples that have passed the depth test (i.e., will be visible). All samples are counted when Statistics Enable is set in the Windower State. See the Windower chapter of the 3D volume for details. Samples that pass the depth test but fail the stencil test will not be counted.



PWR_WELL_CTL

PWR_WELL_CTL		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Access:	R/W	
Size (in bits):	32	
Address:	45400h-45403h	
Name:	Power Well Control 1	
ShortName:	PWR_WELL_CTL1	
Power:	PG0	
Reset:	global	
Address:	45404h-45407h	
Name:	Power Well Control 2	
ShortName:	PWR_WELL_CTL2	
Power:	PG0	
Reset:	global	
Description		
This register is used for display power control. There are multiple instances of this register format to allow software components to have parallel control of the display power. PWR_WELL_CTL1 is generally used for BIOS to control power. PWR_WELL_CTL2 is generally used for driver to control power. The power enable requests from all sources are logically ORd together to enable the power, so the power will only disable after all sources have requested the power to disable. When a power well is disabled (powered down), access to any registers in the power well will complete, but write data will be dropped and read data will be all zeroes. The display connections diagram indicates which functional blocks are contained in each power well. The display MMIO register specification has a field for each register to indicate which power well it is in. This register is on the ungated clock and the chip reset, not the FLR reset.		
Restriction		
Restriction : The power request field must not be changed for a resource while a power enable/disable for that resource is currently in progress, as indicated by power well state for that resource. Restriction : Power wells must be enabled and disabled following the display initialization and mode set sequences.		
DWord	Bit	Description
0	31	Power Well 2 Request
		Access: R/W



PWR_WELL_CTL										
		This field requests power well #2 to enable or disable. <table><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0b</td><td>Disable</td></tr><tr><td>1b</td><td>Enable</td></tr></tbody></table> Restriction Restriction : Power well #2 must not be enabled until after FUSE_STATUS Fuse PG1 Distribution Status is Done. Power well #2 must not be enabled when Power well #1 is disabled.	Value	Name	0b	Disable	1b	Enable		
Value	Name									
0b	Disable									
1b	Enable									
30	Power Well 2 State <table><tr><td>Access:</td><td>RO</td></tr></table> This field indicates the status of power well #2. <table><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0b</td><td>Disabled</td></tr><tr><td>1b</td><td>Enabled</td></tr></tbody></table>		Access:	RO	Value	Name	0b	Disabled	1b	Enabled
Access:	RO									
Value	Name									
0b	Disabled									
1b	Enabled									
29	Power Well 1 Request <table><tr><td>Access:</td><td>R/W</td></tr></table> This field requests power well #1 to enable or disable. <table><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0b</td><td>Disable</td></tr><tr><td>1b</td><td>Enable</td></tr></tbody></table> Restriction Restriction : Power well #1 must not be enabled until after FUSE_STATUS Fuse PG0 Distribution Status is Done. Power well #1 must not be disabled when Power well #2 is enabled.		Access:	R/W	Value	Name	0b	Disable	1b	Enable
Access:	R/W									
Value	Name									
0b	Disable									
1b	Enable									
28	Power Well 1 State <table><tr><td>Access:</td><td>RO</td></tr></table> This field indicates the status of power well #1. <table><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>0b</td><td>Disabled</td></tr><tr><td>1b</td><td>Enabled</td></tr></tbody></table>		Access:	RO	Value	Name	0b	Disabled	1b	Enabled
Access:	RO									
Value	Name									
0b	Disabled									
1b	Enabled									
27:26	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>		Format:	MBZ						
Format:	MBZ									
25:24	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>		Format:	MBZ						
Format:	MBZ									
23:16	Reserved									



PWR_WELL_CTL			
		Format:	MBZ
	15:14	Reserved	
		Format:	MBZ
	13:12	Reserved	
		Format:	MBZ
	11:10	Reserved	
		Format:	MBZ
	9:0	Reserved	
		Format:	MBZ



RC6 Context Base

RC6CTXBASE - RC6 Context Base			
Register Space:		MMIO: 0/2/0	
Default Value:		0x00000000	
Size (in bits):		32	
Address:		00D48h	
RC6 Location			
DWord	Bit	Description	
0	31:12	RC6 Memory Base Low	
		Access:	R/W Lock
		This field is used to set the base of memory where the RC6 power context will be saved This value MUST be above the base and below the top of stolen memory This register is locked (becomes read-only) when RC6MEMLOCK is 1	
	11:4	RC6 Memory Base High	
		Access:	R/W Lock
		This field corresponds to bits [39:32] of RC6MEMBASE Use above 4GB is not currently supported, and these bits must be set to 0 This register is locked (becomes read-only) when RC6MEMLOCK is 1	
	3	Reserved	
		Access:	RO
2	Write Register Content to GT		
	Access:	R/W Lock	
	RPMunit will forward C6 context steering bit/DRAM context base value to MSQCunit on boot vector message as part of GT C6 exit flow. Writing to this bit will re-initiate a c6 steering bit/dram base write to MSQCunit(in GT) even after boot vector message. This bit is self-cleared on sampling. This register is locked (becomes read-only) when RC6MEMLOCK is 1		
1	RC6 DRAM Only		
	Access:	R/W Lock	
	1'b0 : Allow C6 context to go to either DRAM or C6SRAM, as specified by RC6LOCATION(default) 1'b1 : C6 context always goes to DRAM; RC6LOCATION is ignored This register is locked (becomes read-only) when RC6MEMLOCK is 1		



RC6CTXBASE - RC6 Context Base		
	0	RC6Context Base Register Lock Access: R/W Lock 1'b0 : All fields of this register are writable (default) 1'b1 : This register is Read Only BIOS must set this bit to prevent further changes



RC6 LOCATION

RC6LOCATION - RC6 LOCATION			
Register Space:		MMIO: 0/2/0	
Default Value:		0x00000001	
Size (in bits):		32	
Address:		00D40h	
RC6 Location			
DWord	Bit	Description	
0	31	RC6Context Location Lock	
		Access:	R/W Lock
	1'b0 : All fields of this register are writable (default)		
	1'b1 : This register is Read Only		
	BIOS must set this bit to prevent further changes		
30:1	Reserved		
	Access:	RO	
0	0	RC6Context Location	
		Access:	R/W Lock
	1'b0 : Send context data to C6SRAM (default)		
	1'b1 : Send context data to DRAM location specified in RC6MEMBASE		



RCC LRA 0

RCC_LRA_0 - RCC LRA 0			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0200FE00		
Size (in bits):	32		
Address:	04A40h		
DWord	Bit	Description	
0	31:27	Reserved	
		Default Value:	00000b
		Access:	RO
	26:18	RCC LRA1 Min	
		Access:	R/W
		Minimum value of programmable LRA1.	
		Value	Name
		010000000b	[Default]
	17:9	RCC LRA0 Max	
		Access:	R/W
		Maximum value of programmable LRA0.	
		Value	Name
		001111111b	[Default]
	8:0	RCC LRA0 Min	
		Default Value:	000000000b
		Access:	R/W
Minimum value of programmable LRA0.			



RCC LRA 1

RCC_LRA_1 - RCC LRA 1		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x3FDE13BD	
Size (in bits):	32	
Address:	04A44h	
DWord	Bit	Description
0	31	Reserved
		Default Value: 0b
		Access: RO
	30:22	RCC LRA2 Max
		Access: R/W
		Maximum value of programmable LRA2.
		Value Name
		011111111b [Default]
	21:13	RCC LRA2 Min
		Access: R/W
		Minimum value of programmable LRA2.
		Value Name
		011110000b [Default]
	12:11	GATR LRA
		Default Value: 10b
		Access: R/W
		Which LRA should GATR use.
	10:2	RCC LRA1 Max
		Access: R/W
		Maximum value of programmable LRA1. If RCCLRA2Min == RCCLRA2Max , GATR LRA is disabled, GATR cycles are mapped to RCCLRA0 If RCCLRA2Min == RCCLRA2Max , GATR LRA is disabled, RCCLRA1Max will default to RCCLRA2Max to reuse GATR entries
		Value Name
		011101111b [Default]



RCC_LRA_1 - RCC LRA 1		
	1	MSC LRA
		Default Value: 0b
		Access: R/W
		Which LRA should MSC use.
	0	RCC LRA
		Default Value: 1b
		Access: R/W
		Which LRA should RCC use.



Revision Identification

RID2_0_2_0_PCI - Revision Identification			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	8		
Address:	00008h		
This register contains the revision number for Device #2 Functions 0.			
DWord	Bit	Description	
0	7:4	Revision Identification Number MSB	
		Default Value:	0000b
		Access:	RO Variant Firmware Only
		Four MSB of RID	
	3:0	Revision Identification Number	
		Default Value:	0000b
		Access:	RO Variant Firmware Only
		Four LSB of RID	



RTADDR_LSB

RTADDR_LSB - RTADDR_LSB		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 124830h		
Register providing the base address of root-entry table.		
DWord	Bit	Description
0	31:12	RTA
		Default Value: 0000000h
		Access: R/W
		This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.
	11	RTT
		Default Value: 0h
		Access: R/W
		This field specifies the type of root-table referenced by the Root Table Address (RTA) field; 0: Root Table 1: Extended Root Table
	10:0	RESERVED
		Default Value: 000h
		Access: R/W
		Reserved



RTADDR_MSB

RTADDR_MSB - RTADDR_MSB		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 124834h		
Register providing the base address of root-entry table.		
DWord	Bit	Description
0	31:7	RESERVED
		Default Value: 000000h
		Access: R/W
		Reserved
	6:0	RTA Default Value: 00h Access: R/W This register points to base of page aligned, 4KB-sized root-entry table in system memory. Hardware ignores and not implements bits 63:HAW, where HAW is the host address width. Software specifies the base address of the root-entry table through this register, and programs it in hardware through the SRTP field in the Global Command register. Reads of this register returns value that was last programmed to it.



SCRATCH1

SCRATCH1 - SCRATCH1		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000001		
Size (in bits): 32		
Address: 0B11Ch		
DWord	Bit	Description
0	31:13	SCRATCH Access: R/W
	12	SLM Save ECC hang Fix Disable Access: R/W 0 - Hang indication sent to ltiseqslunit when uncorrectable error detected in any of the SLM lanes 1 - Hang indication sent to ltiseqslunit when uncorrectable error detected only in SLM lane0 lbcf_slmsave_ecc_hang_fix_disable
	11	Snoop SLM Save Restore Fix Disable Access: R/W 0 (default): Snoop fix during SLM Save Restore is enabled 1 : Snoop fix in LTCD during SLM Save Restore is disabled lbcf_ltcd_snpfix_dis
	31:10	SCRATCH Access: R/W
	10	LTCD LAST TX IROW FIX Access: R/W 0 (default): last transaction hitting irow before self-init/ebb-init bug fix enabled 1 : last transaction hitting irow before self-init/ebb-init bug fix disabled lbcf_lasttx_hitirow_fix_dis
	9	LSQC RORW Performance Fix Disable Access: R/W 0 (default) : Order cam match should not be qualified with destination for read serialization fix. 1 : Order cam match will be qualified with destination for read serialization fix. lbcf_csr_lsqc_rorwperf_dis



SCRATCH1 - SCRATCH1

	8	Eviction Performance Fix Enable	Access:	R/W
		Disable Eviction Performance fix 0 (default) - Enable Eviction Performance Fix in LSQC 1 - Disable Eviction Performance Fix in LSQC Value of this bit should be same as LBCF register bit 0xb118[22]. Value of this bit should be same as LNCf register bit 0xb008[0]. lbcf_csr_evict_perf_fix_en		
	31:7	SCRATCH	Access:	R/W
	7	Prefetch Page Fault Hang Fix Enable	Access:	R/W
		0 (default) - State/URB prefetch request does not hang for page fault, but no cache fill is done 1 - State/URB prefetch request hangs for page fault. lbcf_csr_cfg_pf_pgflt_fix_en		
	6	Coherent SQCAM Disable	Access:	R/W
		0 (default) - Enable sqcam look up for coh cycles 1 - Disable sqcam look up for coh cycles lbcf_csr_coh_sqcam_en		
	5	SLM/Non-SLM Fair Arbitration Fix Disable	Access:	R/W
		0 (default) - SLM/non-SLM Fair arbitration fix is enabled 1 - SLM/non-SLM Fair arbitration fix is disabled lbcf_csr_fairarb_perf_fix_dis		
	4	LSQC Non Coherent Flush on PM Flush Disable	Access:	R/W
		0 : (default) When PM flush is sent to L3, LSQC will generate Query to flush coherent and Non coherent Lines (DC/L3 ways) from L3. 1: When PM flush is sent to L3, LSQC will generate Query to flush only the Coherent Lines (DC/L3 ways) from L3. lbcf_csr_lsqc_flush_nc_on_pm_flush_dis		

**SCRATCH1 - SCRATCH1**

	3	roinv stall deassert	
		Default Value:	0
		Access:	R/W
		0-When any of the text,const,state,text flag ro invalidation is in progress the stall is not deasserted 1-When any of the text,const,state,text flag ro invalidation is in progress the stall is deasserted lbcf_ltdc_roinv_stall_deassert	
	2	LBS SLA Retry Timer Decrement	
		Default Value:	0b
		Access:	R/W
		1: LBS SLA Retry Timer Decrement is enabled 0: LBS SLA Retry Timer Decrement is disabled This bit needs to be programmed to 1 to avoid SNOOP response livelock lbcf_lbs_sla_retry_timer_dec_en	
	1	LSQC COH SNOOP COAMA STREAM FIX EN	
		Default Value:	0b
		Access:	R/W
		1: Coherent Snoop Coama Stream related fix is enabled. 0: Fix is disabled lbcf_lsqc_coh_snp_coama_stream_fix_en	
	0	Reserved	



SCRATCH 2 for LNCUnit

SCRATCH_LNCF2 - SCRATCH 2 for LNCUnit		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	32	
Address:	0B0A0h	
DWord	Bit	Description
0	31	Disable LNI SLM-ATOMIC on P1 Access: R/W Disable SLMATM on LNI Port1 0 (default) - slm atomic can go on port1 1 - Set the behavior to old rtl without the fix Incf_csr_lni_slmatomic_p1_cb
	30	LNI Read on Port0 with memrdrtm CB Access: R/W LNI Read on Port0 with memrdrtm CB 0 - (default) Read will be scheduled on Port-0 along with Memory Read Return 1 - Read will not be scheduled on Port0 along with Memory Read Return Incf_csr_lni_rdonp0_memrd_cb
	29	LNI Write on P1 with memrdrtm CB Access: R/W LNI Write on P1 with memrdrtm CB 0 - (default) Writes from p0 local bank will be routed to output port1 when mem rd rtn is present 1 - Writes from p0 local bank will not be routed to port1 in presence of mem rd rtn Incf_csr_lni_wronp1_memrd_cb
	28	LNI HDCx WR toggle Signal Fix CB Access: R/W LNI HDCx WR toggle Signal Fix CB 0 - (default) Hdcxwr_tgl will not toggle if HDC Writes are granted on both P0 and P1 1 - (default) Hdcxwr_tgl toggle if HDC Writes are granted on both P0 and P1 Incf_csr_lni_hdcxwr_tgl_cb
	27	Reserved
	26	Reserved
	25	Reserved



SCRATCH_LNCF2 - SCRATCH 2 for LNCFunit			
	24	Reserved	
	23	Reserved	
	22:0	SCRATCH 2 field for LNCFunit	
		Access:	R/W



SCRATCH2 Register

SCRATCH2 - SCRATCH2 Register			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	0B140h		
DWord	Bit	Description	
0	31:0	SCRATCH2	
		Access:	R/W



SCRATCH for LNCUnit

SCRATCH_LNCF1 - SCRATCH for LNCUnit		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x00000001	
Size (in bits):	32	
Address:	0B008h	
DWord	Bit	Description
0	31:8	SCRATCH register for LNCUnit Access: R/W
	7	Reserved3 Access: R/W Reserved
	6	Reserved3 Access: R/W Reserved
	5	Disable LNI Port1 Read Priority Access: R/W 0: (Default) Allow LNI to arbitrate read with highest priority over write on port1. 1: Allow LNI to arbitrate write with highest priority over read on port1. lncf_csr_lni_p1_read_priority_dis
	4	LNI Partial Write Fix Disable Access: R/W 0: (Default) Enable fix to disable write on port1 for a partial write. 1: Disable port1 write disable fix for a partial write. lncf_csr_lni_parwrfix_dis
	3	LNE Arbitration Performance Fix Access: R/W 0: (Default) Enable the performance fix for the case where LNE was inserting bubbles in SS read returns . HSD 2121468 1: Disable the performance fix for HSD 2121468 . lncf_csr_lne_perf_fix_dis



SCRATCH_LNCF1 - SCRATCH for LNCUnit

	2	Memory fill delay	
		Access:	R/W
		Incf_csr_Ini_gt2_memfill_dis. 0:mem fills gt2 latency will be 1 . 1:mem fill gt2 latency will be same as gt3.	
	1	flush start delay	
		Access:	R/W
		Incf_csr_Ini_disable_flush_start_delay. 0:Flush processing in LNLunit starts one clock after receiving the flush command default. 1:Flush processing in LNLunit starts in the same clock in which flush command is received.	
	0	Non-IA coherent atomics enable	
		Default Value:	1b
		Access:	R/W
		0: atomics in GTI (). 1: atomics in L3 (non-IA atomic) (Default). Output signal from LNCF unit Incf_csr_Ini_glblatmcs_I3. Value for this bit should be same as lbcf_csr_Isqc_glblatmcs_I3 b118[22]. Value of this bit should be same as LBCF register bit 0xb11c[8]. Adding Xbuf 8 MCP.	



Slice 0 PFET control register with lock

PFETCTL - Slice 0 PFET control register with lock		
Register Space:		MMIO: 0/2/0
Source:		BSpec
Default Value:		0x0007005A
Size (in bits):		32
Address:		24188h
DWord	Bit	Description
0	31	PFET Control Lock
		Access: R/W Lock 0 = Bits of this register are R/W 1 = All bits of this register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	Reserved
		Access: RO Reserved
	20	Power Well Status
	Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
19	Powergood timer error	
	Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
18:16	Delay from enabling secondary PFETs to power good.	
	Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns 3'b010: 160ns 3'b011: 320ns	



PFETCTL - Slice 0 PFET control register with lock

PFETCTL - Slice 0 PFET control register with lock						
		3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns <table><tr><th>Value</th><th>Name</th></tr><tr><td>111b</td><td>[Default]</td></tr></table>	Value	Name	111b	[Default]
Value	Name					
111b	[Default]					
15:13	Time period last primay pfet strobe to secondary pfet strobe <table><tr><td>Access:</td><td>R/W Lock</td></tr></table> Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)		Access:	R/W Lock		
Access:	R/W Lock					
12:10	Time period b/w two adjacent strobes <table><tr><td>Access:</td><td>R/W Lock</td></tr></table> Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)		Access:	R/W Lock		
Access:	R/W Lock					
9:7	FET setup margin from enable to strobe <table><tr><td>Access:</td><td>R/W Lock</td></tr></table> Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)		Access:	R/W Lock		
Access:	R/W Lock					
6:0	Number of flops to enable primary FETs <table><tr><td>Default Value:</td><td>1011010b</td></tr><tr><td>Access:</td><td>R/W Lock</td></tr></table> Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed		Default Value:	1011010b	Access:	R/W Lock
Default Value:	1011010b					
Access:	R/W Lock					



Slice 0 SubSlice 0 PFET control register with lock

PFETCTL - Slice 0 SubSlice 0 PFET control register with lock		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x0007000A	
Size (in bits):	32	
Address:	24408h	
DWord	Bit	Description
0	31	PFET Control Lock
		Access: R/W Lock 0 = Bits of PFETCTL register are R/W 1 = All bits of PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	Reserved
		Access: RO Reserved
	20	Power Well Status
19	Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
	Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
18:16	Delay from enabling secondary PFETs to power good.	
	Default Value: 111b	
	Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns	



PFETCTL - Slice 0 SubSlice 0 PFET control register with lock

		3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
15:13	Time period last primay pfet strobe to secondary pfet strobe	
	Access:	R/W Lock
	Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
12:10	Time period b/w two adjacent strobes	
	Access:	R/W Lock
	Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
9:7	FET setup margin from enable to strobe	
	Access:	R/W Lock
	Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
6:0	Number of flops to enable primary FETs	
	Access:	R/W Lock
	Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed	
	Value	Name
	0001010b	[Default]



Slice 0 SubSlice 1 PFET control register with lock

PFETCTL - Slice 0 SubSlice 1 PFET control register with lock		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x0007000A	
Size (in bits):	32	
Address:	24488h	
DWord	Bit	Description
0	31	PFET Control Lock
		Access: R/W Lock 0 = Bits of Slice 0 PFETCTL register are R/W 1 = All bits of Slice 0 PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	Reserved
		Access: RO Reserved
	20	Power Well Status
19	Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
	Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
18:16	Delay from enabling secondary PFETs to power good.	
	Default Value: 111b	
	Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns	



PFETCTL - Slice 0 SubSlice 1 PFET control register with lock

		3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
15:13	Time period last primay pfet strobe to secondary pfet strobe	
	Access:	R/W Lock
	Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
12:10	Time period b/w two adjacent strobes	
	Access:	R/W Lock
	Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
9:7	FET setup margin from enable to strobe	
	Access:	R/W Lock
	Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
6:0	Number of flops to enable primary FETs	
	Access:	R/W Lock
	Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed	
	Value	Name
	0001010b	[Default]



Slice 0 SubSlice 2 PFET control register with lock

PFETCTL - Slice 0 SubSlice 2 PFET control register with lock		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x0007000A	
Size (in bits):	32	
Address:	24508h	
DWord	Bit	Description
0	31	PFET Control Lock
		Access: R/W Lock 0 = Bits of Slice 0 PFETCTL register are R/W 1 = All bits of Slice 0 PFETCTL register are RO (including this lock bit) Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
	30:21	Reserved
		Access: RO Reserved
	20	Power Well Status
	Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.	
	19	Powergood timer error
		Access: R/WC 0 = Well is powered Down 1 = Well is powered up Once written to 1, the lock is set and cannot be cleared (i.e., writing a 0 will not clear the lock). These bits are not reset on FLR.
		18:16
		Default Value: 111b
		Access: R/W Lock Delay from enabling secondary PFETs to power good 3'b000: 40ns 3'b001: 80ns



PFETCTL - Slice 0 SubSlice 2 PFET control register with lock

		3'b010: 160ns 3'b011: 320ns 3'b100: 640ns 3'b101: 1280ns 3'b110: 2560ns 3'b111: 5120ns
15:13	Time period last primay pfet strobe to secondary pfet strobe	
	Access:	R/W Lock
	Time period last primay pfet strobe to secondary pfet strobe 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
12:10	Time period b/w two adjacent strobes	
	Access:	R/W Lock
	Time period b/w two adjacent strobes to the primary FETs 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
9:7	FET setup margin from enable to strobe	
	Access:	R/W Lock
	Setup margin in design before sampling enable event at the first pre-charge sequencer/shift register flop 3'b000: 10ns (or 1 bclk) 3'b001: 20ns (or 2 bclk) 3'b010: 30ns (or 3 bclk) 3'b111: 80ns (or 8 bclk)	
6:0	Number of flops to enable primary FETs	
	Access:	R/W Lock
	Number of flops to enable primary FETs. For a setting of N there will be N+1 total strobes generated 7'b0000000: 10 Flops to be strobed 7'b0000001: 11 Flops to be strobed 7'b0000010: 12 Flops to be strobed 7'b0001111: 26 Flops to be strobed	
	Value	Name
	0001010b	[Default]



Software SCI

SWSCI_0_2_0_PCI - Software SCI			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	16		
Address:	000E8h		
This register serves 2 purposes: 1) Support selection of SMI or SCI event source (SMISCISEL - bit15) 2) SCI Event trigger (GSSCIE - bit 0). To generate a SW SCI event, software should program bit 15 (SMISCISEL) to 1. This is typically programmed once (assuming SMIs are never triggered). On a "0" to "1" subsequent transition in bit 0 of this register (caused by a software write operation), a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. The corresponding SCI event handler in BIOS is to be defined as a _Lxx method, indicating level trigger to the operating system. Once written as 1, software must write a "0" to this bit to clear it, and all other write transitions (1-0, 0-0, 1-1) will not cause a SCI message to be sent. To generate a SW SMI event, software should program bit 15 to 0 and trigger SMI via writes to SWSMI register (See SWSMI register for programming details).			
DWord	Bit	Description	
0	15	SMI or SCI event select	
		Default Value:	0b
		Access:	R/W
		0 = SMI (default) 1 = SCI If selected event source is SMI, SMI trigger and associated scratch bits accesses are performed via SWSMI register. If SCI event source is selected, the rest of the bits in this register provide SCI trigger capability and associated SW scratch pad area.	
	14:1	Software scratch bits	
		Default Value:	000000000000000b
		Access:	R/W
	Read/write bits not used by hardware.		
	0	Software SCI Event	
Default Value:		0b	
Access:		R/W	
If SCI event is selected (SMISCISEL = 1), on a 0 to 1 transition of GSSCIE bit, a SCI message will be sent to cause the TCOSCI_STS bit in GPE0 register to be set to 1. Software must write a 0 to clear this bit.			



Software SMI

SWSMI_0_2_0_PCI - Software SMI		
Register Space:	PCI: 0/2/0	
Source:	BSpec	
Default Value:	0x00000000	
Size (in bits):	16	
Address:	000E0h	
DWord	Bit	Description
0	15:8	Software Scratch Bits
		Default Value: 00000000b
		Access: R/W
	7:1	Software Flag
		Default Value: 0000000b
		Access: R/W
		Used to indicate caller and SMI function desired, as well as return result.
	0	GMCH Software SMI Event
		Default Value: 0b
		Access: R/W
		When Set this bit will trigger an SMI. Software must write a "0" to clear this bit. SMI will be triggered only if SWSCI[SMISCISEL] is set to select SMI.



Subsystem Identification

SID2_0_2_0_PCI - Subsystem Identification		
Register Space: PCI: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 16		
Address: 0002Eh		
This register is used to uniquely identify the subsystem where the PCI device resides.		
DWord	Bit	Description
0	15:0	Subsystem Identification
		Default Value: 0000000000000000b
		Access: R/W Once
		This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.



Subsystem Vendor Identification

SVID2_0_2_0_PCI - Subsystem Vendor Identification			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	16		
Address:	0002Ch		
This register is used to uniquely identify the subsystem where the PCI device resides.			
DWord	Bit	Description	
0	15:0	Subsystem Vendor ID	
		Default Value:	0000000000000000b
		Access:	R/W Once
		This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read_Only. This register can only be cleared by a Reset.	



Super Queue Internal Cnt Register I

SQCNT1 - Super Queue Internal Cnt Register I				
Register Space:	MMIO: 0/2/0			
Source:	BSpec			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09024h			
SQ Internal Counter Register				
DWord	Bit	Description		
0	31:24	RSVD <table><tr><td>Access:</td><td>RO</td></tr></table>	Access:	RO
	Access:	RO		
	23:20	SQRWCQD <table><tr><td>Access:</td><td>R/W</td></tr></table> Read-Write Request Queue Command Get Delay: This indicates the number of clocks that are inserted between each GFX cycle being accepted on the GFX Read or GFX Write ports. By default, this is disabled, which means that the RWRQ is able to accept one cycle per clock. By any other value, the RWRQ inserts the number of idle clocks listed in this register before accepting another cycle from GFX, essentially throttling the bandwidth. During each idle clock, RWRQ is guaranteed not to assert its command get to either read or write port. 0000b = Disabled (no additional clocks added). 0001b = One idle clock inserted between command gets. 0010b = Two idle clocks inserted between command gets. ... 1111b = Fifteen idle clocks inserted between command gets.	Access:	R/W
Access:	R/W			
19:16	SQCQD <table><tr><td>Access:</td><td>R/W</td></tr></table> Read-Only Request Queue Command Get Delay: This indicates the number of clocks that are inserted between each GFX cycle being accepted on the GFX Read-Only port. By default, this is disabled, which means that the RORQ will be able to accept one cycle per clock. By any other value, the RORQ inserts the number of idle clocks listed in this register before accepting another cycle from GFX, essentially throttling the bandwidth. During each idle clock, RORQ is guaranteed not to assert its command get. 0000b = Disabled (no additional clocks added). 0001b = One idle clock inserted between command gets. 0010b = Two idle clocks inserted between command gets. ... 1111b = Fifteen idle clocks inserted between command gets.	Access:	R/W	
Access:	R/W			



SQCNT1 - Super Queue Internal Cnt Register I

15:9	SQDPTH <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> Super Queue Depth: 7Fh = SQ Depth of 127. 7Eh = SQ Depth of 126. ... 40h = SQ Depth of 64. 3Fh = SQ Depth of 63. 3Eh = SQ Depth of 62. ... 07h = SQ Depth of 7. 06h = SQ Depth of 6. 05h = SQ Depth of 5. 04h = SQ Depth of 4. 03h = SQ Depth of 3. 02h = SQ Depth of 2. 01h = Reserved. 00h = Disabled (SQ Depth of MAX) (default). For the sizes that are larger than the physical SQ size, the depth limitation is treated as disabled. if SQDPTH > 88 for BXT B-step, SQ Depth should be treated as MAX that h/w is capable of. NOTE - FOR BXT-A STEP, REGISTER DESCRIPTION IS SIMILAR TO SKL DESCRIPTION. THIS FIELD IS ONLY ACCURATE FOR BXT-B STEP AND BEYOND.	Access:	R/W
Access:	R/W		
8	RSVD <table border="1"> <tr> <td>Access:</td><td>RO</td></tr> </table>	Access:	RO
Access:	RO		
7	Reserved		
6:0	SQIDICNT <table border="1"> <tr> <td>Access:</td><td>R/W</td></tr> </table> Outstanding SQ IDI Cycle Counter: This indicates the maximum number of outstanding cycles that are presented to IDI/uncore at any given time by Super Queue. By default, this is MAX, but can be throttled back to support fewer IDI cycles. 0 = Disabled (MAX). 1-127 = Max number of outstanding IDI cycles. For the sizes that are larger than the physical SQ size, the depth limitation is treated as disabled. (i.e. if SQIDICNT is greater than 88 for BXT B-step, SQ IDI limitation should be treated as MAX that h/w is capable of). NOTE - FOR BXT-A STEP, REGISTER DESCRIPTION IS SIMILAR TO SKL DESCRIPTION. THIS FIELD IS ONLY ACCURATE FOR BXT-B STEP AND BEYOND.	Access:	R/W
Access:	R/W		



TILECTL

TILECTL - TILECTL		
Register Space: MMIO: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 101000h		
Tile control and TLB control.		
DWord	Bit	Description
0	31:3	Reserved
		Default Value: 00000000h
		Access: RO
		Reserved
	2	Reserved
		Default Value: 0b
		Access: RO
		Reserved.
	1	TLBPF
		Default Value: 0b
		Access: R/W
		Store multiple PTE enable. This bit must be set to 1 for BXT A0 0: Only one Page Table Entry is stored in the Translation Lookaside Buffer cache. 1: Multiple Page Table Entries (8) are stored in the Translation Lookaside Buffer cache.
	0	SWZCTL
		Default Value: 0b
		Access: R/W
		In order to spread DRAM accesses between multiple channels in the most efficient way, address bits can be used as a channel select. The Driver needs to obtain the need for memory address swizzling via DRAM configuration registers and set the following bits. x0b - No Address Swizzling x1b - Address bit [6] needs to be swizzled for tiled surfaces



Top Of Low Usable DRAM

TOLUD_0_0_0_PCI - Top Of Low Usable DRAM			
Register Space:	PCI: 0/0/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	000BCh		
This 32 bit register defines the low usable DRAM.			
DWord	Bit	Description	
0	31:20	TOLUD	
		Default Value:	000000000000b
		Access:	R/W Lock
		This register contains bits 31 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system. The top of low usable DRAM is the lowest address above both graphics stolen memory and Tseg.	
	19:1	RESERVED	
		Default Value:	000b
		Access:	RO
	Reserved		
	0	Lock	
		Default Value:	0b
Access:		R/W Key Lock	
This bit will lock all writeable settings in this register, including itself.			



Top Of Upper Usable DRAM

TOUUD_0_0_0_PCI - Top Of Upper Usable DRAM			
Register Space:		PCI: 0/0/0	
Source:		BSpec	
Default Value:		0x00000000, 0x00000000	
Size (in bits):		64	
Address:		000A8h	
This 64 bit register defines the top of upper usable DRAM.			
DWord	Bit	Description	
0	63:39	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	38:20	TOUUD	
		Default Value:	0000000000000000000b
		Access:	R/W Lock
		This register contains bits 38 to 20 of an address one byte above the maximum DRAM memory above 4G that is usable by the operating system.	
	19:1	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	0	Lock	
		Default Value:	0b
		Access:	R/W Key Lock
		This bit will lock all writeable settings in this register, including itself.	



TSEG Base Memory

TSEGMB_0_0_0_PCI - TSEG Base Memory			
Register Space:	PCI: 0/0/0		
Source:	BSpec		
Default Value:	0x00000000		
Size (in bits):	32		
Address:	000B8h		
This 32 bit register defines the TSEG Base.			
DWord	Bit	Description	
0	31:20	TSEG Memory Base	
		Default Value:	000000000000b
		Access:	R/W Lock
		This register contains the base address of TSEG DRAM memory. BIOS determines the base of TSEG memory which must be at or below Graphics Base of GTT Stolen Memory (PCI Device 0 Offset B4 bits 31:20). Bios must program the value of TSEGMB to be the same as BGSM when TSEG is disabled.	
	19:1	RESERVED	
		Default Value:	000b
		Access:	RO
	Reserved		
	0	Lock	
		Default Value:	0b
Access:		R/W Key Lock	
This bit will lock all writeable settings in this register, including itself.			



Unit Level Clock Gating Control 2

UCGCTL2 - Unit Level Clock Gating Control 2				
Register Space:	MMIO: 0/2/0			
Source:	BSpec			
Default Value:	0x00000000			
Size (in bits):	32			
Address:	09404h			
Unit Level Clock Gating Control Registers.				
DWord	Bit	Description		
0	31	VFunit Clock Gating Disable <table><tr><td>Access:</td><td>R/W</td></tr></table> VFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
	Access:	R/W		
	30	VDSunit Clock Gating Disable <table><tr><td>Access:</td><td>R/W</td></tr></table> VDSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
	Access:	R/W		
	29	VDIunit Clock Gating Disable <table><tr><td>Access:</td><td>R/W</td></tr></table> VDIunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
Access:	R/W			
28	VCSunit Clock Gating Disable <table><tr><td>Access:</td><td>R/W</td></tr></table> VCSunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W	
Access:	R/W			
27	DTOnit Clock Gating Disable <table><tr><td>Access:</td><td>R/W</td></tr></table> DTOnit Clock Gating Disable Control:	Access:	R/W	
Access:	R/W			



UCGCTL2 - Unit Level Clock Gating Control 2

		'0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
26	VCPunit Clock Gating Disable	<table><tr><td>Access:</td><td>R/W</td></tr></table> VCPunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
Access:	R/W			
25	VCDunit Clock Gating Disable	<table><tr><td>Access:</td><td>R/W</td></tr></table> VCDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
Access:	R/W			
24	URBMunit Clock Gating Disable	<table><tr><td>Access:</td><td>R/W</td></tr></table> URBMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
Access:	R/W			
23	TSGunit Clock Gating Disable	<table><tr><td>Access:</td><td>R/W</td></tr></table> TSGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
Access:	R/W			
22	TDLunit Clock Gating Disable	<table><tr><td>Access:</td><td>R/W</td></tr></table> TDLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
Access:	R/W			
21	TDSunit Clock Gating Disable	<table><tr><td>Access:</td><td>R/W</td></tr></table> TDSunit Clock Gating Disable Control:	Access:	R/W
Access:	R/W			



UCGCTL2 - Unit Level Clock Gating Control 2

	'0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always) Programming note: To work around a clock gating issue for A0-D0, the clock gating disable must be set to a 1 unless the offset h229c bit 11, Replay Mode, is set to 0, mid-cmdbuffer preemption Clock gating on tdsunit cannot be disabled or set to 1		
20	SVSMunit Clock Gating Disable <table><tr><td>Access:</td><td>R/W</td></tr></table> SVSMunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
Access:	R/W		
19	SVGunit Clock Gating Disable <table><tr><td>Access:</td><td>R/W</td></tr></table> SVGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
Access:	R/W		
18	SOunit Clock Gating Disable <table><tr><td>Access:</td><td>R/W</td></tr></table> SOunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
Access:	R/W		
17	Slunit Clock Gating Disable <table><tr><td>Access:</td><td>R/W</td></tr></table> Slunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
Access:	R/W		
16	SFunit Clock Gating Disable <table><tr><td>Access:</td><td>R/W</td></tr></table> SFunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	Access:	R/W
Access:	R/W		
15	SECunit Clock Gating Disable		



UCGCTL2 - Unit Level Clock Gating Control 2

		Access:	R/W
		SECunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	
14	SCunit Clock Gating Disable	Access:	R/W
		SCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	
13	RCZunit Clock Gating Disable	Access:	R/W
		RCZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	
12	RCPBunit Clock Gating Disable	Access:	R/W
		RCPBunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	
11	RCCunit Clock Gating Disable	Access:	R/W
		RCCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	
10	QCunit Clock Gating Disable	Access:	R/W
		QCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	



UCGCTL2 - Unit Level Clock Gating Control 2

UCGCTL2 - Unit Level Clock Gating Control 2		
	9	PSDunit Clock Gating Disable Access: R/W PSDunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	PLunit Clock Gating Disable Access: R/W PLunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	MTunit Clock Gating Disable Access: R/W MTunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	6	MPCunit Clock Gating Disable Access: R/W MPCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	5	TDGunitClock Gating Disable Access: R/W TDGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	MSCunit Clock Gating Disable Access: R/W MSCunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)



UCGCTL2 - Unit Level Clock Gating Control 2

UCGCTL2 - Unit Level Clock Gating Control 2								
	3	<table><tr><td colspan="2">TEunit Clock Gating Disable</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">TEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)</td></tr></table>	TEunit Clock Gating Disable		Access:	R/W	TEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	
	TEunit Clock Gating Disable							
	Access:	R/W						
	TEunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)							
2	<table><tr><td colspan="2">TETGunit Clock Gating Disable</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">TETGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)</td></tr></table>	TETGunit Clock Gating Disable		Access:	R/W	TETGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
TETGunit Clock Gating Disable								
Access:	R/W							
TETGunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)								
1	<table><tr><td colspan="2">MAunit Clock Gating Disable</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">MAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)</td></tr></table>	MAunit Clock Gating Disable		Access:	R/W	MAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
MAunit Clock Gating Disable								
Access:	R/W							
MAunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)								
0	<table><tr><td colspan="2">IZunit Clock Gating Disable</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)</td></tr></table>	IZunit Clock Gating Disable		Access:	R/W	IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
IZunit Clock Gating Disable								
Access:	R/W							
IZunit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)								



Unit Level Clock Gating Control 6

UCGCTL6 - Unit Level Clock Gating Control 6		
Register Space:		MMIO: 0/2/0
Source:		BSpec
Default Value:		0x00000000
Size (in bits):		32
Address:		09430h
Unit Level Clock Gating Disable bits		
DWord	Bit	Description
0	31	SPARE 3 clock gate disable
		Access: R/W SPARE 3 unit Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	30:28	HDCunit clock gate disable
		Access: R/W HDC units Clock Gating Disable Control: HDCREQ bit 28, HDCRET bit 29, HDCTLB bit 30. '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
Programming Notes		
3x6: Bit 28 (HDCREQ) must be set to disable clock gating.		
27	MUCunit clock gate disable	
	Access: R/W MUC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	
26	GACVunit cuclk gate disable	
	Access: R/W GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)	



UCGCTL6 - Unit Level Clock Gating Control 6

	25	GACBunit clock gate disable	Access:	R/W
		GACB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
	24	GAPSunit clock gate disable	Access:	R/W
		GAPS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
	23	GAMTunit clock gate disable	Access:	R/W
		GAMT units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
	22	Reserved		
	21	OASCREP	Access:	R/W
		OASCREP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
	20	OAADDRunit clock gate disable bit	Access:	R/W
		OAADDR units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
	19	GACVunit clock gate disable	Access:	R/W
		GACV units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality)		



UCGCTL6 - Unit Level Clock Gating Control 6

	'1' : Clock Gating Disabled. (that is, clocks are toggling, always)	
18	BDMunit clock gate disable	
	Access:	R/W
BDM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
17	GATSunit clock gate disable	
	Access:	R/W
GATS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
16	OATREPunit clock gate disable	
	Access:	R/W
OATREP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
15	STunit clock gate disable	
	Access:	R/W
ST units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
14	SDEunit clock gate disable	
	Access:	R/W
SDE units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		
13	VIN(VID6) unit clock gate disable	
	Access:	R/W
VIN(VID6) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)		



UCGCTL6 - Unit Level Clock Gating Control 6

	12	VIN(VID5) unit clock gate disable
		Access: R/W
		VIN(VID5) units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	11	WVOPunit clock gate disable
		Access: R/W
		WVOP units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	10	WUSB unit clock gate disable
		Access: R/W
		WUSB units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	9	WSECunit clock gate disable
		Access: R/W
		WSEC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	8	WRSunit clcok gate disable
		Access: R/W
		WRS units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	7	WQRCunit clock gate disable
		Access: R/W
		WQRC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)



UCGCTL6 - Unit Level Clock Gating Control 6

	6	WMPC unit level clock gate disable Access: R/W WMPC units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	5	WINunit Clock gate disable Access: R/W WIN units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	4	WIME unit clock gate disable Access: R/W WIME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	3	WHME unit clock gate disable Access: R/W WHME units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	2	WAVMunit Clock Gate Disable Access: R/W WAVM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)
	1	VSHMunit clock gate disable Access: R/W VSHM units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)



UCGCTL6 - Unit Level Clock Gating Control 6		
	0	VSLunit Clock gating disable Access: R/W VSL units Clock Gating Disable Control: '0' : Clock Gating Enabled. (that is, clocks can be gated when they are not required to toggle for functionality) '1' : Clock Gating Disabled. (that is, clocks are toggling, always)



VEBOX MOCS Register0

VEBOX_MOCS_0 - VEBOX MOCS Register0			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000030	
Size (in bits):		32	
Address:		0CB00h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_0 - VEBOX MOCS Register0

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_0 - VEBOX MOCS Register0**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register1

VEBOX_MOCS_1 - VEBOX MOCS Register1			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000034		
Size (in bits):	32		
Address:	0CB04h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_1 - VEBOX MOCS Register1**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_1 - VEBOX MOCS Register1		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register2

VEBOX_MOCS_2 - VEBOX MOCS Register2			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000038	
Size (in bits):		32	
Address:		0CB08h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_2 - VEBOX MOCS Register2

VEBOX_MOCS_2 - VEBOX MOCS Register2		
		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching	
	Default Value:	0b
	Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
6	Dont allocate on miss	
	Default Value:	0b
	Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
5:4	LRU management	
	Default Value:	11b
	Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
3:2	Target Cache	
	Default Value:	10b
	Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	

**VEBOX_MOCS_2 - VEBOX MOCS Register2**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register3

VEBOX_MOCS_3 - VEBOX MOCS Register3			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000031	
Size (in bits):		32	
Address:		0CB0Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_3 - VEBOX MOCS Register3**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_3 - VEBOX MOCS Register3		
	1:0	LLC/eDRAM cacheability control
		Default Value: 01b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register4

VEBOX_MOCS_4 - VEBOX MOCS Register4			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0CB10h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_4 - VEBOX MOCS Register4

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_4 - VEBOX MOCS Register4		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register5

VEBOX_MOCS_5 - VEBOX MOCS Register5			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0CB14h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**VEBOX_MOCS_5 - VEBOX MOCS Register5**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_5 - VEBOX MOCS Register5		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register6

VEBOX_MOCS_6 - VEBOX MOCS Register6			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CB18h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_6 - VEBOX MOCS Register6

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_6 - VEBOX MOCS Register6		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register7

VEBOX_MOCS_7 - VEBOX MOCS Register7			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000033			
Size (in bits): 32			
Address: 0CB1Ch			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_7 - VEBOX MOCS Register7**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_7 - VEBOX MOCS Register7		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register8

VEBOX_MOCS_8 - VEBOX MOCS Register8			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000037	
Size (in bits):		32	
Address:		0CB20h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_8 - VEBOX MOCS Register8

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_8 - VEBOX MOCS Register8**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register9

VEBOX_MOCS_9 - VEBOX MOCS Register9			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003B		
Size (in bits):	32		
Address:	0CB24h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**VEBOX_MOCS_9 - VEBOX MOCS Register9**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_9 - VEBOX MOCS Register9		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register10

VEBOX_MOCS_10 - VEBOX MOCS Register10			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0CB28h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_10 - VEBOX MOCS Register10

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_10 - VEBOX MOCS Register10**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register11

VEBOX_MOCS_11 - VEBOX MOCS Register11			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000036			
Size (in bits): 32			
Address: 0CB2Ch			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_11 - VEBOX MOCS Register11**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_11 - VEBOX MOCS Register11		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register12

VEBOX_MOCS_12 - VEBOX MOCS Register12			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0CB30h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_12 - VEBOX MOCS Register12

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_12 - VEBOX MOCS Register12**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register13

VEBOX_MOCS_13 - VEBOX MOCS Register13			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000033			
Size (in bits): 32			
Address: 0CB34h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_13 - VEBOX MOCS Register13**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_13 - VEBOX MOCS Register13		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register14

VEBOX_MOCS_14 - VEBOX MOCS Register14			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000037	
Size (in bits):		32	
Address:		0CB38h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
Access:		R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
10:8	Skip Caching control		
	Default Value:	000b	
	Access:	R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_14 - VEBOX MOCS Register14

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_14 - VEBOX MOCS Register14**

1:0

LLC/eDRAM cacheability control

Default Value:

11b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



VEBOX MOCS Register15

VEBOX_MOCS_15 - VEBOX MOCS Register15			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x0000003B			
Size (in bits): 32			
Address: 0CB3Ch			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_15 - VEBOX MOCS Register15**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_15 - VEBOX MOCS Register15		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register16

VEBOX_MOCS_16 - VEBOX MOCS Register16			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000030	
Size (in bits):		32	
Address:		0CB40h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_16 - VEBOX MOCS Register16

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_16 - VEBOX MOCS Register16**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register17

VEBOX_MOCS_17 - VEBOX MOCS Register17			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000034			
Size (in bits): 32			
Address: 0CB44h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_17 - VEBOX MOCS Register17**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_17 - VEBOX MOCS Register17		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register18

VEBOX_MOCS_18 - VEBOX MOCS Register18			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000038	
Size (in bits):		32	
Address:		0CB48h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
Default Value:		000b	
Access:		R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
10:8	Skip Caching control		
	Default Value:	000b	
	Access:	R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_18 - VEBOX MOCS Register18

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_18 - VEBOX MOCS Register18**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register19

VEBOX_MOCS_19 - VEBOX MOCS Register19			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000031		
Size (in bits):	32		
Address:	0CB4Ch		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_19 - VEBOX MOCS Register19**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching	Default Value:	0b
		Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss	Default Value:	0b
		Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management	Default Value:	11b
		Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache	Default Value:	00b
		Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_19 - VEBOX MOCS Register19		
	1:0	LLC/eDRAM cacheability control
		Default Value: 01b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register20

VEBOX_MOCS_20 - VEBOX MOCS Register20			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0CB50h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_20 - VEBOX MOCS Register20

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_20 - VEBOX MOCS Register20**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register21

VEBOX_MOCS_21 - VEBOX MOCS Register21			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0CB54h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_21 - VEBOX MOCS Register21**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching	Default Value:	0b
		Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss	Default Value:	0b
		Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management	Default Value:	11b
		Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache	Default Value:	01b
		Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_21 - VEBOX MOCS Register21		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register22

VEBOX_MOCS_22 - VEBOX MOCS Register22			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0CB58h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_22 - VEBOX MOCS Register22

	Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	Default Value:	11b	Access:	R/W
Default Value:	11b				
Access:	R/W				
3:2	Target Cache <table><tr><td>Default Value:</td><td>10b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	Default Value:	10b	Access:	R/W
Default Value:	10b				
Access:	R/W				

**VEBOX_MOCS_22 - VEBOX MOCS Register22**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register23

VEBOX_MOCS_23 - VEBOX MOCS Register23			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CB5Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_23 - VEBOX MOCS Register23**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_23 - VEBOX MOCS Register23		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register24

VEBOX_MOCS_24 - VEBOX MOCS Register24			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000037	
Size (in bits):		32	
Address:		0CB60h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_24 - VEBOX MOCS Register24

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_24 - VEBOX MOCS Register24		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register25

VEBOX_MOCS_25 - VEBOX MOCS Register25			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x0000003B			
Size (in bits): 32			
Address: 0CB64h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_25 - VEBOX MOCS Register25**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_25 - VEBOX MOCS Register25		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register26

VEBOX_MOCS_26 - VEBOX MOCS Register26			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000032	
Size (in bits):		32	
Address:		0CB68h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_26 - VEBOX MOCS Register26

	Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	Default Value:	0b	Access:	R/W
Default Value:	0b				
Access:	R/W				
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	Default Value:	11b	Access:	R/W
Default Value:	11b				
Access:	R/W				
3:2	Target Cache <table><tr><td>Default Value:</td><td>00b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	Default Value:	00b	Access:	R/W
Default Value:	00b				
Access:	R/W				



VEBOX_MOCS_26 - VEBOX MOCS Register26		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register27

VEBOX_MOCS_27 - VEBOX MOCS Register27			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CB6Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_27 - VEBOX MOCS Register27**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_27 - VEBOX MOCS Register27		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register28

VEBOX_MOCS_28 - VEBOX MOCS Register28			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003A	
Size (in bits):		32	
Address:		0CB70h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
Default Value:		000b	
Access:		R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
10:8	Skip Caching control		
	Default Value:	000b	
	Access:	R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_28 - VEBOX MOCS Register28

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_28 - VEBOX MOCS Register28**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register29

VEBOX_MOCS_29 - VEBOX MOCS Register29			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000033		
Size (in bits):	32		
Address:	0CB74h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_29 - VEBOX MOCS Register29**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching	Default Value:	0b
		Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss	Default Value:	0b
		Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management	Default Value:	11b
		Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache	Default Value:	00b
		Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX MOCS Register30

VEBOX_MOCS_30 - VEBOX MOCS Register30			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000037			
Size (in bits): 32			
Address: 0CB78h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_30 - VEBOX MOCS Register30**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_30 - VEBOX MOCS Register30		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register31

VEBOX_MOCS_31 - VEBOX MOCS Register31			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CB7Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_31 - VEBOX MOCS Register31

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_31 - VEBOX MOCS Register31**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register32

VEBOX_MOCS_32 - VEBOX MOCS Register32			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000030		
Size (in bits):	32		
Address:	0CB80h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_32 - VEBOX MOCS Register32**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_32 - VEBOX MOCS Register32		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register33

VEBOX_MOCS_33 - VEBOX MOCS Register33			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000034		
Size (in bits):	32		
Address:	0CB84h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_33 - VEBOX MOCS Register33

	Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target								
7	<table><tr><td colspan="2">Enable Skip Caching</td></tr><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC</td></tr></table>	Enable Skip Caching		Default Value:	0b	Access:	R/W	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
Enable Skip Caching									
Default Value:	0b								
Access:	R/W								
Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC									
6	<table><tr><td colspan="2">Dont allocate on miss</td></tr><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS</td></tr></table>	Dont allocate on miss		Default Value:	0b	Access:	R/W	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
Dont allocate on miss									
Default Value:	0b								
Access:	R/W								
Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS									
5:4	<table><tr><td colspan="2">LRU management</td></tr><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved</td></tr></table>	LRU management		Default Value:	11b	Access:	R/W	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
LRU management									
Default Value:	11b								
Access:	R/W								
This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved									
3:2	<table><tr><td colspan="2">Target Cache</td></tr><tr><td>Default Value:</td><td>01b</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed</td></tr></table>	Target Cache		Default Value:	01b	Access:	R/W	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
Target Cache									
Default Value:	01b								
Access:	R/W								
This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed									

**VEBOX_MOCS_33 - VEBOX MOCS Register33**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	00b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register34

VEBOX_MOCS_34 - VEBOX MOCS Register34			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000038			
Size (in bits): 32			
Address: 0CB88h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_34 - VEBOX MOCS Register34**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_34 - VEBOX MOCS Register34		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register35

VEBOX_MOCS_35 - VEBOX MOCS Register35			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000031	
Size (in bits):		32	
Address:		0CB8Ch	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_35 - VEBOX MOCS Register35

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_35 - VEBOX MOCS Register35**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	01b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register36

VEBOX_MOCS_36 - VEBOX MOCS Register36			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0CB90h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_36 - VEBOX MOCS Register36**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_36 - VEBOX MOCS Register36		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register37

VEBOX_MOCS_37 - VEBOX MOCS Register37			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000036		
Size (in bits):	32		
Address:	0CB94h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_37 - VEBOX MOCS Register37

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_37 - VEBOX MOCS Register37**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register38

VEBOX_MOCS_38 - VEBOX MOCS Register38			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CB98h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_38 - VEBOX MOCS Register38**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_38 - VEBOX MOCS Register38		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register39

VEBOX_MOCS_39 - VEBOX MOCS Register39			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000033			
Size (in bits): 32			
Address: 0CB9Ch			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_39 - VEBOX MOCS Register39

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_39 - VEBOX MOCS Register39		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register40

VEBOX_MOCS_40 - VEBOX MOCS Register40			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000037			
Size (in bits): 32			
Address: 0CBA0h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_40 - VEBOX MOCS Register40**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_40 - VEBOX MOCS Register40		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register41

VEBOX_MOCS_41 - VEBOX MOCS Register41			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CBA4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
Access:		R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
10:8	Skip Caching control		
	Default Value:	000b	
	Access:	R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		



VEBOX_MOCS_41 - VEBOX MOCS Register41

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target				
7	Enable Skip Caching <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
6	Dont allocate on miss <table><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		Default Value:	0b	Access:	R/W
Default Value:	0b					
Access:	R/W					
5:4	LRU management <table><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		Default Value:	11b	Access:	R/W
Default Value:	11b					
Access:	R/W					
3:2	Target Cache <table><tr><td>Default Value:</td><td>10b</td></tr><tr><td>Access:</td><td>R/W</td></tr></table> This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		Default Value:	10b	Access:	R/W
Default Value:	10b					
Access:	R/W					

**VEBOX_MOCS_41 - VEBOX MOCS Register41**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register42

VEBOX_MOCS_42 - VEBOX MOCS Register42			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000032			
Size (in bits): 32			
Address: 0CBA8h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_42 - VEBOX MOCS Register42**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_42 - VEBOX MOCS Register42		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register43

VEBOX_MOCS_43 - VEBOX MOCS Register43			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CBACH	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_43 - VEBOX MOCS Register43

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_43 - VEBOX MOCS Register43**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register44

VEBOX_MOCS_44 - VEBOX MOCS Register44			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CBB0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_44 - VEBOX MOCS Register44**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_44 - VEBOX MOCS Register44		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register45

VEBOX_MOCS_45 - VEBOX MOCS Register45			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000033	
Size (in bits):		32	
Address:		0CBB4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_45 - VEBOX MOCS Register45

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_45 - VEBOX MOCS Register45**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register46

VEBOX_MOCS_46 - VEBOX MOCS Register46			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000037			
Size (in bits): 32			
Address: 0CBB8h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**VEBOX_MOCS_46 - VEBOX MOCS Register46**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching	Default Value:	0b
		Access:	R/W
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss	Default Value:	0b
		Access:	R/W
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management	Default Value:	11b
		Access:	R/W
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache	Default Value:	01b
		Access:	R/W
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_46 - VEBOX MOCS Register46		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register47

VEBOX_MOCS_47 - VEBOX MOCS Register47			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CBBCh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_47 - VEBOX MOCS Register47

	Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	Dont allocate on miss Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	LRU management Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	Target Cache Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

**VEBOX_MOCS_47 - VEBOX MOCS Register47**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register48

VEBOX_MOCS_48 - VEBOX MOCS Register48			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000030			
Size (in bits): 32			
Address: 0CBC0h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_48 - VEBOX MOCS Register48**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_48 - VEBOX MOCS Register48		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register49

VEBOX_MOCS_49 - VEBOX MOCS Register49			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000034	
Size (in bits):		32	
Address:		0CBC4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_49 - VEBOX MOCS Register49

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_49 - VEBOX MOCS Register49**

1:0

LLC/eDRAM cacheability control

Default Value:

00b

Access:

R/W

Memory type information used in LLC/eDRAM.

00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle)

01: Uncacheable (UC) - non-cacheable

10: Writethrough (WT)

11: Writeback (WB)



VEBOX MOCS Register50

VEBOX_MOCS_50 - VEBOX MOCS Register50			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000038			
Size (in bits): 32			
Address: 0CBC8h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**VEBOX_MOCS_50 - VEBOX MOCS Register50**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_50 - VEBOX MOCS Register50		
	1:0	LLC/eDRAM cacheability control
		Default Value: 00b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register51

VEBOX_MOCS_51 - VEBOX MOCS Register51			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000031	
Size (in bits):		32	
Address:		0CBCCh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_51 - VEBOX MOCS Register51

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_51 - VEBOX MOCS Register51**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	01b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register52

VEBOX_MOCS_52 - VEBOX MOCS Register52			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0CBD0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_52 - VEBOX MOCS Register52**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_52 - VEBOX MOCS Register52		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register53

VEBOX_MOCS_53 - VEBOX MOCS Register53			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x00000036			
Size (in bits): 32			
Address: 0CBD4h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_53 - VEBOX MOCS Register53

	Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target								
7	<table><tr><td colspan="2">Enable Skip Caching</td></tr><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC</td></tr></table>	Enable Skip Caching		Default Value:	0b	Access:	R/W	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC	
Enable Skip Caching									
Default Value:	0b								
Access:	R/W								
Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC									
6	<table><tr><td colspan="2">Dont allocate on miss</td></tr><tr><td>Default Value:</td><td>0b</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS</td></tr></table>	Dont allocate on miss		Default Value:	0b	Access:	R/W	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS	
Dont allocate on miss									
Default Value:	0b								
Access:	R/W								
Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS									
5:4	<table><tr><td colspan="2">LRU management</td></tr><tr><td>Default Value:</td><td>11b</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved</td></tr></table>	LRU management		Default Value:	11b	Access:	R/W	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved	
LRU management									
Default Value:	11b								
Access:	R/W								
This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved									
3:2	<table><tr><td colspan="2">Target Cache</td></tr><tr><td>Default Value:</td><td>01b</td></tr><tr><td>Access:</td><td>R/W</td></tr><tr><td colspan="2">This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed</td></tr></table>	Target Cache		Default Value:	01b	Access:	R/W	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed	
Target Cache									
Default Value:	01b								
Access:	R/W								
This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed									

**VEBOX_MOCS_53 - VEBOX MOCS Register53**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	10b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register54

VEBOX_MOCS_54 - VEBOX MOCS Register54			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x0000003A		
Size (in bits):	32		
Address:	0CBD8h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_54 - VEBOX MOCS Register54**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_54 - VEBOX MOCS Register54		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register55

VEBOX_MOCS_55 - VEBOX MOCS Register55				
Register Space:		MMIO: 0/2/0		
Source:		BSpec		
Default Value:		0x00000033		
Size (in bits):		32		
Address:		0CBDCh		
MOCS register				
DWord	Bit	Description		
0	31:15	Reserved		
		Default Value:	0000000000000000b	
		Access:	RO	
	14	Snoop Control Field		
		Default Value:	0b	
		Access:	R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms		
		13:11	Page Faulting Mode	
			Default Value:	000b
			Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
		10:8	Skip Caching control	
			Default Value:	000b
	Access:		R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care			



VEBOX_MOCS_55 - VEBOX MOCS Register55

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_55 - VEBOX MOCS Register55**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register56

VEBOX_MOCS_56 - VEBOX MOCS Register56			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0CBE0h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_56 - VEBOX MOCS Register56**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_56 - VEBOX MOCS Register56		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register57

VEBOX_MOCS_57 - VEBOX MOCS Register57			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CBE4h	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_57 - VEBOX MOCS Register57

	Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target
7	Enable Skip Caching Default Value: 0b Access: R/W Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC
6	Dont allocate on miss Default Value: 0b Access: R/W Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS
5:4	LRU management Default Value: 11b Access: R/W This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved
3:2	Target Cache Default Value: 10b Access: R/W This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed

**VEBOX_MOCS_57 - VEBOX MOCS Register57**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



VEBOX MOCS Register58

VEBOX_MOCS_58 - VEBOX MOCS Register58			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000032		
Size (in bits):	32		
Address:	0CBE8h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_58 - VEBOX MOCS Register58**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_58 - VEBOX MOCS Register58		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register59

VEBOX_MOCS_59 - VEBOX MOCS Register59			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x00000036	
Size (in bits):		32	
Address:		0CBECh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_59 - VEBOX MOCS Register59

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_59 - VEBOX MOCS Register59		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register60

VEBOX_MOCS_60 - VEBOX MOCS Register60			
Register Space: MMIO: 0/2/0			
Source: BSpec			
Default Value: 0x0000003A			
Size (in bits): 32			
Address: 0CBF0h			
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value: 0000000000000000b	
		Access: RO	
	14	Snoop Control Field	
		Default Value: 0b	
		Access: R/W	
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value: 000b	
		Access: R/W	
	This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved		
	10:8	Skip Caching control	
		Default Value: 000b	
		Access: R/W	
	Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care		

**VEBOX_MOCS_60 - VEBOX MOCS Register60**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_60 - VEBOX MOCS Register60		
	1:0	LLC/eDRAM cacheability control
		Default Value: 10b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register61

VEBOX_MOCS_61 - VEBOX MOCS Register61			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000033		
Size (in bits):	32		
Address:	0CBF4h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_61 - VEBOX MOCS Register61

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	00b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_61 - VEBOX MOCS Register61		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register62

VEBOX_MOCS_62 - VEBOX MOCS Register62			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000037		
Size (in bits):	32		
Address:	0CBF8h		
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	

**VEBOX_MOCS_62 - VEBOX MOCS Register62**

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITS, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	01b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		



VEBOX_MOCS_62 - VEBOX MOCS Register62		
	1:0	LLC/eDRAM cacheability control
		Default Value: 11b
		Access: R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)



VEBOX MOCS Register63

VEBOX_MOCS_63 - VEBOX MOCS Register63			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x0000003B	
Size (in bits):		32	
Address:		0CBFCh	
MOCS register			
DWord	Bit	Description	
0	31:15	Reserved	
		Default Value:	0000000000000000b
		Access:	RO
	14	Snoop Control Field	
		Default Value:	0b
		Access:	R/W
		Enables s/w to have GFX h/w to be able to consume IA generated buffers that are tagged as WB. Driver can mark these buffers as WB when generating them from IA In LP-SOCs, the fabric is not forced to be coherent all the time. IA-core generated WB buffers can only be consumed by GPU if that buffer is tagged as snoop-able in GPUs buffer definitions (or via GPU Page tables) 1: Hardware will snoop the IA caches while accessing this surface 0: Hardware will not snoop the IA caches while accessing this surface Note: There is a performance and power penalty in accessing surfaces that are tagged as snooped Note: S/W should NOT set this field in client platforms	
	13:11	Page Faulting Mode	
		Default Value:	000b
		Access:	R/W
		This fields controls the page faulting mode that will be used in the memory interface block for the given request coming from this surface: 000: Use the global page faulting mode from context descriptor (default) 001-111: Reserved	
	10:8	Skip Caching control	
		Default Value:	000b
		Access:	R/W
		Defines the bit values to enable caching. Outcome overrides the LLC caching for the surface. If "0" - than corresponding address bit value is don't care	



VEBOX_MOCS_63 - VEBOX MOCS Register63

		Bit[8]=1: address bit[9] needs to be "0" to cache in target Bit[9]=1: address bit[10] needs to be "0" to cache in target Bit[10]=1: address bit[11] needs to be "0" to cache in target	
7	Enable Skip Caching		
	Default Value:	0b	
	Access:	R/W	
	Enable for the Skip cache mechanism 0: Not enabled 1: Enabled for LLC		
6	Dont allocate on miss		
	Default Value:	0b	
	Access:	R/W	
	Controls defined for RO surfaces in mind, where if the target cache is missed - don't bring the line (applicable to LLC/eDRAM). 0: Allocate on MISS (normal cache behavior) 1: Do NOT allocate on MISS		
5:4	LRU management		
	Default Value:	11b	
	Access:	R/W	
	This field allows the selection of AGE parameter for a given surface in LLC or eLLC. . If a particular allocation is done at youngest age 3 it tends to stay longer in the cache as compared to older age allocations - 2, 1 or 0. This option is given to driver to be able to decide which surfaces are more likely to generate HITs, hence need to be replaced least often in caches. 11: Good chance of generating hits. 10: Poor chance of generating hits 01: Don't change the LRU if it is a HIT 00: Reserved		
3:2	Target Cache		
	Default Value:	10b	
	Access:	R/W	
	This field allows the choice of LLC vs eLLC for caching 00: eLLC Only 01: LLC Only 10: LLC/eLLC Allowed 11: LLC/eLLC Allowed		

**VEBOX_MOCS_63 - VEBOX MOCS Register63**

	1:0	LLC/eDRAM cacheability control	
		Default Value:	11b
		Access:	R/W
		Memory type information used in LLC/eDRAM. 00: Use Cacheability Controls from page table / UC with Fence (if coherent cycle) 01: Uncacheable (UC) - non-cacheable 10: Writethrough (WT) 11: Writeback (WB)	



Vendor Identification

VID2_0_2_0_PCI - Vendor Identification			
Register Space:	PCI: 0/2/0		
Source:	BSpec		
Default Value:	0x00008086		
Size (in bits):	16		
Address:	00000h		
This register combined with the Device Identification register uniquely identifies any PCI device.			
DWord	Bit	Description	
0	15:0	Vendor Identification Number	
		Default Value:	1000000010000110b
		Access:	RO
		PCI standard identification for Intel.	



VGA_CONTROL

VGA_CONTROL								
Register Space:	MMIO: 0/2/0							
Source:	BSpec							
Default Value:	0x80000000							
Access:	R/W							
Size (in bits):	32							
Address:	41000h-41003h							
Name:	VGA Control							
ShortName:	VGA_CONTROL							
Power:	PG0							
Reset:	global							
Restriction Restriction : VGA requires panel fitting to be enabled. VGA is always connected to pipe A. VGA can not be enabled while the display power well is powered down. VGA display should only be enabled if all display planes other than VGA are disabled.								
DWord	Bit	Description						
0	31	VGA Display Disable This bit will disable the VGA compatible display mode. It has no effect on VGA register or A0000-BFFFF memory aperture accesses which are controlled by the PCI configuration and VGA I/O register settings.						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>0b</td><td>Enable</td></tr><tr><td>1b</td><td>Disable [Default]</td></tr></table>	Value	Name	0b	Enable	1b	Disable [Default]
		Value	Name					
		0b	Enable					
		1b	Disable [Default]					
	Restriction Restriction : The VGA SR01 screen off bit must be programmed when enabling and disabling VGA. See the VGA Registers document. Restriction : GT driver mailbox must be programmed when enabling and disabling VGA. See the "VGA" section.							
	30:27	Reserved <table><tr><td>Format:</td><td>PBC</td></tr></table>	Format:	PBC				
	Format:	PBC						
	26	VGA Border Enable This bit determines if the VGA border areas are included in the active display area. The border will be scaled along with the pixel data.						
		<table><tr><th>Value</th><th>Name</th></tr></table>	Value	Name				
Value	Name							



VGA_CONTROL			
		0b	Disable
		1b	Enable
	25	Reserved	
		Format:	PBC
	24	Pipe CSC Enable	
		Description This bit enables pipe color space conversion for the VGA pixel data.	
		Value	Name
		0b	Disable
		1b	Enable
	23:21	Reserved	
		Format:	PBC
	20	Legacy 8Bit Palette En This bit affects reads and writes to the palette through VGA I/O addresses. In the 6-bit mode, the 8-bits of data are shifted up two bits on the write (upper two bits are lost) and shifted two bits down on the read. This provides backward compatibility for original VGA programs as well as VESA VBE support for 8-bit palette. It does not affect palette accesses through the palette register MMIO path.	
		Value	Name
		0b	6 bit DAC
		1b	8 bit DAC
	19	Reserved	
	18	Reserved	
	17:16	Reserved	
		Format:	PBC
	15:12	Reserved	
	11:8	Reserved	
	7:6	Blink Duty Cycle Controls the VGA text mode blink duty cycle relative to the VGA cursor blink duty cycle.	
		Value	Name
		00b	100%
		01b	25%
		10b	50%
		11b	75%



VGA_CONTROL						
	5:0	VSYNC Blink Rate Controls the VGA blink rate in terms of the number of VSYNCs per on/off cycle. <table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">Program with (VSYNCs/cycle)/2-1</td></tr></table>	Programming Notes		Program with (VSYNCs/cycle)/2-1	
Programming Notes						
Program with (VSYNCs/cycle)/2-1						



Video BIOS ROM Base Address

ROMADR_0_2_0_PCI - Video BIOS ROM Base Address		
Register Space: PCI: 0/2/0		
Source: BSpec		
Default Value: 0x00000000		
Size (in bits): 32		
Address: 00030h		
The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.		
DWord	Bit	Description
0	31:18	ROM Base Address
		Default Value: 000000000000000b
		Access: RO
		Hardwired to 0's.
	17:11	Address Mask
		Default Value: 0000000b
		Access: RO
		Hardwired to 0s to indicate 256 KB address range.
	10:1	Reserved
		Default Value: 0000000b
		Access: RO
		Reserved
	0	ROM BIOS Enable
		Default Value: 0b
		Access: RO
		Hardwired to 0 to indicate ROM not accessible.



VTd Status

VTD_STATUS_0_2_0_PCI - VTd Status			
Register Space:		PCI: 0/2/0	
Source:		BSpec	
Default Value:		0x00000000	
Size (in bits):		8	
Address:		00063h	
This register contains indicator bits for Graphics VTd mode.			
DWord	Bit	Description	
0	7:1	RESERVED	
		Default Value:	000b
		Access:	RO
		Reserved	
	0	GFX VTd Active	
		Default Value:	0b
		Access:	RO Variant Firmware Only
Reflects GFX VTd Mode is active. 1 - if active, 0 if inactive.			



Wait For Event and Display Flip Flags Register 1

SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1				
Register Space:	MMIO: 0/2/0			
Source:	BSpec			
Default Value:	0x00000000			
Access:	R/W			
Size (in bits):	32			
This register is the saved value of what wait for events are still valid. This register is part of context save and restore for RC6 feature.				
Programming Notes		Source		
Programming Restriction: This register should NEVER be programmed by SW, this is for HW internal use only.				
VideoCS/VideoCS2/VideoEnhancementCS: This register functionality is not supported and must not be exercised for reads or writes.		VideoCS, VideoCS2, VideoEnhancementCS		
DWord	Bit	Description		
0	31:25	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ
	Format:	MBZ		
	24	Display Plane 11 Synchronous Flip Pending Wait Enable <table><tr><td>Format:</td><td>Enable</td></tr></table> This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	Format:	Enable
	Format:	Enable		
23	Display Plane 11 Synchronous Flip Display Pending <table><tr><td>Format:</td><td>Enable</td></tr></table> This field enables a wait for the duration of a Display Plane 11 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	Format:	Enable	
Format:	Enable			
22	Display Plane 10 Synchronous Flip Pending Wait Enable <table><tr><td>Format:</td><td>Enable</td></tr></table> This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip	Format:	Enable	
Format:	Enable			



SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

	Pending Condition in the Device Programming Interface chapter of MI Functions.	
21	Display Plane 10 Synchronous Flip Display Pending	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane 10 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	
20	Display Plane 9 Synchronous Flip Pending Wait Enable	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	
19	Display Plane 9 Synchronous Flip Display Pending	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane 9 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	
18	Display Plane 8 Synchronous Flip Pending Wait Enable	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	
17	Display Plane 8 Synchronous Flip Display Pending	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane 8 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	
16	Display Plane 7 Synchronous Flip Pending Wait Enable	
	Format:	Enable
	This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip	



SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags

Register 1

	request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.		
15	Display Plane 7 Synchronous Flip Display Pending <table><tr><td>Format:</td><td>Enable</td></tr></table> This field enables a wait for the duration of a Display Plane 7 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.	Format:	Enable
Format:	Enable		
14	Display Pipe C Scan Line Event Pending <table><tr><td>Format:</td><td>Enable</td></tr></table> This field indicates scan line event operation is pending from Display Pipe C. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-C and gets reset on scan line event completion for Display Plane-C.	Format:	Enable
Format:	Enable		
13	Display Pipe B Scan Line Event Pending <table><tr><td>Format:</td><td>Enable</td></tr></table> This field indicates scan line event operation is pending from Display Pipe B. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-B and gets reset on scan line event completion for Display Plane 3.	Format:	Enable
Format:	Enable		
12	Display Pipe A Scan Line Event Pending <table><tr><td>Format:</td><td>Enable</td></tr></table> This field indicates scan line event operation is pending from Display Pipe A. This field gets set when MI_SCANLINE_INCL/EXCL command is parsed for Display Plane-A and gets reset on scan line event completion for Display Plane 1.	Format:	Enable
Format:	Enable		
11	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ
Format:	MBZ		
10	Display Plane 3 Asynchronous Display Flip Pending <table><tr><td>Format:</td><td>Enable</td></tr></table> This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).	Format:	Enable
Format:	Enable		
9	Display Plane 3 Synchronous Flip Display Pending <table><tr><td>Format:</td><td>Enable</td></tr></table>	Format:	Enable
Format:	Enable		



SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags

Register 1

	This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).					
8	Display Plane 6 Synchronous Flip Display Pending <table><tr><td>Format:</td><td>Enable</td></tr></table> This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.		Format:	Enable		
Format:	Enable					
7	Reserved <table><tr><td>Source:</td><td>BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>		Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS	Format:	MBZ
Source:	BlitterCS, VideoCS, VideoCS2, VideoEnhancementCS					
Format:	MBZ					
7	Display Plane 3 Asynchronous Performance Flip Pending Wait Enable <table><tr><td>Source:</td><td>RenderCS</td></tr><tr><td>Format:</td><td>Enable</td></tr></table> This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).		Source:	RenderCS	Format:	Enable
Source:	RenderCS					
Format:	Enable					
6	Display Plane 3 Asynchronous Flip Pending Wait Enable <table><tr><td>Format:</td><td>Enable</td></tr></table> This field enables a wait for the duration of a Display Plane 3 "Flip Pending" condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).		Format:	Enable		
Format:	Enable					
5	Display Plane 3 Synchronous Flip Pending Wait Enable <table><tr><td>Format:</td><td>Enable</td></tr></table> This field enables a wait for the duration of a Display Plane 3 Flip Pending condition. If a flip request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition (in the Device Programming Interface chapter of MI Functions).		Format:	Enable		
Format:	Enable					
4	Display Plane 6 Synchronous Flip Pending Wait Enable <table><tr><td>Format:</td><td>Enable</td></tr></table> This field enables a wait for the duration of a Display Plane 6 Flip Pending condition. If a flip		Format:	Enable		
Format:	Enable					



SYNC_FLIP_STATUS_1 - Wait For Event and Display Flip Flags Register 1

		request is pending, the parser will wait until the flip operation has completed (i.e., the new front buffer address has now been loaded into the active front buffer registers). See Display Flip Pending Condition in the Device Programming Interface chapter of MI Functions.
3	Reserved	
	Format:	MBZ
2	Display Pipe C Scan Line Wait Enable	
	Format:	Enable
	This field enables a wait while a Display Pipe C Scan Line condition exists. This condition is defined as the the start of the scan line specified in the Pipe C Display Scan Line Count Range Compare Register. See Scan Line Event in the Device Programming Interface chapter of MI Functions.	
1	Display Pipe C Vertical Blank Wait Enable	
	Format:	Enable
	This field enables a wait until the next Display Pipe C Vertical Blank event occurs. This event is defined as the start of the next Display Pipe C vertical blank period. Note that this can cause a wait for up to an entire refresh period. See Vertical Blank Event (See Programming Interface).	
0	Reserved	
	Format:	MBZ



Watchdog Counter Control

PR_CTR_CTL - Watchdog Counter Control			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x00000001		
Access:	R/W		
Size (in bits):	32		
Restriction			
Restriction: SW must enable and disable watch dog counter inline to a command sequence of any given workload within the same command buffer dispatch. Watch Dog counter once enabled doesn't stop unless it is explicitly disabled. SW must explicitly reset the watch dog counter by disabling it before enabling the watch dog counter for a new command sequence. Preemption could happen in a command sequence prior to watch dog counter getting disabled resulting in watch dog counter enabled following preemption. In Ring Buffer Mode of scheduling, SW must explicitly take care of disabling the watch dog counter as part of the preemption sequence. SW must explicitly reset the watch dog counter by disabling it before enabling the watch dog counter for a new command sequence. In Execution List Mode of scheduling, SW must do one of the following programing sequences to ensure watch dog timer is properly managed on context preemption. SW must not preempt workload that has watch dog timer enabled, that can be done by placing MI_ARB_ON_OFF command around the workload. OR SW must disable watch dog timer through direct MMIO access before submitting any execution list to the Execution List Submit port.			
DWord	Bit	Description	
0	31	Count Select	
		Format: U1	
		Value	Name
		Description	
	0h	[Default]	Use eight times the time stamp base unit to increment the watch dog count. The granularity of the time stamp base unit is defined in the "Time Stamp Bases" subsection in Power Management chapter.
	1h		Use the fixed function clock (csclk) to increment the watchdog count
30:0	Counter Logic Op		
	Default Value:		1h
	This field specifies the action to be taken by the clock counter to generate interrupts. Writing a Zero value to this register starts the counting. Writing a Value of 0000_0001 to this counter stops the counter.		



WM_MISC

WM_MISC				
Register Space:		MMIO: 0/2/0		
Source:		BSpec		
Default Value:		0x00000000		
Access:		R/W		
Size (in bits):		32		
Address:		45260h-45263h		
Name:		Watermark Miscellaneous		
ShortName:		WM_MISC		
Power:		PG0		
Reset:		soft		
DWord	Bit	Description		
0	31	Reserved		
		Format:	PBC	
	30:28	Reserved		
	27	MIPI DBI Method		
		This field controls the behavior for the TTNF calculation for MIPI DBI.		
		Value	Name	Description
		0b	Calculated	TTNF calculated in active area and all 1s outside of active. TTVBI all 1s.
	1b	Simple	TTNF all 0s in active area and all 1s outside of active. TTVBI all 1s.	
	26	Reserved		
		Format:	MBZ	
25:24	MIPI DBI On Pipe C			
	This field selects whether MIPI DBI is on this pipe. This changes the TTNF and TTVBI calculations.			
	Value	Name		
	00b	MIPI DBI not on this pipe		
	10b	MIPIA DBI or dual link DBI on this pipe		
23:22	MIPI DBI On Pipe B			
	This field selects whether MIPI DBI is on this pipe. This changes the TTNF and TTVBI calculations.			
	Value	Name		
	00b	MIPI DBI not on this pipe		
	10b	MIPIA DBI or dual link DBI on this pipe		
11b	MIPIC DBI on this pipe			



WM_MISC										
	21:20	MIPI DBI On Pipe A This field selects whether MIPI DBI is on this pipe. This changes the TTNF and TTVBI calculations.								
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>00b</td><td>MIPI DBI not on this pipe</td></tr><tr><td>10b</td><td>MIPIA DBI or dual link DBI on this pipe</td></tr><tr><td>11b</td><td>MIPIC DBI on this pipe</td></tr></table>	Value	Name	00b	MIPI DBI not on this pipe	10b	MIPIA DBI or dual link DBI on this pipe	11b	MIPIC DBI on this pipe
		Value	Name							
		00b	MIPI DBI not on this pipe							
	10b	MIPIA DBI or dual link DBI on this pipe								
11b	MIPIC DBI on this pipe									
19:0	Reserved									



ZTLB LRA 0

ZTLB_LRA_0 - ZTLB LRA 0		
Register Space:	MMIO: 0/2/0	
Source:	BSpec	
Default Value:	0x01007E00	
Size (in bits):	32	
Address:	04A30h	
DWord	Bit	Description
0	31	Reserved
	30:29	Reserved
		Default Value: 00b
		Access: RO
	28:27	STC LRA
		Default Value: 00b
		Access: R/W
		Which LRA should STC use.
	26:18	ZTLB LRA1 Min
		Default Value: 001000000b
		Access: R/W
		Minimum value of programmable LRA1.
	17:9	ZTLB LRA0 Max
		Default Value: 000111111b
		Access: R/W
		Maximum value of programmable LRA0.
	8:0	ZTLB LRA0 Min
		Default Value: 000000000b
		Access: R/W
		Minimum value of programmable LRA0.



ZTLB LRA 1

ZTLB_LRA_1 - ZTLB LRA 1			
Register Space:		MMIO: 0/2/0	
Source:		BSpec	
Default Value:		0x33BD80BF	
Size (in bits):		32	
Address:		04A34h	
DWord	Bit	Description	
0	31	Reserved	
		Default Value:	0b
		Access:	RO
	30:29	HIZ LRA	
		Default Value:	01b
		Access:	R/W
		Which LRA should HIZ use.	
	28:27	RCZ LRA	
		Default Value:	10b
		Access:	R/W
		Which LRA should RCZ use.	
	26:18	ZTLB LRA2 Max	
		Access:	R/W
		Maximum value of programmable LRA2.	
		Value	Name
011101111b		[Default]	
17:9	ZTLB LRA2 Min		
	Default Value:	011000000b	
	Access:	R/W	
	Minimum value of programmable LRA2.		
8:0	ZTLB LRA1 Max		
	Default Value:	010111111b	
	Access:	R/W	
	Maximum value of programmable LRA1.		



ZTLB LRA 2

ZTLB_LRA_2 - ZTLB LRA 2			
Register Space:	MMIO: 0/2/0		
Source:	BSpec		
Default Value:	0x000DFEF0		
Size (in bits):	32		
Address:	04A38h		
DWord	Bit	Description	
0	31:20	Reserved	
		Default Value:	000000000000b
		Access:	RO
	19:18	GATR LRA	
		Default Value:	11b
		Access:	R/W
		Which LRA should GATR use.	
	17:9	ZTLB LRA3 Max	
		Access:	R/W
		Maximum value of programmable LRA3.	
		Value	Name
		011111111b	[Default]
	8:0	ZTLB LRA3 Min	
		Access:	R/W
		Minimum value of programmable LRA3.	
Value		Name	
011110000b		[Default]	



Intel® Open Source HD Graphics

Programmer's Reference Manual

For the 2016 Intel Atom™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Apollo Lake" Platform (Broxton Graphics)

Volume 2c: Command Reference: Structures

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Any Binding Table Index Message Descriptor Control Field

MDC_BTS_SLM_A32 - Any Binding Table Index Message Descriptor Control Field				
Source:		BSpec		
Size (in bits):		8		
Default Value:		0x00000000		
DWord	Bit	Description		
0	7:0	Binding Table Index		
		Format: Enumeration		
		Specifies the surface for the message, which can be Surface State Model, SLM or Stateless.		
		Value	Name	Description
		00h-0EFh	BTS	Index of Binding Table State Surfaces
		F0h-0FBh	Reserved	Reserved for future use
		0FCh	Reserved	Reserved for future use
		0FEh	SLM	Specifies an SLM access
		0FFh	A32_A64	Specifies a A32 or A64 Stateless access that is locally coherent (coherent within a thread group)
		0FDh	A32_A64_NC	Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).
		Restriction		
		Restriction : When using A32_A64_NC, SW must ensure that 2 threads do not both access the same cache line (64B)		



Bit Definition for Interrupt Control Registers - Render

Bit Definition for Interrupt Control Registers - Render		
Source:		RenderCS
Size (in bits):		32
Default Value:		0x00000000
DWord	Bit	Description
0	31:16	Reserved
		Format: MBZ Reserved for other command streamers - cannot be allocated by main command streamer.
	15:12	Reserved
		Format: MBZ
	11	Wait on Semaphore Exec-List Scheduling: Set when MI_SEMAPHORE_WAIT command is un-successful and when "Inhibit Synchronous Context Switch" is set. Scheduler can use this interrupt to preempt the context waiting on semaphore wait.
	10	L3 Counter Save Interrupt
	9	Reserved
		Format: MBZ
	8	Context Switch Interrupt Set when a context switch has just occurred. Execlist Enable bit needs to be set for this interrupt to occur.
	7	Page Fault
		Description This interrupt is for handling Legacy Page Fault interface for all Command Streamers (BCS, RCS, VCS, VECS). When Fault Repair Mode is enabled, Interrupt mask register value is not looked at to generate interrupt due to page fault. Please refer to vol1c "Page Fault Support" section for more details.
	6	Timeout Counter Expired Set when the render pipe timeout counter (0x02190) has reached the timeout threshold value (0x0217c).
5	Reserved	
	Format: MBZ	
4	PIPE_CONTROL Notify Interrupt The Pipe Control packet (Fences) specified in 3D pipeline document may optionally generate an Interrupt. The Store QW associated with a fence is completed ahead of the interrupt.	
3	Render Command Parser Master Error When this status bit is set, it indicates that the hardware has detected an error. It is set by the device upon an error condition and cleared by a CPU write of a one to the appropriate bit contained in the Error ID register followed by a write of a one to this bit in the IIR. Further	



Bit Definition for Interrupt Control Registers - Render

Bit Definition for Interrupt Control Registers - Render			
		information on the source of the error comes from the "Error Status Register" which along with the "Error Mask Register" determine which error conditions will cause the error status bit to be set and the interrupt to occur. Page Table Error: Indicates a page table error. Instruction Parser Error: The Render Instruction Parser encounters an error while parsing an instruction.	
	2	Reserved	
		Format:	MBZ
	1	Reserved	
	0	Render Command Parser User Interrupt This status bit is set when an MI_USER_INTERRUPT instruction is executed on the Render Command Parser. Note that instruction execution is not halted and proceeds normally. A mechanism such as an MI_STORE_DATA instruction is required to associate a particular meaning to a user interrupt.	



Context Descriptor Format

Context Descriptor Format		
Source:	BSpec	
Size (in bits):	64	
Default Value:	0x00000000, 0x00000000	
This is the format of context descriptors which make up submitted execlists.		
DWord	Bit	Description
0..1	63:32	Context ID
		Description
		Context ID is a unique field assigned by GFX driver when a new context is created by which it is identified across all hierarchies of SW and HW. - Context ID is used for semaphore signaling by hardware and software. - Context ID matching is used by hardware to detect Lite Restore. - Context ID is used by hardware for page fault reporting and response with IOMMU. - Context switch reason and the associated Context ID are reported to Context Switch Status Buffer by hardware on a context switch.
		Context ID[31:0] (bits[63:32] of the context descriptor) are used for comparing during lite restore, semaphore signaling and context specific OA enabling.
		Context ID which is a 32 bit field is further divided in to three segments described below: Bits[63:55] (Bits 31:23 of Context ID) is referred to as GroupID. GroupId+PASID combination of a context must be a unique identifier for contexts that are active in the system. The definition of active context is listed as: - Any Context that is already submitted to h/w or already running in h/w. - Any Context that hit page faults, was preempted (didn't run to context complete), and is waiting to be resubmitted pending IOMMU "last in group" response. - Any Context that has experienced reset but not all faults are responded to. Bit[54] (Bit 22 of Context ID) – MBZ for SW programming; this bit is used by hardware to distinguish between F&H vs F&S page requests and response messages to and from IOMMU. This bit is used by hardware on receiving page response to properly manage the page fault counters Bit[53] (Bit 21 of Context ID) – MBZ from SW programming, is reserved for future hardware use. Bits[52:32] (Bits 20:0 of Context ID) are for software use-only and must be unique field assigned by GFX driver when a new context is created.
		Context ID is reported by hardware to OABUFFER along with the performance statistics counters, Context ID is used for filtering the statistics on per context basis.



Context Descriptor Format

Context Descriptor Format				
	31:12	Logical Ring Context Address (LRCA)		
		Format:	GraphicsAddress[31:12]	
	This field contains the 4 KB-aligned address of the Logical Ring Context associated with this execlist element. LRCA must be always programmed in GGTT memory.			
	11:9	Reserved		
		Format:	MBZ	
	8	Privilege Access		
		This field when set indicates PPGTT enabled in legacy context mode. In advanced context mode this field is reserved and must be zero.		
	7:6	Fault Handling		
		Source:	CommandStreamer	
		Value	Name	Description
0h		Fault and Hang	Fault model is not supported and fault occurrence is treated as catastrophic. GAM indicates Fault Error to Command streamer. Fault Error interrupt is reported to scheduler. Command Streamer will not initiate context switch on occurrence of Fault Error.	
1h		Reserved	Reserved	
2h		Fault and Stream	In this mode of operation faults are allowed on EU memory accesses. Page Walker will directly work with memory page handler to fix the faults on the fly for these surfaces. Command streamer is not aware of the fault service being done by page walker and goes with its normal execution rules for context switch. On completion of flush during context switch CS explicitly requests acknowledge message to Page Walker before proceeding further. Page Walker acknowledges Command Streamer once it is done on a clean boundary. Page Walker asserts Fault Error on occurrence of non recoverable fault or access violations (Command Streamer access, VFunit access, etc) to Command Streamer; this is the same as Fault and Hang behavior.	
Others		Reserved	Reserved	
Programming Notes				
When execlist mode is set to "Legacy Context mode" Fault Handling mode must be set to "Fault and Hang." For proper programming for Page Fault modes, refer to memory interface section of the Bspec for the corresponding generation.				
5		Reserved		
	Format:	MBZ		

Context Descriptor Format

Context Descriptor Format			
4:3	Addressing Mode & Legacy Context		
	Format:	U2	
	Legacy context set indicates GPU is operating in legacy context mode of operation and doesn't support any SVM features. Legacy context reset indicates GPU is operating in advanced context mode of operation and support SVM features. Based on the Context mode set Addressing mode is interpreted appropriately. The table below summarizes the combinations supported. GFX engine always uses 32b virtual addressing mode when translated using GGTT irrespective of below options.		
	Value	Name	Description
	00b	Advanced Context with no A/D support	GPU is enabled for advanced context mode and supports SVM features. GPU DOESN'T support Access and Dirty bit management in page tables. GPU supports 64b(48bit canonical) PPGTT graphics virtual addressing. PDP0_DESCRIPTOR contains the PASID (process address space identifier) and other PDP Descriptors are ignored.
	01b	Legacy Context with no 64 bit VA support	GPU is enabled for legacy context mode of operation and DOESN'T support any SVM features. GPU supports 32b PPGTT graphics virtual addressing. PDP*_DESCRIPTOR contains the base address to 4GB of memory space supported.
10b	Advanced Context with A/D support	GPU is enabled for advanced context mode and supports SVM features. GPU DOES support Access and Dirty bit management in page tables. GPU supports 64b (48bit canonical) PPGTT graphics virtual addressing. PDP0_DESCRIPTOR contains the PASID (process address space identifier) and other PDP Descriptors are ignored.	
	11b	Legacy Context with 64 bit VA support	GPU is enabled for legacy context mode of operation and DOESN'T support any SVM features. GPU supports 64b (48bit canonical) PPGTT graphics virtual addressing and PDP0_DESCRIPTOR contains the base address to PML4 and other PDP Descriptors are ignored.
	2	Force Restore Setting this bit will force a context restore operation when switching to this context even if the LRCA in the CCID register (normally the LRCA of the last context from the prior execlist) matches this one. Note that it is legal (and likely desirable) for the Render Context Restore Inhibit bit (part of the CTXT_SR_CTL register) in the context image being restored to also be set. The "ring" context is being forced to be restored from a newly initialized context despite a possible LRCA match. However, the render context for such a newly initialized context will likely be uninitialized and so should not be restored.	
Workaround		Source	
Workaround Force Restore bit must be always be set on all context submissions.		BlitterCS, VideoCS, VideoEnhancementCS	



Context Descriptor Format

	1	Force PD Restore Setting this bit will cause the on-chip page directory to be reloaded from the PD image in memory even on an LRCA match. No other operations of context restore will occur on an LRCA match, however. Software should set this bit if it has updated a context's page directory and wants the context to begin using the new page directory without having to switch away from it (to another context) and back again. Setting this bit will have no effect if Force Restore is also set; a complete context restore (including the PD) will be performed.
	0	Valid Set if this register holds a valid context descriptor. SW should set this bit in the Element registers that it has set up to contain valid context descriptors. Any execlist elements that are not used in a submitted execlist must have this bit clear.



HW Generated BINDING_TABLE_STATE

HW Generated BINDING_TABLE_STATE			
Source:	BSpec		
Size (in bits):	16		
Default Value:	0x00000000		
Description			
The binding table binds surfaces to logical resource indices used by shaders and other compute engine kernels. The HW generated Binding_Table_State have different format than the SW generated Binding_Table_State. The HW generated Binding_Table_State is stored as an array of 256 elements, each of which contains one word as defined here. The start of each element is spaced one word apart. The first element of the binding table is aligned to a 64-byte boundary. Binding table indexes beyond 256 will automatically be mapped to entry 0 by the HW, w/ the exception of any messages which support the special indexes 255 and 254.			
DWord	Bit	Description	
0	15:0	Surface State Pointer	
		Format:	SurfaceStateOffset[21:6]



Image_State_Cost

Image_State_Cost		
Source:	VideoCS	
Size (in bits):	64	
Default Value:	0x00000000, 0x00000000	
DWord	Bit	Description
0	31:24	MV 3 Cost
		Format: U4U4
		Programming Notes
		U4U4 format explanation
	23:16	MV 2 Cost
		Format: U4U4
	15:8	MV 1 Cost
		Format: U4U4
	7:0	MV 0 Cost
		Format: U4U4
1	31:24	MV 7 Cost
		Format: U4U4
	23:16	MV 6 Cost
		Format: U4U4
	15:8	MV 5 Cost
		Format: U4U4
	7:0	MV 4 Cost
		Format: U4U4



INTERFACE_DESCRIPTOR_DATA

INTERFACE_DESCRIPTOR_DATA				
Source:		RenderCS		
Size (in bits):		256		
Default Value:		0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000		
DWord	Bit	Description		
0	31:6	Kernel Start Pointer		
		Format:	InstructionBaseOffset[31:6]Kernel	
	Specifies the 64-byte aligned address offset of the first instruction in the kernel. This pointer is relative to the Instruction Base Address .			
5:0	Reserved			
	Format:	MBZ		
1	31:16	Reserved		
		Format:	MBZ	
	15:0	Kernel Start Pointer High		
		Format:	InstructionBaseOffset[47:32]Kernel	
This field specifies the high 16 bits of starting address of the Kernel Pointer.				
2	31:20	Reserved		
		Format:	MBZ	
	19	Denorm Mode		
		This field specifies how Float denormalized numbers are handles in the dispatched thread.		
		Value	Name	Description
		0h	Ftz	Float denorms will be flushed to zero when appearing as inputs; denorms will never come out of instructions. Double precision float and half precision float numbers are not flushed to zero.
		1h	SetByKernel	Denorms will be handled in by kernel.
	18	Single Program Flow		
		Specifies whether the kernel program has a single program flow (SIMDn _{xm} with m = 1) or multiple program flows (SIMDn _{xm} with m > 1).		
		Value		Name
0h		Multiple		
1h	Single			
17	Thread Priority			
	Specifies the priority of the thread for dispatch.			
	Value		Name	
0h	Normal Priority			



INTERFACE_DESCRIPTOR_DATA			
		1h	High Priority
	16	Floating Point Mode Specifies the floating point mode used by the dispatched thread.	
		Value	Name
		0h	IEEE-754
		1h	Alternate
	15:14	Reserved Format: MBZ	
	13	Illegal Opcode Exception Enable Format: Enable This bit gets loaded into EU CR0.1[12] (note the bit # difference). See <i>Exceptions and ISA Execution Environment</i> .	
	12	Reserved Format: MBZ	
	11	Mask Stack Exception Enable Format: Enable This bit gets loaded into EU CR0.1[11]. See <i>Exceptions and ISA Execution Environment</i> .	
	10:8	Reserved Format: MBZ	
3	7	Software Exception Enable Format: Enable This bit gets loaded into EU CR0.1[13] (note the bit # difference). See <i>Exceptions and ISA Execution Environment</i> .	
	6:0	Reserved Format: MBZ	
	31:5	Sampler State Pointer Format: DynamicStateOffset[31:5]SAMPLER_STATE Specifies the 32-byte aligned address offset of the sampler state table. This pointer is relative to the Dynamic State Base Address . <i>This field is ignored for child threads.</i>	



INTERFACE_DESCRIPTOR_DATA																
	4:2	Sampler Count														
		Format: U3														
		Specifies how many samplers (in multiples of 4) the kernel uses. Used only for prefetching the associated sampler state entries. <i>This field is ignored for child threads.</i> <i>If this field is not zero, sampler state is prefetched for the first instance of a root thread upon the startup of the media pipeline.</i>														
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>[0,4]</td><td></td></tr><tr><td>0h</td><td>No samplers used</td></tr><tr><td>1h</td><td>Between 1 and 4 samplers used</td></tr><tr><td>2h</td><td>Between 5 and 8 samplers used</td></tr><tr><td>3h</td><td>Between 9 and 12 samplers used</td></tr><tr><td>4h</td><td>Between 13 and 16 samplers used</td></tr></table>	Value	Name	[0,4]		0h	No samplers used	1h	Between 1 and 4 samplers used	2h	Between 5 and 8 samplers used	3h	Between 9 and 12 samplers used	4h	Between 13 and 16 samplers used
		Value	Name													
		[0,4]														
		0h	No samplers used													
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		3h	Between 9 and 12 samplers used													
	4h	Between 13 and 16 samplers used														
	1:0	Reserved														
		Format: MBZ														
		4	31:16	Reserved												
				Format: MBZ												
15:5				Binding Table Pointer												
	Format: SurfaceStateOffset[15:5]BINDING_TABLE_STATE*256															
	Description															
	Specifies the 32-byte aligned address of the binding table. This pointer is relative to the Surface State Base Address . <i>This field is ignored for child threads.</i>															
4:0	Binding Table Entry Count															
	Format: U5															
	Specifies how many binding table entries the kernel uses. Used only for prefetching of the binding table entries and associated surface state. <i>This field is ignored for child threads.</i> <i>If this field is not zero, binding table and surface state are prefetched for the first instance of a root thread upon the startup of the media pipeline.</i>															
	<table><tr><th>Value</th><th>Name</th></tr><tr><td>[0,31]</td><td></td></tr></table>	Value	Name	[0,31]												
	Value	Name														
	[0,31]															
	Programming Notes															
The maximum number of prefetched binding table entries is limited to 31. For kernels using a large number of binding table entries, it may be wise to set this field to zero to avoid prefetching too many entries and thrashing the state cache.																



INTERFACE_DESCRIPTOR_DATA																	
5	31:16	Constant/Indirect URB Entry Read Length															
		Format:		U16													
		Specifies the amount of URB data read and passed in the thread payload for the Constant or Indirect URB entry, in 8-DW register increments. A value 0 means that no Constant or Indirect URB Entry will be loaded. The Constant URB Entry Read Offset field will then be ignored. In GPGPU mode this describes how much data is delivered in a single dispatch. Multiple dispatches in a thread group will deliver constant data offset by this value. The total amount of constant data is (Constant URB Read Length * Number of Threads in GPGPU Thread Group + Cross-Thread Constant Data Read Length).															
		If Cross-Thread Constant Data Read Length for Indirect is greater than 0, then this field must also be greater than 0. The allowed combinations are:															
		<table><tr><th>Constant/Indirect URB Entry Read Length</th><th>Cross-Thread Constant Data Read Length</th><th>Notes</th></tr><tr><td>=0</td><td>=0</td><td>No Payload</td></tr><tr><td>>0</td><td>=0</td><td>Per-thread payload only</td></tr><tr><td>>0</td><td>>0</td><td>Both kinds of payload</td></tr><tr><td>=0</td><td>>0</td><td>Only for CURBE payloads</td></tr></table>			Constant/Indirect URB Entry Read Length	Cross-Thread Constant Data Read Length	Notes	=0	=0	No Payload	>0	=0	Per-thread payload only	>0	>0	Both kinds of payload	=0
Constant/Indirect URB Entry Read Length	Cross-Thread Constant Data Read Length	Notes															
=0	=0	No Payload															
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		<table><tr><th>Value</th><th>Name</th></tr><tr><td>[0,63]</td><td></td></tr></table>	Value	Name	[0,63]												
Value	Name																
[0,63]																	
15:0		Constant URB Entry Read Offset															
		Format:		U16													
		Specifies the offset (in 8-DW units) at which Constant URB data is to be read from the URB before being included in the thread payload.															
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[0,1983]</td><td></td><td>Indicating [0,1983] 256-bit register increments. ROB has 64KB of storage; 2048 entries. However, lowest 64 entries are reserved for VFE/TS to store interface descriptor data. Hence, (URB Entry Read Offset + Read Length) shall not exceed 1984.</td></tr></table>	Value	Name	Description	[0,1983]		Indicating [0,1983] 256-bit register increments. ROB has 64KB of storage; 2048 entries. However, lowest 64 entries are reserved for VFE/TS to store interface descriptor data. Hence, (URB Entry Read Offset + Read Length) shall not exceed 1984.									
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6	31:24	Reserved															
		Format:		MBZ													
	23:22	Rounding Mode															
		Format:		U2													
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>00b</td><td>RTNE [Default]</td><td>Round to Nearest Even</td></tr></table>	Value	Name	Description	00b	RTNE [Default]	Round to Nearest Even									
Value	Name	Description															
00b	RTNE [Default]	Round to Nearest Even															

**INTERFACE_DESCRIPTOR_DATA**

		01b	RU	Round toward +Infinity
		10b	RD	Round toward -Infinity
		11b	RTZ	Round toward Zero
21	Barrier Enable			
	Format:		Enable	
	This field specifies whether the thread group requires a barrier. If not, it can be dispatched without allocating one.			
20:16	Shared Local Memory Size			
	Format:		U5	
	This field indicates how much Shared Local Memory the thread group requires. The amount is specified in 4k blocks, but only powers of 2 are allowed: 0, 4k, 8k, 16k, 32k and 64k per half-slice.			
	Uses a different encoding to allow encodings for the new 1k and 2k SLM sizes.			



INTERFACE_DESCRIPTOR_DATA								
	9:0	Number of Threads in GPGPU Thread Group						
		Format:U10						
		Specifies the number of threads that are in this thread group.						
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[1,54]</td><td></td><td>The minimum value is 1, while the maximum value is the number of threads in a pool or subslice for local barriers. See vol1b Configurations for the number of threads per subslice for different products. The number of threads per pool is defined by the MEDIA_POOL_STATE command.</td></tr></table>	Value	Name	Description	[1,54]		The minimum value is 1, while the maximum value is the number of threads in a pool or subslice for local barriers. See vol1b Configurations for the number of threads per subslice for different products. The number of threads per pool is defined by the MEDIA_POOL_STATE command.
		Value	Name	Description				
		[1,54]		The minimum value is 1, while the maximum value is the number of threads in a pool or subslice for local barriers. See vol1b Configurations for the number of threads per subslice for different products. The number of threads per pool is defined by the MEDIA_POOL_STATE command.				
<table><tr><th colspan="3">Restriction</th></tr><tr><td colspan="3">Restriction : The maximum value for global barriers is limited by the number of threads in the system, or by 511, whichever is lower. This field should not be set to 0 even if the barrier is disabled, since an accurate value is needed for proper pre-emption.</td></tr></table>	Restriction			Restriction : The maximum value for global barriers is limited by the number of threads in the system, or by 511, whichever is lower. This field should not be set to 0 even if the barrier is disabled, since an accurate value is needed for proper pre-emption.				
Restriction								
Restriction : The maximum value for global barriers is limited by the number of threads in the system, or by 511, whichever is lower. This field should not be set to 0 even if the barrier is disabled, since an accurate value is needed for proper pre-emption.								
7	31:8	Reserved						
		Format:MBZ						
	7:0	Cross-Thread Constant Data Read Length						
		Format:U8						
		Specifies the amount of constant data in CURBE in 8-DW register increments which will be sent to every thread in the thread group in addition to the per thread ids specified by Constant URB Entry Read Length .						
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>[0,127]</td><td></td></tr></table>	Value	Name	[0,127]			
Value	Name							
[0,127]								



MEDIA_SURFACE_STATE

MEDIA_SURFACE_STATE												
Source:	BSpec											
Exists If:	//[MessageType] == 'Deinterlace') OR ([MessageType] == 'Sample_8x8')											
Size (in bits):	256											
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000											
This is the SURFACE_STATE used by only deinterlace, sample_8x8, and VME messages.												
DWord	Bit	Description										
0	31:30	Rotation										
		<table><tr><th>Value</th><th>Name</th></tr><tr><td>00b</td><td>No Rotation or 0 Degree</td></tr><tr><td>01b</td><td>90 Degree Rotation</td></tr><tr><td>10b</td><td>180 Degree Rotation</td></tr><tr><td>11b</td><td>270 Degree Rotation</td></tr></table>	Value	Name	00b	No Rotation or 0 Degree	01b	90 Degree Rotation	10b	180 Degree Rotation	11b	270 Degree Rotation
		Value	Name									
		00b	No Rotation or 0 Degree									
		01b	90 Degree Rotation									
		10b	180 Degree Rotation									
		11b	270 Degree Rotation									
		Programming Notes										
		Rotation is only supported only with AVS function messages and not with HDC direct write and 16x8 AVS messages.										
		29:27	Reserved									
Format:	MBZ											
26:20	X Offset	Exists If:	//[Surface Format] is one of Planar Formats									
		Format:	PixelFormat[8:2]									
		This field specifies the horizontal offset in pixels from the Surface Base Address to the start (origin) of the surface.										
		This field effectively loosens the alignment restrictions on the origin of tiled surfaces. Previously, tiled surface origin was (by definition) located at the base address, and thus needed to satisfy the 4KB base address alignment restriction. Now the origin can be specified at a finer (4-wide x 4-high pixel) resolution.										
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>[0,508]</td><td></td><td>In multiples of 4 (low 2 bits missing)</td></tr></table>	Value	Name	Description	[0,508]		In multiples of 4 (low 2 bits missing)				
		Value	Name	Description								
		[0,508]		In multiples of 4 (low 2 bits missing)								
		Programming Notes										
		For linear surfaces and Packed Formats, this field must be zero.										
		For Surface Format with 8 bits per element, this field must be a multiple of 16.										
For Surface Format with 16 bits per element, this field must be a multiple of 8.												



MEDIA_SURFACE_STATE			
	26:16	Reserved	
		Exists If:	//[Surface Format] is not one of Planar Formats
		Format:	MBZ
	19:16	Y Offset	
		Exists If:	//[Surface Format] is one of Planar Formats
		Format:	RowOffset[5:2]
		This field specifies the vertical offset in rows from the Surface Base Address to the start of the surface. (See additional description in the X Offset field)	
		Value	Name Description
		[0,28]	In multiples of 4 (low two bits missing)
		Programming Notes	
		For linear surfaces and Packed Formats, this field must be zero.	
	15:12	Reserved	
		Format:	MBZ
	11:0	Reserved	
		Format:	MBZ
1	31:18	Height	
		Format:	U14-1
		This field specifies the height of the surface in units of pixels. For PLANAR surface formats, this field indicates the height of the Y (luma) plane.	
		Value	Name Description Exists If
		[0,16383]	representing heights [1,16384] [Surface Type] != FM_STRBUF_*
		Programming Notes	
		Height (field value + 1) must be a multiple of 2 for PLANAR_420 surfaces.If Vertical Line Stride is 1, this field indicates the height of the field, not the height of the frame.	
	17:4	Width	
		Format:	U14-1
		This field specifies the width of the surface in units of pixels. For PLANAR surface formats, this field indicates the width of the Y (luma) plane.	
		Value	Name Description Exists If
		[0,16383]	representing widths [1,16384] [Surface Type] != FM_STRBUF_*
		Programming Notes	
		- The Width specified by this field multiplied by the pixel size in bytes must be less than or equal to the surface pitch (specified in bytes via the Surface Pitch field). - Width (field value + 1) must be a multiple of 2 for PLANAR_420, PLANAR_422, and all	

**MEDIA_SURFACE_STATE**

MEDIA_SURFACE_STATE												
		YCRCB_* and Y16_UNORM surfaces, and must be a multiple of 4 for PLANAR_411 and Y8_UNORM_VA surfaces. For deinterlace messages, the Width (field value + 1) must be a multiple of 8.										
		For Y8_UNORM_VA format width should be in multiple of 4, for Y16_UNORM_VA format width should be in multiple of 2, for Y1_UNORM format width should be in multiple of 32 When Address Control = Mirror, the total width should be in multiple of 4bytes.										
		Width (field value + 1) must be a multiple of 2 for PLANAR_420_16										
	3:2	Picture Structure Specifies the encoding of the current picture. <table><thead><tr><th>Value</th><th>Name</th></tr></thead><tbody><tr><td>00b</td><td>Frame Picture</td></tr><tr><td>01b</td><td>Top Field Picture</td></tr><tr><td>10b</td><td>Bottom Field Picture</td></tr><tr><td>11b</td><td>Invalid, not allowed</td></tr></tbody></table>	Value	Name	00b	Frame Picture	01b	Top Field Picture	10b	Bottom Field Picture	11b	Invalid, not allowed
	Value	Name										
	00b	Frame Picture										
	01b	Top Field Picture										
	10b	Bottom Field Picture										
	11b	Invalid, not allowed										
	1:0	Cr(V)/Cb(U) Pixel Offset V Direction Default Value: 0 Format: U0.2 Description Specifies the distance to the U/V values with respect to the even numbered Y channels in the V direction Programming Notes This field is ignored for all formats except PLANAR_420_8 This offset has been increased from 2 bits to 3 bits to support U1.2 format, and the MSB bit is added as Pixel Offset V Direction MSB in DWord 2. Valid values for the combined field range from 0 to 4.										
2	31:27	Surface Format Description Specifies the format of the surface. All of the Y and G channels will use table 0 and all of the Cr/Cb/R/B channels will use table 1. Note: Y8_UNORM_VA, Y16_UNORM and Y16_SNORM are used for all functions of sample_8x8 except AVS where rest of the formats are not used. These two formats are packed as 32bits in L1 though the individual pixels are either 8bpp or 16bpp respectively. <table><thead><tr><th>Value</th><th>Name</th><th>Description</th></tr></thead></table>	Value	Name	Description							
Value	Name	Description										



MEDIA_SURFACE_STATE				
		0	YCRCB_NORMAL	
		1	YCRCB_SWAPUVY	
		2	YCRCB_SWAPUV	
		3	YCRCB_SWAPY	
		4	PLANAR_420_8	
		5	Y8_UNORM_VA	Sample_8x8 only except AVS
		6	Y16_SNORM	Sample_8x8 only except AVS
		7	Y16_UNORM_VA	Sample_8x8 only except AVS
		8	R10G10B10A2_UNORM	Sample_8x8 only
		9	R8G8B8A8_UNORM	Sample_8x8 AVS only
		10	R8B8_UNORM (CrCb)	Sample_8x8 AVS only
		11	R8_UNORM (Cr/Cb)	Sample_8x8 AVS only
		12	Y8_UNORM	Sample_8x8 AVS only
		13	A8Y8U8V8_UNORM	Sample_8x8 AVS only
		14	B8G8R8A8_UNORM	Sample_8x8 AVS only
		15	R16G16B16A16	Sample_8x8 AVS only
		16	Y1_UNORM	Sample_8x8 only for boolean surfaces (1bit/pixel)
		17	Y32_UNORM	For Integral Image (32bpp)
		18	PLANAR_422_8	Sample_8x8 AVS only
		Others	Reserved	
26	Interleave Chroma			
	Format:		Enable	
	This field indicates that the chroma fields are interleaved in a single plane rather than stored as two separate planes. This field is only used for PLANAR surface formats.			
25	Cr(V)/Cb(U) Pixel Offset U Direction			
	Default Value:		0	
	Format:		U0.1	
	Description			
	Specifies the distance to the U/V values with respect to the even numbered Y channels in the U direction			
	Programming Notes			
	This field must be zero for all formats except PLANAR_420_8, PLANAR_422_8, YCRCB_NORMAL, YCRCB_SWAPUVY, YCRCB_SWAPUV, YCRCB_SWAPY.			

**MEDIA_SURFACE_STATE**

	24	Cr(V)/Cb(U) Pixel Offset V Direction MSB		
		Default Value:		0
		Format:		U1
		Description		
		Specifies the distance to the U/V values with respect to the even numbered Y channels in the V direction		
		Programming Notes		
	23	This field must be zero for all formats except PLANAR_420_8.		
		This offset has been increased from 2 bits to 3 bits as U1.2 format and this bit is used in conjunction with the bits in the Cr(V)/Cb(U) Pixel Offset V Direction field in DWord 1, which contain the rest of the bits for offset V-direction. Valid values for the combined field range from 0 to 4.		
		Memory Compression Mode		
		Distinguishes Vertical from Horizontal compression.		
	22	Value	Name	Description
		0	Horizontal Compression Mode [Default]	
		1	Vertical Compression Mode	
		Memory Compression Enable		
	21	Format:		Enable
		This surface may contain compressed or compressible pixels. Memory compression will be attempted for writes to this surface. Reads from this surface will check for compressed data.		
		Programming Notes		
		The compression control must have 0 value for non-tileY modes.		
	20:3	Please refer to vol1a Memory Data Formats chapter -- section Media Memory Compression for more details, including format restrictions.		
		Address Control		
		Value	Name	Description
		0	CLAMP	Clamp
		1	MIRROR	Mirror
		Surface Pitch		
		Format:		U18-1 pitch in Bytes
		This field specifies the surface pitch in (#Bytes - 1).		
		Value	Name	Description
		[0,262143]		For other linear surfaces: representing [1B, 256KB]
		[511, 262143]		For X-tiled surface: representing [512B, 256KB] = [1 tile, 512 tiles]



MEDIA_SURFACE_STATE

		[127, 262143]	For Y-tiled surfaces: representing [128B, 256KB] = [1 tile, 2048 tiles]
		Programming Notes	
		For tiled surfaces, the pitch must be a multiple of the tile width. If Half Pitch for Chroma is set, this field must be a multiple of two tile widths for tiled surfaces, or a multiple of 2 bytes for linear surfaces. The Surface Pitches of current picture and reference picture should be declared as the identical type in VDI mode with identical Height, Width and Format. If Media Memory Compression is enabled, the following max pitch size restriction must be honored. For larger resolution, Media Memory compression Must be disabled. Tiling Mode Pixel Format Max Frame Width (bytes) Max Frame Width (pixels) Max Pitch (bytes) Legacy 4K 8bpp 16k 16k 16k + 127 16bpp 16k 8k 16k + 127 32bpp 16k 4k 16k + 127 64bpp 16k 2k 16k + 127 128bpp 16k 1k 16k + 127 TileYF 8bpp 8k 8k 8k + 63 16bpp 16k 8k 16k + 127 32bpp 16k 4k 16k + 127 64bpp 16k 2k 16k + 255 128bpp 16k 1k 16k + 255 TileYS 8bpp 16k 16k 16k + 255 16bpp 16k 8k 16k + 511 32bpp 16k 4k 16k + 511 64bpp 16k 2k 16k + 1023 128bpp 16k 1k 16k + 1023	
	2	Half Pitch for Chroma	
		Format:	Enable
		This field indicates that the chroma plane(s) will use a pitch equal to half the value specified in the Surface Pitch field. This field is only used for PLANAR surface formats.	
		Programming Notes	
	1:0	Must be Zero as this field is not used.	
		Tile Mode	
		Format:	U2 Enumerated Type
		This field specifies the type of memory tiling (Linear, WMajor, XMajor, or YMajor) employed to tile this surface. See Memory Interface Functions for details on memory tiling and restrictions.	
		Value	Name
		0h	TILEMODE_LINEAR
		1h	Reserved
		2h	TILEMODE_XMAJOR
		3h	TILEMODE_YMAJOR
		Programming Notes	
		- Refer to <i>Memory Data Formats</i> for restrictions on TileMode direction for the various buffer types. (Of particular interest is the fact that YMAJOR tiling is not supported for display/overlay buffers). - The corresponding cache(s) must be invalidated before a previously accessed surface is accessed again with an altered state of this field. - Linear surfaces can be mapped to Main Memory (uncached) or System Memory (cacheable, snooped). Tiled (X/Y/W) surfaces can only be mapped to Main Memory.	



MEDIA_SURFACE_STATE			
3	31:30	Reserved	
		Format:	MBZ
	29:16	X Offset for U(Cb)	
		Format:	U14 Pixel Offset
		Description	
		For non planar surfaces this field specifies the horizontal offset in pixels from the Surface Base Address to the start (origin) of the surface.	
		For Planar surfaces this field specifies the horizontal offset in pixels from the Y-plane origin to the start (origin) of the U(Cb) plane or the interleaved UV plane if Interleave Chroma is enabled. Resultant X-offset = 'X-offset of the surface (Y-plane)' + 'X offset for U(Cb)'	
		For TileYS and TileYF this offset should be integral multiple of Tile width of Luma plane.	
		Programming Notes	
		For PLANAR_420 and PLANAR_422 surface formats, this field must indicate an even number of pixels.	
	15:14	Reserved	
		Format:	MBZ
	13:0	Y Offset for U(Cb)	
		Format:	U14 Row Offset
		Description	
		For non planar surfaces this field specifies the vertical offset in pixels from the Surface Base Address to the start (origin) of the surface.	
		For Planar surfaces this field specifies the vertical offset in rows from the Y-plane origin to the start (origin) of the U(Cb) plane or the interleaved UV plane if Interleave Chroma is enabled. Resultant X-offset = 'Y-offset of the surface (Y-plane)' + 'Y offset for U(Cb)'	
		For TileYS and TileYF this offset should be integral multiple of Tile width of Luma plane.	
		Programming Notes	
		This field must be aligned by 4 bit[1:0] = 00	
		This field must be aligned by 4 bit[1:0] = 00 for all format besides PLANAR_420_*	
4	31:30	Reserved	
		Format:	MBZ
	29:16	X Offset for V(Cr)	
		Exists If:	///([Surface Format] is one of planar) AND ([Interleave Chroma] == '0')
		Format:	U14 Pixel Offset



MEDIA_SURFACE_STATE		
		Description For Planar surfaces this field specifies the horizontal offset in pixels from the Y-plane origin to the start (origin) of the V(Cb) plane. Resultant X-offset = 'X-offset of the surface (Y-plane)' + 'X offset for V(Cb)' For TileYS and TileYF this offset should be integral multiple of Tile width of Luma plane.
		Programming Notes For PLANAR_420 and PLANAR_422 surface formats, this field must indicate an even number of pixels.
	15	Reserved Format: MBZ
	14:0	Y Offset for V(Cr) Exists If: $(((\text{Surface Format}] \text{ is one of planar}) \text{ AND } ([\text{Interleave Chroma}] == '0'))$ Format: U15 Row Offset
		Description For Planar surfaces this field specifies the vertical offset in rows from the Y-plane origin to the start (origin) of the V(Cb) plane. Resultant Y-offset = 'Y-offset of the surface (Y-plane)' + 'Y offset for V(Cb)' For TileYS and TileYF this offset should be integral multiple of Tile width of Luma plane.
		Programming Notes This field must indicate a multiple of 4 (bit 0 & 1 = 00).
5	31	Vertical Line Stride Format: U1 in lines to skip between logically adjacent lines For Surfaces accessed via the sample_8x8 message: Specifies number of lines (0 or 1) to skip between logically adjacent lines - provides support of interleaved (field) surfaces as textures. For Other Surfaces: Vertical Line Stride must be zero.
	30	Vertical Line Stride Offset Format: U1 in lines of initial offset (when Vertical Line Stride == 1) For Surfaces accessed via the sample_8x8 message: Specifies the offset of the initial line from the beginning of the buffer. For Other Surfaces: Vertical Line Stride Offset must be zero.
		Programming Notes This field must be set to 0 if Vertical Line Stride is 0.
	29:24	Reserved Format: MBZ
	23:20	Reserved



MEDIA_SURFACE_STATE																	
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ													
Format:	MBZ																
19:18	Tiled Resource Mode																
	<table><tr><td>Format:</td><td>U2</td></tr></table>		Format:	U2													
	Format:	U2															
	For Sampling Engine, Render Target, and Typed/Untyped Surfaces: This field specifies the tiled resource mode.																
	For other surfaces: This field is ignored.																
	<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>TRMODE_NONE</td><td>No tiled resource</td></tr><tr><td>1h</td><td>TRMODE_TILEYF</td><td>4KB tiled resources</td></tr><tr><td>2h</td><td>TRMODE_TILEYS</td><td>64KB tiled resources</td></tr><tr><td>3h</td><td>Reserved</td><td></td></tr></table>	Value	Name	Description	0h	TRMODE_NONE	No tiled resource	1h	TRMODE_TILEYF	4KB tiled resources	2h	TRMODE_TILEYS	64KB tiled resources	3h	Reserved		
	Value	Name	Description														
	0h	TRMODE_NONE	No tiled resource														
	1h	TRMODE_TILEYF	4KB tiled resources														
	2h	TRMODE_TILEYS	64KB tiled resources														
3h	Reserved																
Programming Notes																	
If Tile Mode is not set to TILEMODE_YMAJOR, this field must be set to TRMODE_NONE.																	
If this field is not set to TRMODE_NONE, the Surface Format must be one with 8, 16, 32, 64, or 128 bits per element, or one of the compressed texture modes (BC*, ETC*, EAC*, ASTC*). Additionally, YCRCB* formats are supported and treated as 16 bits per element, and the PLANAR_420_8 and PLANAR_422_8 formats are supported and treated as 8 bits per element on the Y plane and 16 bits per element on the UV plane (if Interleave Chroma is enabled) or 8 bits per element on the U and V planes (if Interleave Chroma is disabled).																	
17:7	Reserved																
<table><tr><td>Format:</td><td>MBZ</td></tr></table>		Format:	MBZ														
Format:	MBZ																
6:0	Surface Memory Object Control State																
	<table><tr><td>Default Value:</td><td>0h DefaultVaueDesc</td></tr></table>	Default Value:	0h DefaultVaueDesc														
	Default Value:	0h DefaultVaueDesc															
	<table><tr><td>Format:</td><td>MEMORY_OBJECT_CONTROL_STATE</td></tr></table>	Format:	MEMORY_OBJECT_CONTROL_STATE														
Format:	MEMORY_OBJECT_CONTROL_STATE																
This 7-bit field is used in various state commands and indirect state objects to define cacheability and other attributes related to memory objects.																	
6	31:0	Surface Base Address															
		<table><tr><td>Format:</td><td>GraphicsAddress[31:0]</td></tr></table>	Format:	GraphicsAddress[31:0]													
		Format:	GraphicsAddress[31:0]														
		Specifies the low 32 bits of the byte-aligned base address of the surface.															
		Programming Notes															
For SURFTYPE_BUFFER render targets, this field specifies the base address of first element of the surface. The surface is interpreted as a simple array of that single element type. The address must be naturally-aligned to the element size (e.g., a buffer containing R32G32B32A32_FLOAT elements must be 16-byte aligned).For SURFTYPE_BUFFER non-rendertarget surfaces, this field specifies the base address of the first element of the surface, computed in software by adding the surface base address to the byte offset of the element in the buffer.Mipmapped, cube and 3D sampling engine surfaces are stored in a 'monolithic' (fixed) format, and only require a																	



MEDIA_SURFACE_STATE				
		single address for the base texture.Linear render target surface base addresses must be element-size aligned, for non-YUV surface formats, or a multiple of 2 element-sizes for YUV surface formats. Other linear surfaces have no alignment requirements (byte alignment is sufficient.)Linear depth buffer surface base addresses must be 64-byte aligned. Note that while render targets (color) can be SURFTYPE_BUFFER, depth buffers cannot.Tiled surface base addresses must be 4KB-aligned. Note that only the offsets from Surface Base Address are tiled, Surface Base Address itself is not transformed using the tiling algorithm.For tiled surfaces, the actual start of the surface can be offset from the Surface Base Address by the X Offset and Y Offset fields.Certain message types used to access surfaces have more stringent alignment requirements. Please refer to the specific message documentation for additional restrictions.		
7	31:16	Reserved		
		<table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ
	Format:	MBZ		
15:0	Surface Base Address High			
		<table><tr><td>Format:</td><td>GraphicsAddress[47:32]</td></tr></table> Specifies the high 16 bits of the byte-aligned base address of the surface. Refer to Surface Base Address [31:0] for programming notes applying to this field.	Format:	GraphicsAddress[47:32]
Format:	GraphicsAddress[47:32]			



Power Clock State Format

Power Clock State Format				
Source:		RenderCS		
Size (in bits):		31		
Default Value:		0x00000266		
Known Uses				
- R_PWR_CLK_STATE - Render Power Clock State Register - PM_PWR_CLK_STATE - PM Power Clock State Request (Intended, in GT/GTI space, not yet in use) - PM_PWR_CLK_STATE (Intended, in GT/GTI space, not yet in use)				
DWord	Bit	Description		
0	30:19	RSVD		
		Access:		RO
		Format:		MBZ
		Reserved (CSunit implements full 32b storage)		
	18:15	Reserved		
		Format:		MBZ
	14:13	RSVD		
		Access:		RO
		Reserved (CSunit implements full 32b storage)		
	12	Spare		
		Access:		R/W
		Format:		MBZ
		Spare bit		
	11	SSCountEn		
		Access:		R/W
		Enable Subslice Count Request.		
		Value	Name	Description
		0h	Disable	Use async PMunit subslice count request.
		1h	Enable	Use SliceCount from this register.
	10:8	SScount		
Access:		R/W		
Number of subslices to power.				
Value		Name	Description	
001b			1 subslice.	
010b			2 subslices.	
100b		[Default]	3 subslices.	



Power Clock State Format

	7:4	EUmax	
		Access:	R/W
		Maximum number of EUs to power (per subslice if multiple subslices enabled). To specify an exact number of subslices, set EUmax equal to EUmin.	
		Value	Name
		0010b	2 EUs
		0100b	4 EUs
		0110b	[Default] 6 EUs
		Programming Notes	
		EUmin and EUmax need to be even and odd numbers are illegal; hardware will clip odd EU counts to an even value.	
	3:0	EUmin	
		Access:	R/W
		Minimum number of EUs to power (per subslice if multiple subslices enabled).	
		Value	Name
		0010b	2 EUs
		0100b	4 EUs
		0110b	[Default] 6 EUs
		Programming Notes	
		EUmin and EUmax need to be even and odd numbers are illegal; hardware will clip odd EU counts to an even value.	



RENDER SURFACE STATE

Source:	BSpec			
Exists If:	//[MessageType] != 'Sample_8x8'			
Size (in bits):	512			
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000, 0x00000000			
This is the normal surface state used by all messages that use SURFACE_STATE except those that use MEDIA_SURFACE_STATE.				
DWord	Bit	Description		
0	31:29	Surface Type This field defines the type of the surface.		
		Value	Name	Description
		0h	SURFTYPE_1D	Defines a 1-dimensional map or array of maps
		1h	SURFTYPE_2D	Defines a 2-dimensional map or array of maps
		2h	SURFTYPE_3D	Defines a 3-dimensional (volumetric) map
		3h	SURFTYPE_CUBE	Defines a cube map or array of cube maps
		4h	SURFTYPE_BUFFER	Defines an element in a buffer
		5h	SURFTYPE_STRBUF	Defines a structured buffer surface
		6h	Reserved	
		7h	SURFTYPE_NULL	Defines a null surface
		Programming Notes		
		A null surface is used in instances where an actual surface is not bound. When a write message is generated to a null surface, no actual surface is written to. When a read message (including any sampling engine message) is generated to a null surface, the result is all zeros. Note that a null surface type is allowed to be used with all messages, even if it is not specifically indicated as supported. All of the remaining fields in surface state are ignored for null surfaces, with the following exceptions:		
		• Width, Height, Depth, LOD, and Render Target View Extent fields must match the depth buffer's corresponding state for all render target surfaces, including null.		
		All sampling engine and data port messages support null surfaces with the above behavior, even if not mentioned as specifically supported, except for the following:		
• Data Port Media Block Read/Write messages • Data Port Transpose Read message • The Surface Type of a surface used as a render target (accessed via the Data Port's Render Target Write message) must be the same as the Surface Type of all other render targets and of the depth buffer (defined in 3DSTATE_DEPTH_BUFFER), unless either the depth buffer				



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		or render targets are SURFETYPE_NULL.
28	Surface Array	
	Format:	Enable
	This field, if enabled, indicates that the surface is an array.	
	Programming Notes If this field is <i>enabled</i> , the Surface Type must be SURFETYPE_1D, SURFETYPE_2D, or SURFETYPE_CUBE. If this field is <i>disabled</i> and Surface Type is SURFETYPE_1D, SURFETYPE_2D, or SURFETYPE_CUBE, the Depth field must be set to zero.	
27	ASTC_Enable	
	Format:	Enable
	This field, if enabled, indicates that the surface is one of ASTC compression formats.	
	Programming Notes If this field is <i>enabled</i> , the definition of Surface Format encoding will follow a new convention defined by ASTC. If this field is <i>disabled</i> , the definition of Surface Format will follow the legacy convention defined in non-ASTC style.	
26:18	Surface Format	
	Format:	SURFACE_FORMAT
	Description This field specifies the format of the surface or element within this surface. This field is ignored for all data port messages other than the render target message and streamed vertex buffer write message. Some forms of the media block messages use the surface format. If ASTC_Enable is set to 0, the supported formats and their encoding is listed in the table (x) in Section (y); Otherwise the supported formats and their encoding is listed in the table (x+1) in Section (y).	
	Programming Notes If ASTC_Enable is set to 0: YUV (YCRCB) surfaces used as render targets can only be rendered to using 3DPRIM_RECTLIST with even X coordinates on all of its vertices, and the pixel shader cannot kill pixels. If Number of Multisamples is set to a value other than MULTISAMPLECOUNT_1, this field cannot be set to the following formats: - Any compressed texture format (BC*, DXT*, FXT*, ETC*, EAC*) - Any YCRCB* format This field cannot ASTC format if the Surface Type is SURFETYPE_BUFFER or SURFETYPE_STRBUF This field cannot be ASTC format if the Surface Type is SURFETYPE_1D.	



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This field cannot be a YUV (YCRCB*) or compressed (BC*, DXT*, FXT*, ETC*, EAC*) format if the **Surface Type** is SURFTYPE_BUFFER or SURFTYPE_STRBUF.
This field cannot be a planar YUV (PLANAR_*) or compressed (BC*, DXT*, FXT*, ETC*, EAC*) format if the **Surface Type** is SURFTYPE_1D.

17:16 Surface Vertical Alignment

Description

For Sampling Engine and Render Target Surfaces: This field specifies the vertical alignment requirement in elements for the surface. Refer to the "Memory Data Formats" chapter for details on how this field changes the layout of the surface in memory. An *element* is defined as a pixel in uncompressed surface formats, and as a compression block in compressed surface formats. For MSFMT_DEPTH_STENCIL type multisampled surfaces, an element is a sample.

This field is used for 2D, CUBE, and 3D surface alignment when Tiled Resource Mode is TRMODE_NONE (Tiled Resource Mode is disabled). This field is ignored for 1D surfaces and also when Tiled Resource Mode is not TRMODE_NONE (e.g. Tiled Resource Mode is enabled). See the appropriate Alignment table in the "Surface Layout and Tiling" section under Common Surface Formats for the table of alignment values for Tiled Resources.

For other surfaces: This field is ignored.

Value	Name	Description
0h	Reserved	Reserved
1h	VALIGN 4	Vertical alignment factor j = 4
2h	VALIGN 8	Vertical alignment factor j = 8
3h	VALIGN 16	Vertical alignment factor j = 16

Programming Notes

This field is intended to be set to VALIGN_4 if the surface was rendered as a depth buffer, for a multisampled (4x) render target, or for a multisampled (8x) render target, since these surfaces support only alignment of 4. Use of VALIGN_4 for other surfaces is supported, but increases memory usage.

This field is intended to be set to VALIGN_8 only if the surface was rendered as a stencil buffer, since stencil buffer surfaces support only alignment of 8. If set to VALIGN_8, Surface Format must be R8_UINT.

For uncompressed surfaces, the units of "j" are rows of pixels on the physical surface. For compressed texture formats, the units of "j" are in compression blocks, thus each increment in "j" is equal to h pixels, where h is the height of the compression block in pixels.

15:14 Surface Horizontal Alignment

Description

For Sampling Engine and Render Target Surfaces: This field specifies the horizontal alignment requirement for the surface.



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This field is used for alignment when LOD $\geq$ Mip Tail Start LOD
 This field is ignored when Tiled Resource Mode is not TRMODE_NONE (i.e. Tiled Resources are enabled). See the "Surface Layout and Tiling" section under Common Surface Formats for the table of alignment values for Tile Resources.

For other surfaces:

This field is ignored.

Value	Name	Description
0h	Reserved	Reserved
1h	HALIGN 4	Horizontal alignment factor $j = 4$
2h	HALIGN 8	Horizontal alignment factor $j = 8$
3h	HALIGN 16	Horizontal alignment factor $j = 16$

Programming Notes

This field is intended to be set to HALIGN_8 only if the surface was rendered as a depth buffer with Z16 format or a stencil buffer. In this case it must be set to HALIGN_8 since these surfaces support only alignment of 8. For Z32 formats it must be set to HALIGN_4. Use of HALIGN_8 for other surfaces is supported, but increases memory usage.

For uncompressed surfaces, the units of "i" are pixels on the physical surface. For compressed texture formats, the units of "i" are in compression blocks, thus each increment in "i" is equal to w pixels, where w is the width of the compression block in pixels.

When Auxiliary Surface Mode is set to AUX_CCS_D or AUX_CCS_E, HALIGN 16 must be used.

13:12 Tile Mode

This field specifies the type of memory tiling (Linear, WMajor, XMajor, or YMajor) employed to tile this surface. See *Memory Interface Functions* for details on memory tiling and restrictions.

Value	Name	Description
0h	LINEAR	Linear mode (no tiling)
1h	WMAJOR	W major tiling
2h	XMAJOR	X major tiling
3h	YMAJOR	Y major tiling

Programming Notes

- Refer to *Memory Data Formats* for restrictions on *TileMode* direction for the various buffer types. (Of particular interest is the fact that YMAJOR tiling is not supported for display/overlay buffers).
- The corresponding cache(s) must be invalidated before a previously accessed surface is accessed again with an altered state of this field.
- Use of WMAJOR is valid only for sampling engine, Data Cache Data Port and render target surfaces and **Surface Format** must be R8_UINT. Vertical Line Stride must be zero. In addition to W tiling, this mode implies that the surface is stored as a stencil buffer. Refer to

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		<i>Memory Data Formats</i> section for details on stencil buffer surface layout. - Linear surfaces can be mapped to Main Memory (uncached) or System Memory (cacheable, snooped). Tiled (X/Y/W) surfaces can only be mapped to Main Memory. - If Surface Type is SURFTYPE_BUFFER, this field must be TILEMODE_LINEAR - If Number of Multisamples is not MULTISAMPLECOUNT_1, this field must be YMAJOR. If Surface Type is SURFTYPE_STRBUF, this field must be TILEMODE_LINEAR. If Surface Type is SURFTYPE_1D this field must be TILEMODE_LINEAR, unless Sampler Legacy 1D Map Layout Disable is set to 0, in which case TILEMODE_YMAJOR and TILEMODE_WMAJOR are also allowed. Tiled Resource Mode must be set to TRMODE_NONE for these cases. TILEMODE_XMAJOR is only allowed if Surface Type is SURFTYPE_2D. If Surface Format is ASTC*, this field must be TILEMODE_YMAJOR.
11	Vertical Line Stride	Format: U1 In lines to skip between logically adjacent lines For 2D Non-Array Surfaces accessed via the Sampling Engine or Data Cache Data Port: Specifies number of lines (0 or 1) to skip between logically adjacent lines - provides support of interleaved (field) surfaces as textures. For Other Surfaces: Vertical Line Stride must be zero. Programming Notes This bit must not be set if the surface format is a compressed type (BCn*, FXT1, ETC*, EAC*). This bit must not be set if the surface format is compressed type ASTC*. This bit must not be set if the Auxiliary Surface Mode is not AUX_NONE. If this bit is set on a sampling engine surface, the mip mode filter must be set to MIPFILTER_NONE and the min and mag mode filter cannot be set to MAPFILTER_FLEXIBLE.
10	Vertical Line Stride Offset	Format: U1 In lines of initial offset (when Vertical Line Stride == 1) For 2D Non-Array Surfaces accessed via the Sampling Engine or Data Cache Data Port: Specifies the offset of the initial line from the beginning of the buffer. Ignored when Vertical Line Stride is 0. For Other Surfaces: Vertical Line Stride Offset must be zero.
9	Sampler L2 Out of Order Mode Disable	Format: Disable If disabled this will forced formats which would have bypassed the L2 and been filled into the L1 out of order to be cached in the L2 and send in order to the L1. In general that is any format which is expaned 1:2 in L1 or not expanded at all. This would include all lossless compressed cases For all other formats this will have no affect. Programming Notes This bit must be set for the following surface types: BC2_UNORM BC3_UNORM BC5_UNORM BC5_SNORM BC7_UNORM



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8	Render Cache Read Write Mode For Surfaces accessed via the Data Port to Render Cache: This field specifies the way Render Cache treats a write request. If unset, Render Cache allocates a write-only cache line for a write miss. If set, Render Cache allocates a read-write cache line for a write miss. For Surfaces accessed via the Sampling Engine or Data Port to Texture Cache or Data Cache: This field is reserved : MBZ <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>Write-Only Cache</td><td>Allocating write-only cache for a write miss</td></tr><tr><td>1h</td><td>Read-Write Cache</td><td>Allocating read-write cache for a write miss</td></tr></table> Programming Notes This field is provided for performance optimization for Render Cache read/write accesses (from Gen4 EU's point of view).	Value	Name	Description	0h	Write-Only Cache	Allocating write-only cache for a write miss	1h	Read-Write Cache	Allocating read-write cache for a write miss						
Value	Name	Description														
0h	Write-Only Cache	Allocating write-only cache for a write miss														
1h	Read-Write Cache	Allocating read-write cache for a write miss														
7:6	Media Boundary Pixel Mode For 2D Non-Array Surfaces accessed via the Data Port Media Block Read Message or Data Port Transpose Read message: This field enables control of which rows are returned on vertical out-of-bounds reads using the Data Port Media Block Read Message or Data Port Transpose Read message. In the description below, frame mode refers to Vertical Line Stride = 0, field mode is Vertical Line Stride = 1 in which only the even or odd rows are addressable. The frame refers to the entire surface, while the field refers only to the even or odd rows within the surface. For Other Surfaces: Reserved : MBZ <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>NORMAL_MODE</td><td>The row returned on an out-of-bound access is the closest row in the frame or field. Rows from the opposite field are never returned.</td></tr><tr><td>1h</td><td>Reserved</td><td></td></tr><tr><td>2h</td><td>PROGRESSIVE_FRAME</td><td>The row returned on an out-of-bound access is the closest row in the frame, even if in field mode.</td></tr><tr><td>3h</td><td>INTERLACED_FRAME</td><td>In field mode, the row returned on an out-of-bound access is the closest row in the field. In frame mode, even out-of-bound rows return the nearest even row while odd out-of-bound rows return the nearest odd row.</td></tr></table>	Value	Name	Description	0h	NORMAL_MODE	The row returned on an out-of-bound access is the closest row in the frame or field. Rows from the opposite field are never returned.	1h	Reserved		2h	PROGRESSIVE_FRAME	The row returned on an out-of-bound access is the closest row in the frame, even if in field mode.	3h	INTERLACED_FRAME	In field mode, the row returned on an out-of-bound access is the closest row in the field. In frame mode, even out-of-bound rows return the nearest even row while odd out-of-bound rows return the nearest odd row.
Value	Name	Description														
0h	NORMAL_MODE	The row returned on an out-of-bound access is the closest row in the frame or field. Rows from the opposite field are never returned.														
1h	Reserved															
2h	PROGRESSIVE_FRAME	The row returned on an out-of-bound access is the closest row in the frame, even if in field mode.														
3h	INTERLACED_FRAME	In field mode, the row returned on an out-of-bound access is the closest row in the field. In frame mode, even out-of-bound rows return the nearest even row while odd out-of-bound rows return the nearest odd row.														
5	Cube Face Enable - Negative X <table><tr><td>Exists If:</td><td>[Surface Type] == 'SURFTYPE_CUBE'</td></tr><tr><td>Format:</td><td>Enable</td></tr></table> For SURFTYPE_CUBE Surfaces accessed via the Sampling Engine: This field enable the individual face of a cube map. Enabling a face indicates that the face is present in the cube map, while disabling it indicates that that face is represented by the texture map's border color. Refer to Memory Data Formats for the correlation between faces and the cube map	Exists If:	[Surface Type] == 'SURFTYPE_CUBE'	Format:	Enable											
Exists If:	[Surface Type] == 'SURFTYPE_CUBE'															
Format:	Enable															



RENDER_SURFACE_STATE

		memory layout. Note that storage for disabled faces must be provided.
		Programming Notes
		When TEXCOORDMODE_CLAMP is used when accessing a cube map, this field must be programmed to 1b (face enabled).
4	Cube Face Enable - Positive X	
	Exists If:	[Surface Type] == 'SURFTYPE_CUBE'
	Format:	Enable
	For SURFTYPE_CUBE Surfaces accessed via the Sampling Engine: This field enable the individual face of a cube map. Enabling a face indicates that the face is present in the cube map, while disabling it indicates that that face is represented by the texture map's border color. Refer to Memory Data Formats for the correlation between faces and the cube map memory layout. Note that storage for disabled faces must be provided.	
		Programming Notes
		When TEXCOORDMODE_CLAMP is used when accessing a cube map, this field must be programmed to 1b (face enabled).
3	Cube Face Enable - Negative Y	
	Exists If:	[Surface Type] == 'SURFTYPE_CUBE'
	Format:	Enable
	For SURFTYPE_CUBE Surfaces accessed via the Sampling Engine: This field enable the individual face of a cube map. Enabling a face indicates that the face is present in the cube map, while disabling it indicates that that face is represented by the texture map's border color. Refer to Memory Data Formats for the correlation between faces and the cube map memory layout. Note that storage for disabled faces must be provided.	
		Programming Notes
		When TEXCOORDMODE_CLAMP is used when accessing a cube map, this field must be programmed to 1b (face enabled).
2	Cube Face Enable - Positive Y	
	Exists If:	[Surface Type] == 'SURFTYPE_CUBE'
	Format:	Enable
	For SURFTYPE_CUBE Surfaces accessed via the Sampling Engine: This field enable the individual face of a cube map. Enabling a face indicates that the face is present in the cube map, while disabling it indicates that that face is represented by the texture map's border color. Refer to Memory Data Formats for the correlation between faces and the cube map memory layout. Note that storage for disabled faces must be provided.	
		Programming Notes
		When TEXCOORDMODE_CLAMP is used when accessing a cube map, this field must be programmed to 1b (face enabled).



RENDER_SURFACE_STATE			
	1	Cube Face Enable - Negative Z	
		Exists If:	[Surface Type] == 'SURFTYPE_CUBE'
		Format:	Enable
		For SURFTYPE_CUBE Surfaces accessed via the Sampling Engine: This field enable the individual face of a cube map. Enabling a face indicates that the face is present in the cube map, while disabling it indicates that that face is represented by the texture map's border color. Refer to Memory Data Formats for the correlation between faces and the cube map memory layout. Note that storage for disabled faces must be provided.	
		Programming Notes When TEXCOORDMODE_CLAMP is used when accessing a cube map, this field must be programmed to 1b (face enabled).	
	5:0	Reserved	
		Exists If:	[Surface Type] != 'SURFTYPE_CUBE'
		Format:	MBZ
	0	Cube Face Enable - Positive Z	
		Exists If:	[Surface Type] == 'SURFTYPE_CUBE'
Format:		Enable	
For SURFTYPE_CUBE Surfaces accessed via the Sampling Engine: This field enable the individual face of a cube map. Enabling a face indicates that the face is present in the cube map, while disabling it indicates that that face is represented by the texture map's border color. Refer to Memory Data Formats for the correlation between faces and the cube map memory layout. Note that storage for disabled faces must be provided.			
Programming Notes When TEXCOORDMODE_CLAMP is used when accessing a cube map, this field must be programmed to 1b (face enabled).			
1	31	Reserved	
		Format:	MBZ
	30:24	Memory Object Control State	
	Format:	MEMORY_OBJECT_CONTROL_STATE	
	Specifies the memory object control state for this surface and the associated Auxiliary surface (if any).		



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23:19	Base Mip Level	
	Format:	U4.1
	Range: [0.0, 14.0]	
	Specifies which mip level is considered the "base" level when determining mag-vs-min filter and selecting the "base" mip level.	
	Programming Notes	
	This field also exists in SAMPLER_STATE. If both fields are zero, the Base Mip Level is zero. If one is nonzero, Base Mip Level is the nonzero field. It is illegal to have both Base Mip Level fields nonzero.	
18	Reserved	
	Format:	MBZ
17	Reserved	
	Format:	MBZ
16	Reserved	
	Format:	MBZ
15	Reserved	
	Format:	MBZ
14:0	Surface QPitch	
	Format:	QPitch[16:2]
	Description	
	The interpretation of this field is dependent on Surface Type as follows:	
	- SURFTYPE_1D: distance in <i>pixels</i> between array slices - SURFTYPE_2D/CUBE: distance in <i>rows</i> between array slices. For Quilted Textures this field specifies the distance in rows between <i>quilt</i> slices. For compressed texture formats, one row contains a complete compression block vertically. - SURFTYPE_3D: distance in <i>rows</i> between R-slices [Note: these <i>rows</i> are only in the vertical dimension without considering the depth dimension]. For compressed texture formats, one row contains a complete compression block vertically. - Other surface types: field is ignored	
	Value	Name
	[4h,1FFFCh]	
	in multiples of 4 (low 2 bits missing)	
	Programming Notes	
	For Surface Type 1D: This field must be set to an integer multiple of the Surface Horizontal	



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		Alignment For Surface Type 2D, CUBE: This field must be set to an integer multiple of the Surface Vertical Alignment For Surface Type 3D: <i>Tile Mode != Linear:</i> This field must be set to an integer multiple of the tile height (2^{Cv}) <i>Tile Mode == Linear:</i> This field must be set to an integer multiple of the Surface Vertical Alignment Note: for compressed textures (BC*, FXT1, ETC*, EAC*), this field is in units of rows of compression blocks. Note: for the compressed texture ASTC Surface Format, this field is in units of rows of compression blocks. Software must ensure that this field is set to a value sufficiently large such that the array slices in the surface do not overlap. Refer to the Memory Data Formats section for information on how surfaces are stored in memory.																										
2	31:30	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ																								
Format:	MBZ																											
	29:16	Height <table><tr><td>Format:</td><td>U14-1</td></tr></table> This field specifies the height of the surface, minus 1. If the surface is MIP-mapped, this field contains the height of the base MIP level. For buffers, this field specifies a portion of the buffer size. <table><thead><tr><th>Value</th><th>Name</th><th>Description</th><th>Exists If</th></tr></thead><tbody><tr><td>[0,0]</td><td></td><td>must be zero</td><td>[Surface Type] == 'SURFTYPE_1D'</td></tr><tr><td>[0,16383]</td><td></td><td>height of surface - 1 (y/v dimension)</td><td>[SurfaceType] == 'SURFTYPE_2D'</td></tr><tr><td>[0,16383]</td><td></td><td>height of surface - 1 (y/v dimension)</td><td>[SurfaceType] == 'SURFTYPE_3D'</td></tr><tr><td>[0,16383]</td><td></td><td>height of surface - 1 (y/v dimension)</td><td>[SurfaceType] == 'SURFTYPE_CUBE'</td></tr><tr><td>[0,16383]</td><td></td><td>contains bits [20:7] of the number of entries in the buffer - 1</td><td>([SurfaceType] == 'SURFTYPE_BUFFER') ([SurfaceType] == 'SURFTYPE_STRBUF')</td></tr></tbody></table> Programming Notes For typed buffer and structured buffer surfaces, the number of entries in the buffer ranges from 1 to 2^{27}. For raw buffer surfaces, the number of entries in the buffer is the number of bytes which can range from 1 to 2^{30}. After subtracting one from the number of entries, software must place the fields of the resulting 27-bit value into the Height, Width, and Depth fields as indicated, right-justified in each field. Unused upper bits must be set to zero. If Vertical Line Stride is 1, this field indicates the height of the field, not the height of the frame The Height of a render target must be the same as the Height of the other render targets and the depth buffer (defined in 3DSTATE_DEPTH_BUFFER), unless Surface Type is SURFTYPE_1D or SURFTYPE_2D with Depth = 0 (non-array) and LOD = 0 (non-mip mapped).	Format:	U14-1	Value	Name	Description	Exists If	[0,0]		must be zero	[Surface Type] == 'SURFTYPE_1D'	[0,16383]		height of surface - 1 (y/v dimension)	[SurfaceType] == 'SURFTYPE_2D'	[0,16383]		height of surface - 1 (y/v dimension)	[SurfaceType] == 'SURFTYPE_3D'	[0,16383]		height of surface - 1 (y/v dimension)	[SurfaceType] == 'SURFTYPE_CUBE'	[0,16383]		contains bits [20:7] of the number of entries in the buffer - 1	([SurfaceType] == 'SURFTYPE_BUFFER') ([SurfaceType] == 'SURFTYPE_STRBUF')
Format:	U14-1																											
Value	Name	Description	Exists If																									
[0,0]		must be zero	[Surface Type] == 'SURFTYPE_1D'																									
[0,16383]		height of surface - 1 (y/v dimension)	[SurfaceType] == 'SURFTYPE_2D'																									
[0,16383]		height of surface - 1 (y/v dimension)	[SurfaceType] == 'SURFTYPE_3D'																									
[0,16383]		height of surface - 1 (y/v dimension)	[SurfaceType] == 'SURFTYPE_CUBE'																									
[0,16383]		contains bits [20:7] of the number of entries in the buffer - 1	([SurfaceType] == 'SURFTYPE_BUFFER') ([SurfaceType] == 'SURFTYPE_STRBUF')																									

**RENDER_SURFACE_STATE**

If this surface in memory is accessed with Vertical Line Stride set to both 0 and 1, this field must be an even value when Vertical Line Stride is 0.

If Media Pixel Boundary Mode is not set to NORMAL_MODE, this field must be an even value.

If Surface Format is PLANAR*, see Planar Memory Organization section for restrictions on the value of this field.

15:14

Reserved

Format:

MBZ

13:0

Width

Format:

U14-1

Description

This field specifies the width of the surface, minus 1. If the surface is MIP-mapped, this field specifies the width of the base MIP level. The width is specified in units of pixels or texels. For buffers, this field specifies a portion of the buffer size.

For surfaces accessed with the Media Block Read/Write message, this field is in units of DWords.

For surfaces accessed with the Transpose Read Message, this field is in units of DWords.

Value	Name	Description	Exists If
[0,16383]		width of surface - 1 (x/u dimension)	[SurfaceType] == 'SURFTYPE_1D'
[0,16383]		width of surface - 1 (x/u dimension)	[SurfaceType] == 'SURFTYPE_2D'
[0,16383]		width of surface - 1 (x/u dimension)	[SurfaceType] == 'SURFTYPE_3D'
[0,16383]		width of surface - 1 (x/u dimension)	[SurfaceType] == 'SURFTYPE_CUBE'
[0,127]		contains bits [6:0] of the number of entries in the buffer - 1	([SurfaceType] == 'SURFTYPE_BUFFER') ([SurfaceType] == 'SURFTYPE_STRBUF')

Programming Notes

- For surface types other than SURFTYPE_BUFFER or STRBUF The Width specified by this field must be less than or equal to the surface pitch (specified in bytes via the Surface Pitch field).
- For cube maps, Width must be set equal to the Height.
- For MONO8 textures, Width must be a multiple of 32 texels.
- The **Width** of a render target must be the same as the **Width** of the other render target(s) and the depth buffer (defined in 3DSTATE_DEPTH_BUFFER), unless **Surface Type** is SURFTYPE_1D or SURFTYPE_2D with **Depth** = 0 (non-array) and **LOD** = 0 (non-mip mapped).



RENDER_SURFACE_STATE																																			
		- The Width of a render target with YUV surface format must be a multiple of 2. - For SURFTYPE_BUFFER: The low two bits of this field must be 11 if the Surface Format is RAW (the size of the buffer must be a multiple of 4 bytes).																																	
		If Surface Format is PLANAR*, this field must be a multiple of 2																																	
		If Number of Multisamples is MULTISAMPLECOUNT_16, then Width must be 8K texels or less, or the surface must not use the a multisample control surface (MCS).																																	
3	31:21	Depth <table><tr><td>Format:</td><td>U11-1</td></tr><tr><td colspan="2">This field specifies the total number of levels, minus 1, for a volume texture or the number of array elements, minus 1, allowed to be accessed starting at the Minimum Array Element for arrayed surfaces. If the volume texture is MIP-mapped, this field specifies the depth of the base MIP level. For buffers, this field specifies a portion of the buffer size.</td></tr><tr><th>Value</th><th>Name</th><th>Description</th><th>Exists If</th></tr><tr><td>[0,2047]</td><td></td><td>number of array elements - 1</td><td>[SurfaceType] == 'SURFTYPE_1D'</td></tr><tr><td>[0,2047]</td><td></td><td>number of array elements - 1</td><td>[SurfaceType] == 'SURFTYPE_2D'</td></tr><tr><td>[0,2047]</td><td></td><td>depth of surface - 1 (z/r dimension)</td><td>[SurfaceType] == 'SURFTYPE_3D'</td></tr><tr><td>[0,340]</td><td></td><td>number of array elements - 1 [see programming notes for range]</td><td>[SurfaceType] == 'SURFTYPE_CUBE'</td></tr><tr><td>[0,511]</td><td></td><td>contains bits [29:21] of the number of entries in the buffer - 1</td><td>([SurfaceType] == SURFTYPE_BUFFER) OR ([SurfaceType] == 'SURFTYPE_STRBUF')</td></tr></table> <table><tr><th>Programming Notes</th></tr><tr><td>The Depth of a render target must be the same as the Depth of the other render target(s) and of the depth buffer (defined in 3DSTATE_DEPTH_BUFFER).</td></tr><tr><td>For SURFTYPE_CUBE: For Sampling Engine Surfaces and Typed Data Port Surfaces, the range of this field is [0,340], indicating the number of cube array elements (equal to the number of underlying 2D array elements divided by 6). For other surfaces, this field must be zero.</td></tr><tr><td>For SURFTYPE_1D, 2D, and CUBE: The range of this field is reduced by one for each increase from zero of Minimum Array Element. For example, if Minimum Array Element is set to 1024 on a 2D surface, the range of this field is reduced to [0,1023].</td></tr></table>		Format:	U11-1	This field specifies the total number of levels, minus 1, for a volume texture or the number of array elements, minus 1, allowed to be accessed starting at the Minimum Array Element for arrayed surfaces. If the volume texture is MIP-mapped, this field specifies the depth of the base MIP level. For buffers, this field specifies a portion of the buffer size.		Value	Name	Description	Exists If	[0,2047]		number of array elements - 1	[SurfaceType] == 'SURFTYPE_1D'	[0,2047]		number of array elements - 1	[SurfaceType] == 'SURFTYPE_2D'	[0,2047]		depth of surface - 1 (z/r dimension)	[SurfaceType] == 'SURFTYPE_3D'	[0,340]		number of array elements - 1 [see programming notes for range]	[SurfaceType] == 'SURFTYPE_CUBE'	[0,511]		contains bits [29:21] of the number of entries in the buffer - 1	([SurfaceType] == SURFTYPE_BUFFER) OR ([SurfaceType] == 'SURFTYPE_STRBUF')	Programming Notes	The Depth of a render target must be the same as the Depth of the other render target(s) and of the depth buffer (defined in 3DSTATE_DEPTH_BUFFER).	For SURFTYPE_CUBE: For Sampling Engine Surfaces and Typed Data Port Surfaces, the range of this field is [0,340], indicating the number of cube array elements (equal to the number of underlying 2D array elements divided by 6). For other surfaces, this field must be zero.	For SURFTYPE_1D, 2D, and CUBE: The range of this field is reduced by one for each increase from zero of Minimum Array Element . For example, if Minimum Array Element is set to 1024 on a 2D surface, the range of this field is reduced to [0,1023].
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RENDER_SURFACE_STATE										
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	Reserved									
	Format:	MBZ								
	17:0	<table><tr><td colspan="2">Surface Pitch</td></tr><tr><td>Format:</td><td>U18-1 Pitch in #Bytes</td></tr></table> Surface Pitch Range: - For surfaces of type SURFTYPE_BUFFER: [0,2047] -> [1B, 2048B] - For surfaces of type SURFTYPE_STRBUF: [0,2047] -> [1B, 2048B] - For other linear surfaces: [0, 262143] -> [1B, 256KB] - For X-tiled surface: [511, 262143] -> [512B, 256KB] = [1 tile, 512 tiles] - For Y-tiled surfaces: [127, 262143]->[128B, 256KB] = [1 tile, 2048 tiles] - For W-tiled surfaces: [127, 262143]->[128B, 256KB] = [1 tile, 2048 tiles] - For TileYF and TileYS surfaces, the range is dependent on the Cu parameter (refer to <i>Memory Data Formats</i> section for the definition of the Cu parameter depending on the case). The range in bytes is [2^{Cu}-1,262143] -> [(2^{Cu})B,256KB] = [1 tile, 256KB/(2^{Cu}) tiles] This field specifies the surface pitch in (#Bytes - 1). For surfaces of type SURFTYPE_BUFFER and SURFTYPE_STRBUF, this field indicates the size of the structure. <table><tr><th>Programming Notes</th></tr><tr><td> - For linear <i>render target</i> surfaces and surfaces accessed with the typed data port messages, the pitch must be a multiple of the element size for non-YUV surface formats. Pitch must be a multiple of 2 * element size for YUV surface formats. - For untyped data port messages, which are only supported with Surface Type SURFTYPE_BUFFER, the pitch is ignored and assumed to be 1 byte. - For linear surfaces with Surface Type of SURFTYPE_STRBUF, the pitch must be a multiple of 4 bytes. - For linear surfaces with Surface Type of SURFTYPE_BUFFER and Surface Format RAW, the pitch must be 1 byte. - For other linear surfaces, the pitch can be any multiple of bytes. - For tiled surfaces, the pitch must be a multiple of the tile width. </td></tr><tr><td> If the surface is a stencil buffer (and thus has Tile Mode set to TILEMODE_WMAJOR), the pitch must be set to 2x the value computed based on width, as the stencil buffer is stored with two rows interleaved. For details on the separate stencil buffer storage format in memory, see GPU Overview (vol1a), Memory Data Formats, Surface Layout, 2D Surfaces, Stencil Buffer Layout (section 8.20.4.8). </td></tr><tr><td> - The width of a tile depends on the surface format if Tiled Resource Enable is enabled. Refer to the Tiled Resource Enable field to determine which sub-mode applies to the surface format in use, and determine the Cu parameter from the Surface Layout section. The tile width is equal to 2^{Cu} bytes. - For surfaces of type SURFTYPE_1D, this field is ignored. </td></tr></table>	Surface Pitch		Format:	U18-1 Pitch in #Bytes	Programming Notes	- For linear <i>render target</i> surfaces and surfaces accessed with the typed data port messages, the pitch must be a multiple of the element size for non-YUV surface formats. Pitch must be a multiple of 2 * element size for YUV surface formats. - For untyped data port messages, which are only supported with Surface Type SURFTYPE_BUFFER, the pitch is ignored and assumed to be 1 byte. - For linear surfaces with Surface Type of SURFTYPE_STRBUF, the pitch must be a multiple of 4 bytes. - For linear surfaces with Surface Type of SURFTYPE_BUFFER and Surface Format RAW, the pitch must be 1 byte. - For other linear surfaces, the pitch can be any multiple of bytes. - For tiled surfaces, the pitch must be a multiple of the tile width.	If the surface is a stencil buffer (and thus has Tile Mode set to TILEMODE_WMAJOR), the pitch must be set to 2x the value computed based on width, as the stencil buffer is stored with two rows interleaved. For details on the separate stencil buffer storage format in memory, see GPU Overview (vol1a), Memory Data Formats, Surface Layout, 2D Surfaces, Stencil Buffer Layout (section 8.20.4.8).	- The width of a tile depends on the surface format if Tiled Resource Enable is enabled. Refer to the Tiled Resource Enable field to determine which sub-mode applies to the surface format in use, and determine the Cu parameter from the Surface Layout section. The tile width is equal to 2^{Cu} bytes. - For surfaces of type SURFTYPE_1D, this field is ignored.
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The following table indicates the maximum byte width, frame width, and pitch size allowed when memory compression is on.

Tiling Mode	Pixel Format	Max Frame Width (bytes)	Max Frame Width (pixels)	Max Pitch (bytes)
Legacy 4K	8bpp	16k	16k	16k + 127
	16bpp	16k	8k	16k + 127
	32bpp	16k	4k	16k + 127
	64bpp	16k	2k	16k + 127
	128bpp	16k	1k	16k + 127
TileYF	8bpp	8k	8k	8k + 63
	16bpp	16k	8k	16k + 127
	32bpp	16k	4k	16k + 127
	64bpp	16k	2k	16k + 255
	128bpp	16k	1k	16k + 255
TileYS	8bpp	16k	16k	16k + 255
	16bpp	16k	8k	16k + 511
	32bpp	16k	4k	16k + 511
	64bpp	16k	2k	16k + 1023
	128bpp	16k	1k	16k + 1023

4

31

Reserved

Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'
Format:	MBZ

30:29

Render Target And Sample Unorm Rotation

Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'

Description

For Render Target Surfaces:

This field specifies the rotation of this render target surface when being written to memory.

For sample_unorm Messages: This field specifies the rotation of the data returned by sampler for sample_unorm message.

For Other Surfaces:

This field is ignored.

Value	Name	Description
0h	0DEG	No rotation (0 degrees)
1h	90DEG	Rotate by 90 degrees
2h	180DEG	Rotate by 180 degrees [for sample_unorm message]

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		3h	270DEG	Rotate by 270 degrees
		Programming Notes		
		Programming Notes for Render Target Surfaces only - Rotation is not supported for render targets of any type other than simple, non-mip-mapped, non-array 2D surfaces. The surface must be using tiled with X major. Width and Height fields apply to the dimensions of the surface before rotation. - For 90 and 270 degree rotated surfaces, the Height (rather than the Width) must be less than or equal to the Surface Pitch (specified in bytes). - For 90 and 270 degree rotated surfaces, the actual Height and Width of the surface in pixels (not the field value which is decremented) must both be even.		
		Rotation is supported only for surfaces with the following surface formats: B5G6R5_UNORM, B5G6R5_UNORM_SRGB, R8G8B8A8_UNORM, R8G8B8A8_UNORM_SRGB, B8G8R8[A]X8_UNORM, B8G8R8[A]X8_UNORM_SRGB, B10G10R10[A]X2_UNORM, B10G10R10A2_UNORM_SRGB, R10G10B10A2_UNORM, R10G10B10A2_UNORM_SRGB, R16G16B16A16_FLOAT, R16G16B16X16_FLOAT		
28:18	Minimum Array Element			
	Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'		
	Format:	U11		
17:7	Render Target View Extent			
	Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'		
	Format:	U11-1		
	Range [0,2047] to indicate extent of [1,2048]			
	For Render Target and Typed Dataport 3D Surfaces:			
	This field indicates the extent of the accessible 'R' coordinates minus 1 on the LOD currently being rendered to.			
	For Render Target and Typed Dataport 1D and 2D Surfaces:			
	This field must be set to the same value as the Depth field.			
	For Other Surfaces:			
	This field is ignored.			
6	Multisampled Surface Storage Format			
	Exists If:	[Surface Type] != 'SURFTYPE_STRBUF'		
	This field indicates the storage format of the multisampled surface.			
	Value	Name	Description	
	0h	MSS	Multisampled surface was/is rendered as a render target	
	1h	DEPTH_STENCIL	Multisampled surface was rendered as a depth or stencil buffer	



RENDER_SURFACE_STATE																												
		<table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2"> - All multisampled render target surfaces must have this field set to MSFMT_MSS - IF this field is MSFMT_DEPTH_STENCIL, the only sampling engine messages allowed are "ld2dms", "resinfo", and "sampleinfo". - This field is ignored if Number of Multisamples is MULTISAMPLECOUNT_1 </td></tr></table>	Programming Notes		- All multisampled render target surfaces must have this field set to MSFMT_MSS - IF this field is MSFMT_DEPTH_STENCIL, the only sampling engine messages allowed are "ld2dms", "resinfo", and "sampleinfo". - This field is ignored if Number of Multisamples is MULTISAMPLECOUNT_1																							
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resolution.

Value	Name	Description
[0,508]		In multiples of 4 (low 2 bits missing)

Programming Notes

- For linear surfaces, this field must be zero.
- For surfaces accessed with the *Data Port Media Block Read/Write* message, the pixel size is assumed to be 32 bits in width.
- For surfaces accessed with the **Data Port Transpose Read message**, the pixel size is assumed to be 32 bits in width.
- For **Surface Format** with other than 8, 16, 32, 64, or 128 bits per pixel, this field must be zero.
- If **Render Target Rotation** is set to other than RTROTATE_0DEG, this field must be zero.
- If **Surface Type** not SURFTYPE_2D, this field must be zero.
- If **MIP Count** is not zero, this field must be zero.
- If **Number of Multisamples** is not MULTISAMPLECOUNT_1, this field must be zero.
- If **Surface Array** is enabled, this field must be zero.
- If **Auxiliary Surface Mode** is not AUX_NONE, this field must be zero.
- If **Surface Vertical Alignment** is VALIGN_8, this field must be a multiple of 8.
- For **Surface Format** with 8 bits per element, this field must be a multiple of 16.
- For **Surface Format** with 16 bits per element, this field must be a multiple of 8.

- If **Tiled Resource Mode** is not TRMODE_NONE, this field must be zero.

24 **Reserved**

Format:	MBZ

23:21 **Y Offset**

Format:	RowOffset[4:2]

This field specifies the vertical offset in rows from the **Surface Base Address** to the start of the surface. (See additional description in the **X Offset** field.)

Value	Name	Description
[0,28]		In multiples of 4 (low two bits missing)

Programming Notes

- For linear surfaces, this field must be zero.
- For render targets in which the **Render Target Array Index** is not zero, this field must be zero.
- For **Surface Format** with other than 8, 16, 32, 64, or 128 bits per pixel, this field must be zero.



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- If **Render Target Rotation** is set to other than RTROTATE_0DEG, this field must be zero.
- If **Surface Type** not SURFTYPE_2D, this field must be zero.
- If **MIP Count** is not zero, this field must be zero.
- If **Number of Multisamples** is not MULTISAMPLECOUNT_1, this field must be zero.
- If **Surface Array** is enabled, this field must be zero.
- If **Auxiliary Surface Mode** is not AUX_NONE, this field must be zero.

- If **Tiled Resource Mode** is not TRMODE_NONE, this field must be zero.

This field must be zero if Surface Format is Planar and the U and V planes are half-pitch (e.g. YV12 format).

20 EWA Disable For Cube

Format: Disable

Specifies if EWA mode for LOD quality improvement needs to be disabled for cube maps.

Value	Name	Description
0h	Enable [Default]	EWA is enabled for cube maps
1h	Disable	EWA is disabled for cube maps

Programming Notes

This field indicates if EWA mode for LOD quality improvement needs to be disabled for cube maps. By default EWA would be on for cube maps hence this field must be 0. If there is any spec violation seen with EWA on cube maps then this field must be set to 1 to disable EWA for cubes.

19:18 Tiled Resource Mode

For Sampling Engine, Render Target, and Typed/Untyped Surfaces:

This field specifies the tiled resource mode.

For other surfaces:

This field is ignored.

Value	Name	Description	Exists If
0h	NONE	No tiled resource	
1h	4KB	4KB tiled resources	[SurfaceType] == 'SURFTYPE_1D'
2h	64KB	64KB tiled resources	[SurfaceType] == 'SURFTYPE_1D'
1h	TILEYF	4KB tiled resources	[SurfaceType] != 'SURFTYPE_1D'
2h	TILEYS	64KB tiled resources	[SurfaceType] != 'SURFTYPE_1D'
3h	Reserved		

Programming Notes

If **Tile Mode** is not set to TILEMODE_YMAJOR, this field must be set to TRMODE_NONE, unless the Surface Type is SURFTYPE_1D.

If this field is not set to TRMODE_NONE, the **Surface Format** must be one with 8, 16, 32, 64, or 128



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	bits per element, or one of the compressed texture modes (BC*, ETC*, EAC*, ASTC*). Additionally, YCRCB* formats are supported and treated as 16 bits per element, and the PLANAR_420_8 format is support and treated as 8 bits per element on the Y plane and 16 bits per element on the UV plane (if Separate UV Plane Enable is disabled) or 8 bits per element on the U and V planes (if Separate UV Plane Enable is enabled). If this field is set to TRMODE_NONE, the surface cannot contain any null pages unless Surface Type is BUFFER or STRBUF. A BUFFER or STRBUF surface with null pages must have Surface Base Address and Surface Pitch set to an integer multiple of the element size, and Surface Format must be one with 8, 16, 32, 64, or 128 bits per element. If Surface Format is PLANAR, the surface cannot contain any null pages.										
17:16	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>		Format:	MBZ							
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15	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>		Format:	MBZ							
Format:	MBZ										
14	Coherency Type Specifies the type of coherency maintained for this surface. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>GPU coherent</td><td>Surface memory is kept coherent with GPU threads using GPU read/write ordering rules. Surface memory is backed by system memory but is not kept coherent with CPU (LLC).</td></tr><tr><td>1h</td><td>IA coherent</td><td>Surface memory is kept coherent with CPU (LLC).</td></tr></table> Programming Notes This field may optionally be 1 (IA coherent) for messages sent to SFID_DP_DC0 or SFID_DP_DC1 or SFID_DP_DC2. This field is typically set to 0 (GPU coherent) if the context is operating in a non-SVM legacy mode (for example, Ring Buffer or a Execlist using 32-bit Virtual Address Legacy Context PPGTT32). If the surface is not IA coherent, then it is possible that data written to Null Tile address will be cached, and then a later read to that same address might return a non-zero value. If a value is cached for a Null Tile address, the data will be eventually be discarded when the cache line is evicted. If the surface is IA coherent, then the cache line never contains a non-zero value, and Null Tile reads always return zero.		Value	Name	Description	0h	GPU coherent	Surface memory is kept coherent with GPU threads using GPU read/write ordering rules. Surface memory is backed by system memory but is not kept coherent with CPU (LLC).	1h	IA coherent	Surface memory is kept coherent with CPU (LLC).
Value	Name	Description									
0h	GPU coherent	Surface memory is kept coherent with GPU threads using GPU read/write ordering rules. Surface memory is backed by system memory but is not kept coherent with CPU (LLC).									
1h	IA coherent	Surface memory is kept coherent with CPU (LLC).									
13:12	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>		Format:	MBZ							
Format:	MBZ										
11:8	Mip Tail Start LOD <table><tr><td>Format:</td><td>U4 in LOD Units</td></tr></table> For Sampling Engine, Render Target, and Typed Surfaces: This field indicates which LOD is the first one in the MIP tail if Tiled Resource Mode is not TRMODE_NONE. The MIP tail has a different layout than the rest of the surface. Refer to the <i>Memory Data Formats</i> section for more details.		Format:	U4 in LOD Units							
Format:	U4 in LOD Units										



RENDER_SURFACE_STATE

For other surfaces:

This field is ignored.

Programming Notes

This field must be zero if the **Surface Format** is MONO8

This field is ignored if **Tiled Resource Mode** is TRMODE_NONE.

If **Tiled Resource Mode** is not TRMODE_NONE, this field must be set to ensure that mips within the mip tail do not overlap given the storage algorithms given in the Memory Data Formats section.

If **Tiled Resource Mode** is not TRMODE_NONE, to disable the Mip Tail this field must be set to a mip that larger than those present in the surface (i.e. 15). This is recommended for non-mip-mapped surfaces.

The following table indicates the *maximum* size of the mip that is set to be the Mip Tail Start LOD for various cases:

Surface Type	Tiling Mode	#MS	Bits Per Element				
			8	16	32	64	128
1D	64KB	1	16384	8192	4096	2048	1024
	4KB	1	1024	512	256	128	64
2D/ CUBE	TlleYS	1	128x256	128x128	64x128	64x64	32x64
		2	128x128	128x64	64x64	64x32	32x32
		4	64x128	64x64	32x64	32x32	16x32
		8	64x64	64x32	32x32	32x16	16x16
		16	32x64	32x32	16x32	16x16	8x16
	TlleYF	any	32x64	32x32	16x32	16x16	8x16
3D	TlleYS	1	32x32x32	16x32x32	16x32x16	16x16x16	8x16x16
	TlleYF	1	16x8x16	8x8x16	8x8x8	8x4x8	4x4x8

7:4

Surface Min LOD

Format: U4 In LOD Units

For Sampling Engine and Typed Surfaces:

This field indicates the most detailed LOD that can be accessed as part of this surface. This field is added to the delivered LOD (*sample_l*, *ld*, or *resinfo* message types) before it is used to address the surface.

For Other Surfaces:

This field is ignored.

Programming Notes

This field must be zero if the **Surface Format** is MONO8

RENDER_SURFACE_STATE

RENDER_SURFACE_STATE				
	3:0	MIP Count / LOD		
		Format:	Sampling Engine and Typed Surfaces: U4 in (LOD units - 1) Render Target Surfaces: U4 in LOD units	
	Range	Sampling Engine and Typed Surfaces: [0,14] representing [1,15] MIP levels Render Target Surfaces: [0,14] representing LOD Other Surfaces: [0]		
	For Sampling Engine and Typed Surfaces: This field indicates the number of MIP levels allowed to be accessed starting at Surface Min LOD , which must be less than or equal to the number of MIP levels actually stored in memory for this surface. For sample* messages, the mip map access is clamped to be between the mipmap specified by the integer bits of the Min LOD and the ceiling of the value specified here. For Id* messages, out-of-bounds behavior results for LODs outside of the range specified in this field.			
	For Render Target Surfaces: This field defines the MIP level that is currently being rendered into. This is the absolute MIP level on the surface and is not relative to the Surface Min LOD field, which is ignored for render target surfaces.			
	For Other Surfaces: This field is reserved : MBZ			
	Programming Notes			
	The LOD of a render target must be the same as the LOD of the other render target(s) and of the depth buffer (defined in 3DSTATE_DEPTH_BUFFER). For render targets with YUV surface formats, the LOD must be zero. For sampling engine surfaces with YCRCB* or PLANAR* surface format, MIP Count must be zero.			
	6	31	Reserved	
			Exists If:	([Surface Format] != 'PLANAR')
Format:			MBZ	
31		Separate UV Plane Enable		
		Exists If:	([Surface Format] == 'PLANAR')	
		Format:	Enable	
		If enabled, this field indicates that the U and V are present as separate planes. If disabled, the UV data is interleaved on a single plane.		
		Programming Notes		
		See the section "Planar Memory Organization" for a description of how the size and location of the chroma planes (U and V) are calculated.		
		Workaround		
	The U and V planes, when separate (e.g. YV12) are treated as full-pitch (same width as Y plane). Zero padding in memory image will be required on each row of the U and V planes to sample			



RENDER_SURFACE_STATE

		correctly.
30	Reserved	
	Exists If:	([Surface Format] == 'PLANAR')
	Format:	MBZ
30:16	Auxiliary Surface QPitch	
	Exists If:	([Surface Format] != 'PLANAR')
	Format:	QPitch[16:2]
	This field specifies the distance in rows between array slices on the auxiliary surface.	
	Value	Name Description
	[4h,1FFCh]	in multiples of 4 (low 2 bits missing)
	Programming Notes	
	This field must be set to an integer multiple of the Surface Vertical Alignment	
	Software must ensure that this field is set to a value sufficiently large such that the array slices in the auxiliary surface do not overlap. Refer to the Memory Data Formats section for information on how surfaces are stored in memory.	
	For non-multisampled render target's CCS auxiliary surface, QPitch must be computed with Horizontal Alignment = 128 and Surface Vertical Alignment = 256. These alignments are only for CCS buffer and not for associated render target.	
29:16	X Offset for U or UV Plane	
	Exists If:	([Surface Format] == 'PLANAR')
	Format:	U14
	This field specifies the horizontal offset in pixels from the Surface Base Address to the start (origin) of the U plane or interleaved UV plane, depending on the setting of Separate UV Plane Enable .	
	Programming Notes	
	This field must be a multiple of 4 (bits 1:0 MBZ).	
	If Tiled Resource Mode is enabled, this field must be a multiple of the tile width in pixels.	
	Auxiliary Surface Mode is forced to AUX_NONE.	
15	Reserved	
	Format:	MBZ
14	Reserved	
	Exists If:	([Surface Format] == 'PLANAR')
	Format:	MBZ
14:12	Reserved	
	Exists If:	([Surface Format] != 'PLANAR')
	Format:	MBZ



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11:3

Auxiliary Surface Pitch		
Exists If:	([Surface Format] != 'PLANAR')	
Format:	U9-1 Pitch in #Tiles	
This field specifies the Auxiliary surface pitch in (#Tiles - 1).		
Value	Name	Description
[0, 511]		-> [1 tile, 512 tiles]

13:0

Y Offset for U or UV Plane	
Exists If:	([Surface Format] == 'PLANAR')
Format:	U14
This field specifies the vertical offset in rows from the Surface Base Address to the start (origin) of the U plane or interleaved UV plane, depending on the setting of Separate UV Plane Enable .	
Programming Notes	
For surfaces where Surface Format = PLANAR* and Separate UV Plane is Enabled, the Y Offset must be programmed in multiples of half-rows . For example, for a surface where Y is physically followed by U and then V in memory, the Y Offset to U plane would be (2*Y-Height). For all other PLANAR YUV formats this is programmed in multiples of full rows.	
This field must be a multiple of 4 (bits 1:0 MBZ) for all YUV PLANAR surfaces.	
If Tiled Resource Mode is enabled, this field must be a multiple of the tile height in rows.	
Auxiliary Surface Mode is forced to AUX_NONE.	
Workaround	
Workaround : For formats PLANAR_420_* when this field is not a multiple of 4 the Out-of-Bounds Supression check must be disabled to avoid false out of bound detection.	

2:0

Auxiliary Surface Mode		
Exists If:	([Surface Format] != 'PLANAR')	
Format:	U3	
Specifies what type of surface the Auxiliary surface is. The Auxiliary surface has its own base address and pitch, but otherwise shares or overrides other fields set for the primary surface, detailed in the programming notes below.		
Value	Name	Description
0h	AUX_NONE	No Auxiliary surface is used
1h	AUX_CCS_D	The Auxiliary surface is a CCS (Color Control Surface) with compression disabled or an MCS with compression enabled, depending on Number of Multisamples . MCS (Multisample Control Surface) is a special type of CCS.
2h	AUX_APPEND	The Auxiliary surface is an append buffer
3h	AUX_HIZ	The Auxiliary surface is a hierarchical depth buffer
4h	Reserved	



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5h	AUX_CCS_E	The Auxiliary surface is a CCS with compression enabled or an MCS with compression enabled, depending on Number of Multisamples .
	6h-7h	Reserved
Programming Notes		
The CCS and hierarchical depth Auxiliary surface shares Height, Width, Depth, Surface Type, Surface Array, Surface Min LOD, MIP Count / LOD, Surface Object Control State, Resource Min LOD, and Minimum Array Element with the primary surface. The hierarchical depth Auxiliary surface uses Surface Horizontal Alignment of 16, Surface Vertical Alignment of 8, regardless of the primary surface's values for these fields. X & Y Offset are set to zero for the purpose of accessing the Auxiliary surface. If this field is set to AUX_HIZ, Surface Format must be one of the following: R32_FLOAT, R24_UNORM_X8_TYPELESS, or R16_UNORM, and the format must match the format used when the surface was used as a depth buffer (with R channel corresponding to D channel).		
CCS and hierarchical depth Auxiliary surfaces are TileY with Tiled Resource Mode of TRMODE_NONE regardless of the tile mode of the primary surface, and Mip Tail Start LOD is ignored for these surfaces.		
The CCS Auxiliary surface for non-multisampled render targets has Horizontal Alignment = 128 and Vertical alignment = 64.		
The CCS Auxiliary surface for Number of Multisamples > 1 uses Surface Horizontal Alignment of 16 and Surface Vertical Alignment of 4 regardless of the primary surface's values for these fields.		
If this field is set to AUX_HIZ, Number of Multisamples must be MULTISAMPLECOUNT_1, and Surface Type cannot be SURFTYPE_3D.		
If Number of Multisamples is MULTISAMPLECOUNT_1, AUX_CCS_E setting is only allowed if Surface Format is supported for Render Target Compression. This setting enables render target compression.		
If Number of Multisamples is MULTISAMPLECOUNT_1, AUX_CCS_D setting is only allowed if Surface Format supported for Fast Clear. In addition, if the surface is bound to the sampling engine, Surface Format must be supported for Render Target Compression for surfaces bound to the sampling engine. For render target surfaces, this setting disables render target compression. For sampling engine surfaces, this mode behaves the same as AUX_CCS_E.		
If Number of Multisamples is <i>not</i> MULTISAMPLECOUNT_1, both AUX_CCS_E and AUX_CCS_D settings indicate that the auxiliary surface is a multisample control surface (MCS), and multisample compression is enabled.		
If Number of Multisamples is MULTISAMPLECOUNT_1, and if Tiled Resource Mode is NOT TRMODE_NONE, then, if CCS tile is NULL, Render Target Tiles represented by that CCS tile are assumed to be NULL by HW.		

**RENDER_SURFACE_STATE**

7	31	Memory Compression Mode Distinguishes Vertical from Horizontal compression.										
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0</td><td>Horizontal [Default]</td><td></td></tr><tr><td>1</td><td>Vertical</td><td></td></tr></table>	Value	Name	Description	0	Horizontal [Default]		1	Vertical		
	Value	Name	Description									
	0	Horizontal [Default]										
	1	Vertical										
	30	Memory Compression Enable										
		Format:	Enable									
		This surface may contain compressed or compressible pixels. Memory compression will be attempted for writes to this surface. Reads from this surface will check for compressed data.										
		Programming Notes										
		The compression control must have 0 value for non-tileY modes. The Memory Compression Enable can be non-zero only for the surface state that has media messages. That is for 3d case the compression control bits will be 0 in normal surface state but can be non-zero in normal surface state for media messages. E.g. <i>sample_unorm</i> .										
	The only sampler messages supported with memory compression enabled are <i>sample_8x8</i> , <i>sample_unorm</i> , and SIMD16 <i>sample</i> .											
	Please refer to vol1a Memory Data Formats chapter section Media Memory Compression for more details, including format restrictions.											
29	Reserved											
	Format:	MBZ										
28	Reserved											
27:25	Shader Channel Select Red											
	Format:	Shader Channel Select Enumerated Type										
	Specifies which surface channel is read or written in the Red shader channel.											
	Programming Notes											
	The Shader channel selects also define which shader channels are written to which surface channel. If the Shader channel select is SCS_ZERO or SCS_ONE then it is not written to the surface. If the shader channel select is SCS_RED it is written to the surface red channel and so on. If more than one shader channel select is set to the same surface channel only the first shader channel in RGBA order will be written. Each shader channel select must be set to the same surface channel (R = SCS_RED, G = SCS_GREEN, B = SCS_BLUE, A = SCS_ALPHA) if the surface is accessed via the sampler's <i>sample_unorm*</i> or <i>sample_8x8</i> messages.											
	The Shader Channel Select fields do not affect the following sampling engine message types: <i>resinfo</i> , <i>sampleinfo</i> , <i>LOD</i> , and <i>ld_mcs</i> . These messages behave as if each Shader Channel Select is set to the same color surface channel.											
	For the sampling engine <i>gather4*</i> messages, the Gather4 Source Channel Select field in the message header defines which channel's Shader Channel Select is used to select the surface channel to be sampled. Other Shader Channel Select fields are ignored.											
	For the sampling engine <i>sample*_c</i> and <i>gather4*_c</i> messages, the compare operation always occurs on the red channel from the surface regardless of the setting of the Shader Channel Select fields.											



RENDER_SURFACE_STATE

	For Render Target, Red, Green and Blue Shader Channel Selects MUST be such that only valid components can be swapped i.e. only change the order of components in the pixel. Any other values for these Shader Channel Select fields are not valid for Render Targets. This also means that there MUST not be multiple shader channels mapped to the same RT channel. When multiple Channel selects have the same value and shader channel is disabled, disable channel writes 0s to memory. This behavior does not match with Data Port message via HDC. The output channel is undefined if the source is to a channel is not present for the current surface format. For example, If the surface format is R16_float and the shader channel select green specifies green as the source the output is undefined. It should instead select 0 which is the default for a missing color channel..				
24:22	Shader Channel Select Green Format: Shader Channel Select Enumerated Type See Shader Channel Select Red for details.				
21:19	Shader Channel Select Blue Format: Shader Channel Select Enumerated Type See Shader Channel Select Red for details.				
18:16	Shader Channel Select Alpha Format: Shader Channel Select Enumerated Type See Shader Channel Select Red for details. Programming Notes For Render Target, this field MUST be programmed to value = SCS_ALPHA.				
15:12	Reserved Format: MBZ				
11:0	Resource Min LOD Format: U4.8 in LOD units For Sampling Engine Surfaces: This field indicates the most detailed LOD that is present in the resource underlying the surface. Refer to the "LOD Computation Pseudocode" section for the use of this field. For Other Surfaces: This field is ignored. <table><tr><th>Value</th><th>Name</th></tr><tr><td>[0,14]</td><td></td></tr></table> Programming Notes This field must be zero if the Surface Format is MONO8 This field must be zero if the ChromaKey Enable is enabled in the associated sampler.	Value	Name	[0,14]	
Value	Name				
[0,14]					



RENDER_SURFACE_STATE

8..9

63:0

Surface Base Address

Format:	GraphicsAddress[63:0]SurfaceBase

Specifies the byte-aligned base address of the surface.

Programming Notes

- For SURFTYPE_BUFFER render targets, this field specifies the base address of first element of the surface. The surface is interpreted as a simple array of that single element type. The address must be naturally-aligned to the element size (e.g., a buffer containing R32G32B32A32_FLOAT elements must be 16-byte aligned).
- For SURFTYPE_BUFFER non-rendertarget surfaces, this field specifies the base address of the first element of the surface, computed in software by adding the surface base address to the byte offset of the element in the buffer. The base address must be aligned to element size.
- Linear depth buffer surface base addresses must be 64-byte aligned. Note that while render targets (color) can be SURFTYPE_BUFFER, depth buffers cannot.
- Mipmapped surfaces are stored in a "monolithic" (fixed) format, and only require a single address for the base MIP. All other MIPs are positioned relative to the base MIP.
- The Base Address for linear (non-tiled) render target surfaces and surfaces accessed with the typed surface read/write data port messages must be element-size aligned for Non-YUV surface formats, or a multiple of 2 element-sizes for YUV surface formats.
- Other linear (non-tiled) surfaces have no alignment requirements (byte alignment is sufficient).
- For tiled surfaces, the actual start of the surface can be offset from the Surface Base Address by the X Offset and Y Offset fields. Tiles are inherently page-aligned (4K or 64K).
- Certain message types used to access surfaces have more stringent alignment requirements. Please refer to the specific data-port message documentation for additional restrictions.

Tiled surface base addresses must be 4KB-aligned. Note that only the offsets from Surface Base Address are tiled, Surface Base Address itself is not transformed using the tiling algorithm.

Tiled surface base addresses must be tile aligned (64KB aligned for TileYS, 4KB aligned for all other tile modes). For 1D surfaces, the base address must be 64KB aligned if Tiled Resource Mode is TRMODE_64KB, and 4KB aligned if Tiled Resource Mode is TRMODE_4KB. Compressed (BC*, ASTC, etc.) surface data is usually copied by re-describing each MIP/slice as a separate surface, using a size-equivalent RGBA format. But a MIP/slice within a packed **MIP Tail** doesn't have the tile-aligned **Surface Base Address** required for the re-description. This case must be specially handled by re-describing the packed **MIP Tail** as a single-MIP surface with the width/pitch/height/depth of a single tile, and then use drawing geometry to "reach out" to the desired tail slot (x, y, z) offset.



RENDER_SURFACE_STATE															
10..11	63:62	Reserved <table><tr><td>Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>	Exists If:	([Surface Format] == 'PLANAR')	Format:	MBZ									
	Exists If:	([Surface Format] == 'PLANAR')													
	Format:	MBZ													
	61:48	X Offset for V Plane <table><tr><td>Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr><tr><td>Format:</td><td>U14</td></tr></table> This field specifies the horizontal offset in pixels from the Surface Base Address to the start (origin) of the V plane.	Exists If:	([Surface Format] == 'PLANAR')	Format:	U14									
	Exists If:	([Surface Format] == 'PLANAR')													
	Format:	U14													
	47:46	Reserved <table><tr><td>Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>	Exists If:	([Surface Format] == 'PLANAR')	Format:	MBZ									
	Exists If:	([Surface Format] == 'PLANAR')													
	Format:	MBZ													
	45:32	Y Offset for V Plane <table><tr><td>Exists If:</td><td>([Surface Format] == 'PLANAR')</td></tr><tr><td>Format:</td><td>U14</td></tr></table> This field specifies the vertical offset in rows from the Surface Base Address to the start (origin) of the V plane. <table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">For surfaces where Surface Format = PLANAR* and Separate UV Plane is Enabled, the Y Offset must be programmed in multiples of half-rows. For example, for a surface where Y is physically followed by U and then V in memory, the Y Offset to V plane would be (2*Y-Height+ U-Height). For all other PLANAR YUV formats this is programmed in multiples of full rows (e.g Y-Height + U-Height).</td></tr><tr><td colspan="2">This field must be a multiple of 4 (bits 1:0 MBZ).</td></tr><tr><td colspan="2">If Tiled Resource Mode is enabled, this field must be a multiple of the tile height in rows.</td></tr><tr><td colspan="2">This field is ignored if Separate UV Plane Enable is disabled.</td></tr></table>	Exists If:	([Surface Format] == 'PLANAR')	Format:	U14	Programming Notes		For surfaces where Surface Format = PLANAR* and Separate UV Plane is Enabled, the Y Offset must be programmed in multiples of half-rows . For example, for a surface where Y is physically followed by U and then V in memory, the Y Offset to V plane would be (2*Y-Height+ U-Height). For all other PLANAR YUV formats this is programmed in multiples of full rows (e.g Y-Height + U-Height).		This field must be a multiple of 4 (bits 1:0 MBZ).		If Tiled Resource Mode is enabled, this field must be a multiple of the tile height in rows.		This field is ignored if Separate UV Plane Enable is disabled.
Exists If:	([Surface Format] == 'PLANAR')														
Format:	U14														
Programming Notes															
For surfaces where Surface Format = PLANAR* and Separate UV Plane is Enabled, the Y Offset must be programmed in multiples of half-rows . For example, for a surface where Y is physically followed by U and then V in memory, the Y Offset to V plane would be (2*Y-Height+ U-Height). For all other PLANAR YUV formats this is programmed in multiples of full rows (e.g Y-Height + U-Height).															
This field must be a multiple of 4 (bits 1:0 MBZ).															
If Tiled Resource Mode is enabled, this field must be a multiple of the tile height in rows.															
This field is ignored if Separate UV Plane Enable is disabled.															
31:21	Auxiliary Table Index for Media Compressed Surface <table><tr><td>Exists If:</td><td>[Memory Compression Enable] == 1</td></tr></table> This field is valid only if Media Memory Compression is on for the surface(Memory Compression Enable == 1). In that case, the Auxiliary Surface Base address is never expected to be used and hence can be overloaded. This represents the 11 bit index into the table in memory which maps the surface to the auxiliary base address.	Exists If:	[Memory Compression Enable] == 1												
Exists If:	[Memory Compression Enable] == 1														
63:12	Auxiliary Surface Base Address <table><tr><td>Exists If:</td><td>([Surface Format] != 'PLANAR') AND [Memory Compression Enable] == 0</td></tr><tr><td>Format:</td><td>GraphicsAddress[63:12]</td></tr></table> Specifies the 4kbyte-aligned base address of the Auxiliary surface associated with the primary surface specified in other SURFACE_STATE fields.	Exists If:	([Surface Format] != 'PLANAR') AND [Memory Compression Enable] == 0	Format:	GraphicsAddress[63:12]										
Exists If:	([Surface Format] != 'PLANAR') AND [Memory Compression Enable] == 0														
Format:	GraphicsAddress[63:12]														
11	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ												
Format:	MBZ														



RENDER_SURFACE_STATE												
	10	Reserved <table><tr><td>Format:</td><td>MBZ</td></tr></table>	Format:	MBZ								
	Format:	MBZ										
	9:5	Quilt Height <table><tr><td>Format:</td><td>U5</td></tr><tr><td colspan="2">This field specifies the height of a quilted texture in units of quilt slices. Refer to the section on Quilted Textures for more details.</td></tr><tr><td>Value</td><td>Name</td><td>Description</td></tr><tr><td>[0,31]</td><td></td><td>representing height of quilt - 1 (y/v dimension)</td></tr></table> Programming Notes Programming Notes - Only power-of-2 Quilt Height and Quilt Width values are allowed: (1,2,4,8,16,32) mapping to (0,1,3,7,15,31) values in the fields. - A surface is defined as a quilted texture if either Quilt Height or Quilt Width is nonzero (actual field value, not the incremented value). - A quilted texture - is only supported by the sampling engine (other shared functions will ignore the Quilt Width and Quilt Height field, behaving as if they are set to zero). - must have a Surface Type of SURFTYPE_2D. - must have Number of Multisamples set to NUMSAMPLES_1. - must have Vertical Line Stride set to 0. - must have Auxiliary Surface Mode set to AUX_NONE. Depth indicates the array dimension of the quilted texture if Surface Array is enabled. The valid range of Depth is [0, 2048 / (QuiltWidth * QuiltHeight) - 1], i.e. the total number of underlying array slices including quilt slices cannot exceed 2048. - cannot be accessed with any Id* message type or using a sampler with the Non-Normalized Coordinate Enable field enabled.	Format:	U5	This field specifies the height of a quilted texture in units of quilt slices. Refer to the section on Quilted Textures for more details.		Value	Name	Description	[0,31]		representing height of quilt - 1 (y/v dimension)
	Format:	U5										
	This field specifies the height of a quilted texture in units of quilt slices. Refer to the section on Quilted Textures for more details.											
	Value	Name	Description									
	[0,31]		representing height of quilt - 1 (y/v dimension)									
	4:0	Quilt Width <table><tr><td>Format:</td><td>U5</td></tr><tr><td colspan="2">This field specifies the width of a quilted texture in units of quilt slices. Refer to the section on Quilted Textures for more details.</td></tr><tr><td>Value</td><td>Name</td><td>Description</td></tr><tr><td>[0,31]</td><td></td><td>representing width of quilt - 1 (x/u dimension)</td></tr></table>	Format:	U5	This field specifies the width of a quilted texture in units of quilt slices. Refer to the section on Quilted Textures for more details.		Value	Name	Description	[0,31]		representing width of quilt - 1 (x/u dimension)
	Format:	U5										
	This field specifies the width of a quilted texture in units of quilt slices. Refer to the section on Quilted Textures for more details.											
Value	Name	Description										
[0,31]		representing width of quilt - 1 (x/u dimension)										
12	31:0	Reserved <table><tr><td>Exists If:</td><td>([Auxiliary Surface Mode] != 'AUX_CCS_D') AND ([Auxiliary Surface Mode] != 'AUX_CCS_E') AND ([Auxiliary Surface Mode] != 'AUX_HIZ')</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>	Exists If:	([Auxiliary Surface Mode] != 'AUX_CCS_D') AND ([Auxiliary Surface Mode] != 'AUX_CCS_E') AND ([Auxiliary Surface Mode] != 'AUX_HIZ')	Format:	MBZ						
Exists If:	([Auxiliary Surface Mode] != 'AUX_CCS_D') AND ([Auxiliary Surface Mode] != 'AUX_CCS_E') AND ([Auxiliary Surface Mode] != 'AUX_HIZ')											
Format:	MBZ											



RENDER_SURFACE_STATE																
	31:0	Red Clear Color <table><tr><td>Exists If:</td><td>[Auxiliary Surface Mode] == 'AUX_CCS_D' OR [Auxiliary Surface Mode] == 'AUX_CCS_E'</td></tr><tr><td>Format:</td><td>S31 (2's complement) for all SINT surface formats</td></tr><tr><td>Format:</td><td>U32 for all UINT surface formats</td></tr><tr><td>Format:</td><td>IEEE_FP for all other surface formats</td></tr></table> For Sampling Engine Surfaces and Render Targets with Auxiliary Surface Mode set to AUX_CCS: Specifies the clear value for the red channel. For Other Surfaces: This field is ignored. <table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">If Number of Multisamples is not MULTISAMPLECOUNT_1, only 0/1 values allowed</td></tr><tr><td colspan="2">If Number of Multisamples is MULTISAMPLECOUNT_1 AND if this RT is fast cleared with non-0/1 clear value, this RT must be partially resolved (refer to Partial Resolve operation) before binding this surface to Sampler.</td></tr></table>	Exists If:	[Auxiliary Surface Mode] == 'AUX_CCS_D' OR [Auxiliary Surface Mode] == 'AUX_CCS_E'	Format:	S31 (2's complement) for all SINT surface formats	Format:	U32 for all UINT surface formats	Format:	IEEE_FP for all other surface formats	Programming Notes		If Number of Multisamples is not MULTISAMPLECOUNT_1, only 0/1 values allowed		If Number of Multisamples is MULTISAMPLECOUNT_1 AND if this RT is fast cleared with non-0/1 clear value, this RT must be partially resolved (refer to Partial Resolve operation) before binding this surface to Sampler.	
		Exists If:	[Auxiliary Surface Mode] == 'AUX_CCS_D' OR [Auxiliary Surface Mode] == 'AUX_CCS_E'													
		Format:	S31 (2's complement) for all SINT surface formats													
		Format:	U32 for all UINT surface formats													
		Format:	IEEE_FP for all other surface formats													
		Programming Notes														
		If Number of Multisamples is not MULTISAMPLECOUNT_1, only 0/1 values allowed														
		If Number of Multisamples is MULTISAMPLECOUNT_1 AND if this RT is fast cleared with non-0/1 clear value, this RT must be partially resolved (refer to Partial Resolve operation) before binding this surface to Sampler.														
		31:0	Hierarchical Depth Clear Value <table><tr><td>Exists If:</td><td>[Auxiliary Surface Mode] == 'AUX_HIZ'</td></tr><tr><td>Format:</td><td>IEEE_Float</td></tr></table> If Auxiliary Surface Mode is AUX_HIZ, this field specifies the depth clear value associated with this surface. If disabled, this field is ignored.	Exists If:	[Auxiliary Surface Mode] == 'AUX_HIZ'	Format:	IEEE_Float									
			Exists If:	[Auxiliary Surface Mode] == 'AUX_HIZ'												
Format:	IEEE_Float															
13	31:0	Green Clear Color <table><tr><td>Exists If:</td><td>[Auxiliary Surface Mode] == 'AUX_CCS_D' OR [Auxiliary Surface Mode] == 'AUX_CCS_E'</td></tr><tr><td>Format:</td><td>S31 (2's complement) for all SINT surface formats</td></tr><tr><td>Format:</td><td>U32 for all UINT surface formats</td></tr><tr><td>Format:</td><td>IEEE_FP for all other surface formats</td></tr></table> For Sampling Engine Surfaces and Render Targets with Auxiliary Surface Mode set to AUX_CCS: Specifies the clear value for the green channel. For Other Surfaces: This field is ignored. <table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">If programmed to non 0/1 values, SW must ensure a render target partial resolve pass before binding a cleared RT to texture.</td></tr></table>	Exists If:	[Auxiliary Surface Mode] == 'AUX_CCS_D' OR [Auxiliary Surface Mode] == 'AUX_CCS_E'	Format:	S31 (2's complement) for all SINT surface formats	Format:	U32 for all UINT surface formats	Format:	IEEE_FP for all other surface formats	Programming Notes		If programmed to non 0/1 values, SW must ensure a render target partial resolve pass before binding a cleared RT to texture.			
Exists If:	[Auxiliary Surface Mode] == 'AUX_CCS_D' OR [Auxiliary Surface Mode] == 'AUX_CCS_E'															
Format:	S31 (2's complement) for all SINT surface formats															
Format:	U32 for all UINT surface formats															
Format:	IEEE_FP for all other surface formats															
Programming Notes																
If programmed to non 0/1 values, SW must ensure a render target partial resolve pass before binding a cleared RT to texture.																
31:0	Reserved <table><tr><td>Exists If:</td><td>[Auxiliary Surface Mode] == 'AUX_HIZ'</td></tr><tr><td>Format:</td><td>MBZ</td></tr></table>	Exists If:	[Auxiliary Surface Mode] == 'AUX_HIZ'	Format:	MBZ											
	Exists If:	[Auxiliary Surface Mode] == 'AUX_HIZ'														
Format:	MBZ															



RENDER_SURFACE_STATE			
14	31:0	Blue Clear Color	
		Exists If:	[Auxiliary Surface Mode] == 'AUX_CCS_D' OR [Auxiliary Surface Mode] == 'AUX_CCS_E'
		Format:	S31 (2's complement) for all SINT surface formats
		Format:	U32 for all UINT surface formats
		Format:	IEEE_FP for all other surface formats
	For Sampling Engine Surfaces and Render Targets with Auxiliary Surface Mode set to AUX_CCS: Specifies the clear value for the blue channel.		
	For Other Surfaces: This field is ignored.		
	Programming Notes		
	If programmed to non 0/1 values, SW must ensure a render target partial resolve pass before binding a cleared RT to texture.		
	31:0	Reserved	
Exists If:		[Auxiliary Surface Mode] == 'AUX_HIZ'	
Format:		MBZ	
15	31:0	Alpha Clear Color	
		Exists If:	[Auxiliary Surface Mode] == 'AUX_CCS_D' OR [Auxiliary Surface Mode] == 'AUX_CCS_E'
		Format:	S31 (2's complement) for all SINT surface formats
		Format:	U32 for all UINT surface formats
		Format:	IEEE_FP for all other surface formats
	For Sampling Engine Surfaces and Render Targets with Auxiliary Surface Mode set to AUX_CCS: Specifies the clear value for the alpha channel.		
	For Other Surfaces: This field is ignored.		
	Programming Notes		
	If programmed to non 0/1 values, SW must ensure a render target partial resolve pass before binding a cleared RT to texture.		
	31:0	Reserved	
Exists If:		[Auxiliary Surface Mode] == 'AUX_HIZ'	
Format:		MBZ	



SAMPLER_STATE

SAMPLER_STATE																									
Source:	BSpec																								
Exists If:	//(MessageType != 'Deinterlace') && (MessageType != 'Sample_8x8')																								
Size (in bits):	128																								
Default Value:	0x00000000, 0x00000000, 0x00000000, 0x00000000																								
This is the normal sampler state used by all messages that use SAMPLER_STATE except sample_8x8 and deinterlace. The sampler state is stored as an array of up to 16 elements, each of which contains the dwords described here. The start of each element is spaced 4 dwords apart. The first element of the sampler state array is aligned to a 32-byte boundary.																									
DWord	Bit	Description																							
0	31	Sampler Disable <table><tr><td>Format:</td><td>Disable</td></tr></table> This field allows the sampler to be disabled. If disabled, all output channels will return 0.	Format:	Disable																					
	Format:	Disable																							
	30	Reserved																							
	29	Texture Border Color Mode For some surface formats, the 32 bit border color is decoded differently based on the border color mode. In addition, the default value of channels not included in the surface may be affected by this field. Refer to the "Sampler Output Channel Mapping" table for the values of these channels, and for surface formats that may only support one of these modes. Also refer to the definition of SAMPLER_BORDER_COLOR_STATE for more details on the behavior of the two modes defined by this field. <table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>DX10/OGL</td><td>DX10/OGL mode for interpreting the border color</td></tr><tr><td>1h</td><td>DX9</td><td>DX9 and earlier mode for interpreting the border color</td></tr></table> <table><tr><th colspan="2">Programming Notes</th></tr><tr><td colspan="2">This feild must not be set to DX9 if there are null tiles in use</td></tr><tr><td colspan="2">This field is required to be the same for every message over a period of time. A flush of the sampler cache must occur before a message with the opposite state of this field is delivered.</td></tr><tr><td colspan="2">This field must be set to DX9 mode when used with surfaces that have Surface Format P4A4_UNORM or A4P4_UNORM.</td></tr><tr><td colspan="2">This field must be set to DX10/OGL mode when used with surfaces that have Surface Format YCRCB_SWAPUV or YCRCB_SWAPY.</td></tr><tr><td colspan="2">This field must be set to DX10/OGL mode if Surface Format for the associated surface is UINT OR SINT.</td></tr><tr><td colspan="2">This field must be set to DX10/OGL mode if REDUCTION_MINIMUM or REDUCTION_MAXIMUM or message type is sample_min or sample_max.</td></tr></table>	Value	Name	Description	0h	DX10/OGL	DX10/OGL mode for interpreting the border color	1h	DX9	DX9 and earlier mode for interpreting the border color	Programming Notes		This feild must not be set to DX9 if there are null tiles in use		This field is required to be the same for every message over a period of time. A flush of the sampler cache must occur before a message with the opposite state of this field is delivered.		This field must be set to DX9 mode when used with surfaces that have Surface Format P4A4_UNORM or A4P4_UNORM.		This field must be set to DX10/OGL mode when used with surfaces that have Surface Format YCRCB_SWAPUV or YCRCB_SWAPY.		This field must be set to DX10/OGL mode if Surface Format for the associated surface is UINT OR SINT.		This field must be set to DX10/OGL mode if REDUCTION_MINIMUM or REDUCTION_MAXIMUM or message type is sample_min or sample_max.	
	Value	Name	Description																						
0h	DX10/OGL	DX10/OGL mode for interpreting the border color																							
1h	DX9	DX9 and earlier mode for interpreting the border color																							
Programming Notes																									
This feild must not be set to DX9 if there are null tiles in use																									
This field is required to be the same for every message over a period of time. A flush of the sampler cache must occur before a message with the opposite state of this field is delivered.																									
This field must be set to DX9 mode when used with surfaces that have Surface Format P4A4_UNORM or A4P4_UNORM.																									
This field must be set to DX10/OGL mode when used with surfaces that have Surface Format YCRCB_SWAPUV or YCRCB_SWAPY.																									
This field must be set to DX10/OGL mode if Surface Format for the associated surface is UINT OR SINT.																									
This field must be set to DX10/OGL mode if REDUCTION_MINIMUM or REDUCTION_MAXIMUM or message type is sample_min or sample_max.																									

**SAMPLER_STATE**

28:27	LOD PreClamp Mode												
	This field determines whether the computed LOD is clamped to [max,min] mip level before the mag-vs-min determination is performed. PRECLAMP_OGL: LOD pre-clamped to Min LOD and Max LOD OpenGL API currently clamps LOD to the Min LOD and Max LOD (from Sampler State) prior to performing min/mag determination, and therefore it is expected that an OpenGL driver would need to set this field to PRECLAMP_OGL. <table><thead><tr><th>Value</th><th>Name</th><th>Description</th></tr></thead><tbody><tr><td>0h</td><td>NONE</td><td>LOD PreClamp disabled</td></tr><tr><td>1h</td><td>Reserved</td><td></td></tr><tr><td>2h</td><td>OGL</td><td>LOD PreClamp enabled (OGL mode)</td></tr></tbody></table>		Value	Name	Description	0h	NONE	LOD PreClamp disabled	1h	Reserved		2h	OGL
Value	Name	Description											
0h	NONE	LOD PreClamp disabled											
1h	Reserved												
2h	OGL	LOD PreClamp enabled (OGL mode)											
26:22	Coarse LOD Quality Mode												
	Format:	U5											
This field configures the coarse LOD image quality mode for the sample_d, sample_l, and sample_b messages in the sampling engine. In general, performance will increase and power consumption will decrease with each step of reduced quality (performance gain for sample_l and sample_b will be minimal). <table><thead><tr><th>Value</th><th>Name</th><th>Description</th></tr></thead><tbody><tr><td>0h</td><td>Disabled</td><td>Full quality is enabled, matching prior products</td></tr><tr><td>01h-1Fh</td><td></td><td>Quality degrades with each larger value, performance improves with each larger value</td></tr></tbody></table> Programming Notes Although allowed, it is not recommended to program this field to a value greater than 17h to avoid masking the exponent which may generate incorrect LOD values.			Value	Name	Description	0h	Disabled	Full quality is enabled, matching prior products	01h-1Fh		Quality degrades with each larger value, performance improves with each larger value		
Value	Name	Description											
0h	Disabled	Full quality is enabled, matching prior products											
01h-1Fh		Quality degrades with each larger value, performance improves with each larger value											



SAMPLER_STATE

21:20	Mip Mode Filter		
	Format:		U2 Enumerated Type
	This field determines if and how mip map levels are chosen and/or combined when texture filtering.		
	Value	Name	Description
	0h	NONE	Disable mip mapping - force use of the mipmap level corresponding to Min LOD.
	1h	NEAREST	Nearest, Select the nearest mip map
	2h	Reserved	
	3h	LINEAR	Linearly interpolate between nearest mip maps (combined with linear min/mag filters this is analogous to "Trilinear" filtering).
	Programming Notes		
	MIPFILTER_LINEAR is not supported for surface formats that do not support "Sampling Engine Filtering" as indicated in the Surface Formats table unless using the sample_c message type or minimum/maximum operation.		
	Mip Mode Filter must be set to MIPFILTER_NONE or MIPFILTER_NEAREST if Surface Format for the associated surface is UINT or SINT. However, all settings of this field are allowed with UINT/SINT if a minimum or maximum operation is being performed.		
	Mip Mode Filter must be set to MIPFILTER_NONE for Planar YUV surfaces.		

19:17	Mag Mode Filter		
	Format:		U3 Enumerated Type
	This field determines how texels are sampled/filtered when a texture is being "magnified" (enlarged). For volume maps, this filter mode selection also applies to the 3rd (inter-layer) dimension.		
	Value	Name	Description
	0h	NEAREST	Sample the nearest texel
	1h	LINEAR	Bilinearly filter the 4 nearest texels
	2h	ANISOTROPIC	Perform an "anisotropic" filter on the chosen mip level
	4h-5h	Reserved	
	6h	MONO	Perform a monochrome convolution filter
	7h	Reserved	
	Programming Notes		
	Only MAPFILTER_NEAREST and MAPFILTER_LINEAR are supported for surfaces of type SURFTYPE_3D.		
Only MAPFILTER_NEAREST is supported for surface formats that do not support "Sampling Engine Filtering" as indicated in the Surface Formats table unless using the sample_c message type or minimum/maximum operation.			



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	MAPFILTER_MONO: Only CLAMP_BORDER texture addressing mode is supported. . Both Mag Mode Filter and Min Mode Filter must be programmed to MAPFILTER_MONO. Mip Mode Filter must be MIPFILTER_NONE. Only valid on surfaces with Surface Format MONO8 and with Surface Type SURFTYPE_2D.		
	MAPFILTER_ANISOTROPIC may cause artifacts at cube edges if enabled for cube maps with the TEXCOORDMODE_CUBE addressing mode.		
	MAPFILTER_ANISOTROPIC will be overridden to MAPFILTER_LINEAR when using a sample_l or sample_l_c message type or when Force LOD to Zero is set in the message header.		
	Both Mag Mode Filter and Min Mode Filter must be set to MAPFILTER_NEAREST if Surface Format for the associated surface is UINT or SINT. However, all settings of this field other than MAPFILTER_MONO are allowed with UINT/SINT if a minimum or maximum operation is being performed.		
16:14	Min Mode Filter		
	Format:	U3 Enumerated Type	
	This field determines how texels are sampled/filtered when a texture is being "minified" (shrunk). For volume maps, this filter mode selection also applies to the 3rd (inter-layer) dimension.See Mag Mode Filter		
	Value	Name	Description
	0h	NEAREST	Sample the nearest texel
	1h	LINEAR	Bilinearly filter the 4 nearest texels
	2h	ANISOTROPIC	Perform an "anisotropic" filter on the chosen mip level
	4h-5h	Reserved	
6h	MONO	Perform a monochrome convolution filter	
7h	Reserved		
13:1	Texture LOD Bias		
	Format:	S4.8 2's complement	
	Range: [-16.0, 16.0)		
	This field specifies the signed bias value added to the calculated texture map LOD prior to min-vs-mag determination and mip-level clamping. Assuming mipmapping is enabled, a positive LOD bias will result in a somewhat blurrier image (using less-detailed mip levels) and possibly higher performance, while a negative bias will result in a somewhat crisper image (using more-detailed mip levels) and may lower performance.		
	Programming Notes		
	There is no requirement or need to offset the LOD Bias in order to produce a correct LOD for texture filtering (as was required for correct bilinear and anisotropic filtering in some legacy devices).		



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0	LOD algorithm	Format: U1 Enumerated Type	
		Controls which algorithm is used for LOD calculation. Generally, the EWA approximation algorithm results in higher image quality than the legacy algorithm.	
1	31:20	Value	Name
		0h	LEGACY
		1h	EWA Approximation
		Description	
		Use the legacy algorithm for non-anisotropic filtering	
1	19:8	Use the new EWA approximation algorithm for anisotropic filtering	
		Programming Notes	
		The EWA Algorithm should only be enabled for Anisotropic Filtering modes. It must not be enabled for non-anisotropic filtering as the increased accuracy of the LOD calculation will is not required and will increase the power and reduce overall efficiency.	
		Min LOD	
		Format: U4.8 in LOD units	
1	19:8	Range: [0.0, 14.0], where the upper limit is also bounded by the Max LOD.	
		This field specifies the minimum value used to clamp the computed LOD after LOD bias is applied. Note that the minification-vs.-magnification status is determined after LOD bias and before this maximum (resolution) mip clamping is applied. The integer bits of this field are used to control the "maximum" (highest resolution) mipmap level that may be accessed (where LOD 0 is the highest resolution map). The fractional bits of this value effectively clamp the inter-level trilinear blend factor when trilinear filtering is in use.	
		Programming Notes	
		If Min LOD is greater than Max LOD, Min LOD takes precedence, i.e. the resulting LOD will always be Min LOD.	
		This field must be zero if the Min or Mag Mode Filter is set to MAPFILTER_MONO	
1	19:8	Max LOD	
		Format: U4.8 in LOD units	
		Range: [0.0, 14.0]	
		This field specifies the maximum value used to clamp the computed LOD after LOD bias is applied. Note that the minification-vs.-magnification status is determined after LOD bias and before this minimum (resolution) mip clamping is applied. The integer bits of this field are used to control the "minimum" (lowest resolution) mipmap level that may be accessed. The fractional bits of this value effectively clamp the inter-level trilinear blend factor when trilinear filtering is in use. Force the mip map access to be between the mipmap specified by the integer bits of the Min LOD and the ceiling of the value specified here.	

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	7	ChromaKey Enable		
		Format: Enable This field enables the chroma key function.		
		Programming Notes		
		Supported only on a specific subset of surface formats. See section titled: "Surface Formats" in this volume for supported formats. This field must be disabled if min or mag filter is MAPFILTER_MONO or MAPFILTER_ANISOTROPIC. This field must be disabled if used with a surface of type SURFTYPE_3D.		
6:5		ChromaKey Index		
		Format: U2		
		Range: [0, 3]		
		This field specifies the index of the ChromaKey Table entry associated with this Sampler. This field is a "don't care" unless ChromaKey Enable is ENABLED.		
4		ChromaKey Mode		
		Format: U1 Enumerated Type		
		This field specifies the behavior of the device in the event of a ChromaKey match. This field is ignored if ChromaKey is disabled.		
		KEYFILTER_REPLACE_BLACK: In this mode, each texel that matches the chroma key is replaced with (0,0,0,0) (black with alpha=0) prior to filtering. For YCrCb surface formats, the black value is A=0, R(Cr)=0x80, G(Y)=0x10, B(Cb)=0x80. This will tend to darken/fade edges of keyed regions. Note that the pixel pipeline must be programmed to use the resulting filtered texel value to gain the intended effect, e.g., handle the case of a totally keyed-out region (filtered texel alpha=0) through use of alpha test, etc.		



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			region (filtered texel alpha==0) through use of alpha test, etc.
3:1	Shadow Function		
	Format:		U3 Enumerated Type
	This field is used for shadow mapping support via the sample_c message type, and specifies the specific comparison operation to be used. The comparison is between the texture sample red channel (except for alpha-only formats which use the alpha channel), and the "ref" value provided in the input message.		
	Value	Name	
	0h	PREFILTEROP ALWAYS	
	1h	PREFILTEROP NEVER	
	2h	PREFILTEROP LESS	
	3h	PREFILTEROP EQUAL	
	4h	PREFILTEROP LEQUAL	
	5h	PREFILTEROP GREATER	
6h	PREFILTEROP NOTEQUAL		
7h	PREFILTEROP GEQUAL		
0	Cube Surface Control Mode		
	Format:		U1 Enumerated Type
	When sampling from a SURFTYPE_CUBE surface, this field controls whether the TC* Address Control Mode fields are interpreted as programmed or overridden to TEXCOORDMODE_CUBE.		
	Value	Name	
0h	PROGRAMMED		
1h	OVERRIDE		
2	31:30	Reserved	
	29:28	Reserved	
	27:26	Reserved	
	31:24	Reserved	
	25:24	Reserved	
	23:6	Indirect State Pointer	
		Description This pointer is relative to the Dynamic State Base Address.	
	5	Reserved	
		Format:	MBZ
	4	Reserved	
3	Reserved		



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	2	Reserved															
	1	Reserved															
	0	LOD Clamp Magnification Mode															
		Format: U1 Enumerated Type															
		This field allows the flexibility to control how LOD clamping is handled when in magnification mode.															
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>MIPNONE</td><td>When in magnification mode, Sampler will clamp LOD as if the Mip Mode Filter is MIPFILTER_NONE. This is how OpenGL defines magnification, and therefore it is expected that those drivers would not set this bit.</td></tr><tr><td>1h</td><td>MIPFILTER</td><td>When in magnification mode, Sampler will clamp LOD based on the value of Mip Mode Filter.</td></tr></table>	Value	Name	Description	0h	MIPNONE	When in magnification mode, Sampler will clamp LOD as if the Mip Mode Filter is MIPFILTER_NONE. This is how OpenGL defines magnification, and therefore it is expected that those drivers would not set this bit.	1h	MIPFILTER	When in magnification mode, Sampler will clamp LOD based on the value of Mip Mode Filter .						
Value	Name	Description															
0h	MIPNONE	When in magnification mode, Sampler will clamp LOD as if the Mip Mode Filter is MIPFILTER_NONE. This is how OpenGL defines magnification, and therefore it is expected that those drivers would not set this bit.															
1h	MIPFILTER	When in magnification mode, Sampler will clamp LOD based on the value of Mip Mode Filter .															
3	31:24	Reserved															
	25:24	Reserved															
		Format: MBZ															
	23:22	Reduction Type															
		Format: U2 Enumerated Type															
		This field defines the type of reduction that will be performed on the texels in the footprint defined by the Min/Mag/Mip Filter Mode fields. This field is ignored if Reduction Type Enable is disabled.															
		<table><tr><th>Value</th><th>Name</th><th>Description</th></tr><tr><td>0h</td><td>STD_FILTER</td><td>standard filter</td></tr><tr><td>1h</td><td>COMPARISON</td><td>comparison followed by standard filter</td></tr><tr><td>2h</td><td>MINIMUM</td><td>minimum of footprint</td></tr><tr><td>3h</td><td>MAXIMUM</td><td>maximum of footprint</td></tr></table>	Value	Name	Description	0h	STD_FILTER	standard filter	1h	COMPARISON	comparison followed by standard filter	2h	MINIMUM	minimum of footprint	3h	MAXIMUM	maximum of footprint
		Value	Name	Description													
		0h	STD_FILTER	standard filter													
		1h	COMPARISON	comparison followed by standard filter													
2h		MINIMUM	minimum of footprint														
3h		MAXIMUM	maximum of footprint														
Programming Notes																	
The following message types ignore this field: <i>sample_min</i> , <i>sample_max</i> , <i>sample_unorm*</i> , <i>resinfo</i> , <i>sampleinfo</i> , <i>LOD</i> , <i>ld*</i> , <i>sample_8x8</i> .																	
If the current min/mag filter mode is MAPFILTER_MONO, this field is ignored.																	
The <i>sample_c</i> , <i>sample_l_c</i> , <i>sample_d_c</i> , <i>sample_b_c</i> , <i>gather4_c</i> , and <i>gather4_po_c</i> message types, when used with STD_FILTER, MINIMUM, or MAXIMUM settings of this field, perform the operation of the message of the same name without the "_c". The ref parameter is ignored by hardware.																	
For message types not listed above, when used with COMPARISON setting of this field, perform the operation of the message of the same name with "_c" included. The ref parameter used by the operation (since it is not delivered in the message) is set to zero.																	



SAMPLER_STATE

	Restrictions applying to the message whose behavior is being performed must be followed. For example, a sample message used with COMPARISON reduction filter must follow all of the restrictions of <i>sample_c</i>. An exception to this is the MINIMUM and MAXIMUM reduction types allow SURFTYPE_1D, 2D, 3D, and CUBE, including with Surface Array enabled, even though the sample_min/max messages only allow 2D. Restrictions applying to the message delivered need not be followed. For example, a <i>sample_c</i> message used with STD_FILTER reduction filter needs to follow only the restrictions of sample, not the restrictions of <i>sample_c</i>.																											
21:19	Maximum Anisotropy Format: U3 Enumerated Type This field clamps the maximum value of the anisotropy ratio used by the MAPFILTER_ANISOTROPIC filter (Min or Mag Mode Filter). <table><thead><tr><th>Value</th><th>Name</th><th>Description</th></tr></thead><tbody><tr><td>0h</td><td>RATIO 2:1</td><td>At most a 2:1 aspect ratio filter is used</td></tr><tr><td>1h</td><td>RATIO 4:1</td><td>At most a 4:1 aspect ratio filter is used</td></tr><tr><td>2h</td><td>RATIO 6:1</td><td>At most a 6:1 aspect ratio filter is used</td></tr><tr><td>3h</td><td>RATIO 8:1</td><td>At most a 8:1 aspect ratio filter is used</td></tr><tr><td>4h</td><td>RATIO 10:1</td><td>At most a 10:1 aspect ratio filter is used</td></tr><tr><td>5h</td><td>RATIO 12:1</td><td>At most a 12:1 aspect ratio filter is used</td></tr><tr><td>6h</td><td>RATIO 14:1</td><td>At most a 14:1 aspect ratio filter is used</td></tr><tr><td>7h</td><td>RATIO 16:1</td><td>At most a 16:1 aspect ratio filter is used</td></tr></tbody></table>	Value	Name	Description	0h	RATIO 2:1	At most a 2:1 aspect ratio filter is used	1h	RATIO 4:1	At most a 4:1 aspect ratio filter is used	2h	RATIO 6:1	At most a 6:1 aspect ratio filter is used	3h	RATIO 8:1	At most a 8:1 aspect ratio filter is used	4h	RATIO 10:1	At most a 10:1 aspect ratio filter is used	5h	RATIO 12:1	At most a 12:1 aspect ratio filter is used	6h	RATIO 14:1	At most a 14:1 aspect ratio filter is used	7h	RATIO 16:1	At most a 16:1 aspect ratio filter is used
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4h	RATIO 10:1	At most a 10:1 aspect ratio filter is used																										
5h	RATIO 12:1	At most a 12:1 aspect ratio filter is used																										
6h	RATIO 14:1	At most a 14:1 aspect ratio filter is used																										
7h	RATIO 16:1	At most a 16:1 aspect ratio filter is used																										
18	U Address Mag Filter Rounding Enable Format: Enable Controls whether the texture address is rounded or truncated before being used to select texels to sample. Provides independent control of rounding on one texture address dimension (U/V/R) in either mag or min filter mode. Programming Notes Hardware will not force rounding enable.																											
17	U Address Min Filter Rounding Enable Format: Enable Controls whether the texture address is rounded or truncated before being used to select texels to sample. Provides independent control of rounding on one texture address dimension (U/V/R) in either mag or min filter mode. Programming Notes Hardware will not force rounding enable.																											
16	V Address Mag Filter Rounding Enable Format: Enable Controls whether the texture address is rounded or truncated before being used to select texels to sample. Provides independent control of rounding on one texture address dimension (U/V/R)																											



SAMPLER_STATE

		in either mag or min filter mode.
		Programming Notes
		Hardware will not force rounding enable.
15	V Address Min Filter Rounding Enable	
	Format:	Enable
	Controls whether the texture address is rounded or truncated before being used to select texels to sample. Provides independent control of rounding on one texture address dimension (U/V/R) in either mag or min filter mode.	
		Programming Notes
		Hardware will not force rounding enable.
14	R Address Mag Filter Rounding Enable	
	Format:	Enable
	Controls whether the texture address is rounded or truncated before being used to select texels to sample. Provides independent control of rounding on one texture address dimension (U/V/R) in either mag or min filter mode.	
		Programming Notes
		Hardware will not force rounding enable.
13	R Address Min Filter Rounding Enable	
	Format:	Enable
	Controls whether the texture address is rounded or truncated before being used to select texels to sample. Provides independent control of rounding on one texture address dimension (U/V/R) in either mag or min filter mode.	
		Programming Notes
		Hardware will not force rounding enable.
12:11	Trilinear Filter Quality	
	Format:	U2 Enumerated Type
	Selects the quality level for the trilinear filter.	
	Value	Name
	0	FULL
	1	TRIQUAL_HIGH/MAG_CLAMP_MIPFILTER
	2	MED
	3	LOW
		Description
		Full Quality. Both mip maps are sampled under all circumstances.
		If High Quality. Same as full quality.
		If Medium Quality. If the contribution of one mip map is less than 25%, only the other mip map contributes.
		If Low Quality. If the contribution of one mip map is less than 37.5%, only the other mip map contributes.



SAMPLER_STATE

	10	Non-normalized Coordinate Enable	
		Format:	Enable
		This field, if enabled, specifies that the input coordinates (U/V/R) are in non-normalized space, where each integer increment is one texel on LOD 0. If disabled, coordinates are normalized, where the range 0 to 1 spans the entire surface.	
		Programming Notes	
		The following state must be set as indicated if this field is <i>enabled</i>: • TCX/Y/Z Address Control Mode must be TEXCOORDMODE_CLAMP, TEXCOORDMODE_HALF_BORDER, or TEXCOORDMODE_CLAMP_BORDER. • Surface Type must be SURFTYPE_2D or SURFTYPE_3D. • Mag Mode Filter must be MAPFILTER_NEAREST or MAPFILTER_LINEAR. • Min Mode Filter must be MAPFILTER_NEAREST or MAPFILTER_LINEAR. • Mip Mode Filter must be MIPFILTER_NONE. • Min LOD must be 0. • Max LOD must be 0. • MIP Count must be 0. • Surface Min LOD must be 0. • Texture LOD Bias must be 0.	
	9	Reduction Type Enable	
		Format:	Enable
		This field enables the Reduction Type field to modify the behavior of messages based on its setting. If this field is disabled, all messages behave as defined and the Reduction Type field is ignored.	
	8:6	TCX Address Control Mode	
		Format:	Texture Coordinate Mode Enumerated Type
		Controls how the 1st (TCX, aka U) component of input texture coordinates are mapped to texture map addresses - specifically, how coordinates "outside" the texture are handled (wrap/clamp/mirror). The setting of this field is subject to being overridden by the Cube Surface Control Mode field when sampling from a SURFTYPE_CUBE surface.	
		Programming Notes	
		When using cube map texture coordinates, each TC component must have the same Address Control Mode.	
		When TEXCOORDMODE_CUBE is not used accessing a cube map, the map's Cube Face Enable field must be programmed to 111111b (all faces enabled).	
		MAPFILTER_MONO: Texture addressing modes must all be set to TEXCOORDMODE_CLAMP_BORDER. The Border Color is ignored in this mode, a constant value of 0 is used for border color. Software must pad the border texels within the map itself with 0.	
		If Surface Format is PLANAR*, this field must be set to TEXCOORDMODE_CLAMP.	
	5:3	TCY Address Control Mode	



SAMPLER_STATE

SAMPLER_STATE								
		<table><tr><td>Format:</td><td>Texture Coordinate Mode Enumerated Type</td></tr></table> Controls how the 2nd (TCY, aka V) component of input texture coordinates are mapped to texture map addresses - specifically, how coordinates "outside" the texture are handled (wrap/clamp/mirror). See Address TCX Control Mode above for details <table><tr><td colspan="2">Programming Notes</td></tr><tr><td colspan="2">If this field is set to TEXCOORDMODE_CLAMP_BORDER or TEXCOORDMODE_HALF_BORDER and a 1D surface is sampled, incorrect blending with the border color in the vertical direction may occur.</td></tr></table>	Format:	Texture Coordinate Mode Enumerated Type	Programming Notes		If this field is set to TEXCOORDMODE_CLAMP_BORDER or TEXCOORDMODE_HALF_BORDER and a 1D surface is sampled, incorrect blending with the border color in the vertical direction may occur.	
Format:	Texture Coordinate Mode Enumerated Type							
Programming Notes								
If this field is set to TEXCOORDMODE_CLAMP_BORDER or TEXCOORDMODE_HALF_BORDER and a 1D surface is sampled, incorrect blending with the border color in the vertical direction may occur.								
2:0	TCZ Address Control Mode	<table><tr><td>Format:</td><td>Texture Coordinate Mode Enumerated Type</td></tr></table> Controls how the 3rd (TCZ) component of input texture coordinates are mapped to texture map addresses - specifically, how coordinates "outside" the texture are handled (wrap/clamp/mirror). See Address TCX Control Mode above for details	Format:	Texture Coordinate Mode Enumerated Type				
Format:	Texture Coordinate Mode Enumerated Type							



SubslicePool

SubslicePool			
Source:	BSpec		
Size (in bits):	32		
Default Value:	0x00000000		
These fields specify the assignment of EUs within the given subslice to one of two pools. Bit 7..0 correspond to EU7..0 in the subslice. Assignment of the corresponding EU is to Pool-0 if its bit=0, or Pool-1, if its bit=1. Bit values in bit positions of non-existent or disabled EUs must be set to 0.			
DWord	Bit	Description	
0	31:24	Subslice3	
		Default Value:	00h Default Value
		Format:	U8
	23:16	Subslice2	
		Default Value:	00h Default Value
		Format:	U8
	15:8	Subslice1	
		Default Value:	00h Default Value
		Format:	U8
	7:0	Subslice0	
		Default Value:	00h Default Value
		Format:	U8



Surface Binding Table Index Message Descriptor Control Field

MDC_BTS - Surface Binding Table Index Message Descriptor Control Field				
Source:		BSpec		
Size (in bits):		8		
Default Value:		0x00000000		
DWord	Bit	Description		
0	7:0	Binding Table Index		
		Format:	Enumeration	
		Specifies the Binding Table index for the message, which must be a Surface State Model.		
		Value	Name	Description
		00h-0EFh	BTS	Index of Binding Table State Surfaces
		F0h-0FBh	Reserved	Reserved for future use
		0FCh	Reserved	Reserved for future use
		Others	Reserved	Ignored



Surface or Stateless Binding Table Index Message Descriptor Control Field

MDC_BT_S_A32 - Surface or Stateless Binding Table Index Message Descriptor Control Field																							
Source:		BSpec																					
Size (in bits):		8																					
Default Value:		0x00000000																					
DWord	Bit	Description																					
0	7:0	Binding Table Index																					
		Format: Enumeration																					
		Specifies the surface for the message, either Surface State Model or Stateless.																					
		<table><thead><tr><th>Value</th><th>Name</th><th>Description</th></tr></thead><tbody><tr><td>00h-0EFh</td><td>BTS</td><td>Index of Binding Table State Surfaces</td></tr><tr><td>F0h-0FBh</td><td>Reserved</td><td>Reserved for future use</td></tr><tr><td>0FCh</td><td>Reserved</td><td>Reserved for future use</td></tr><tr><td>0FFh</td><td>A32_A64</td><td>Specifies a A32 or A64 Stateless access that is locally coherent (coherent within a thread group)</td></tr><tr><td>0FDh</td><td>A32_A64_NC</td><td>Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).</td></tr><tr><td>Others</td><td>Reserved</td><td>Ignored</td></tr></tbody></table>	Value	Name	Description	00h-0EFh	BTS	Index of Binding Table State Surfaces	F0h-0FBh	Reserved	Reserved for future use	0FCh	Reserved	Reserved for future use	0FFh	A32_A64	Specifies a A32 or A64 Stateless access that is locally coherent (coherent within a thread group)	0FDh	A32_A64_NC	Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).	Others	Reserved	Ignored
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		0FDh	A32_A64_NC	Specifies a A32 or A64 Stateless access that is non-coherent (coherent within a thread).																			
Others	Reserved	Ignored																					
Restriction																							
Restriction : When using A32_A64_NC, SW must ensure that 2 threads do not both access the same cache line (64B)																							



SW Generated BINDING_TABLE_STATE

SW Generated BINDING_TABLE_STATE		
Source:	BSpec	
Size (in bits):	32	
Default Value:	0x00000000	
Description		
The binding table binds surfaces to logical resource indices used by shaders and other compute engine kernels. It is stored as an array of up to 256 elements, each of which contains one dword as defined here. The start of each element is spaced one dword apart.		
The first element of the binding table is aligned to a 64-byte boundary.		
Binding table indexes beyond 256 will automatically be mapped to entry 0 by the HW, w/ the exception of any messages which support the special indexes 255 and 254.		
DWord	Bit	Description
0	31:6	Surface State Pointer
		Format: SurfaceStateOffset[31:6] This 64-byte aligned address points to a surface state block. This pointer is relative to the Surface State Base Address
	5	Reserved
		Format: MBZ
	4:0	Reserved
Format: MBZ		



Intel® Open Source HD Graphics

Programmer's Reference Manual

For the 2016 Intel Atom™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Apollo Lake" Platform (Broxton Graphics)

Volume 3: Configurations

May 2017, Revision 1.0



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Configurations Overview

The Intel "Gen" Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and implementation have evolved to add many new features, increase performance, and improve power efficiency.

Each product generation has its own configurations chapter. Each chapter has a section for each project, and each project contains the following subsections:

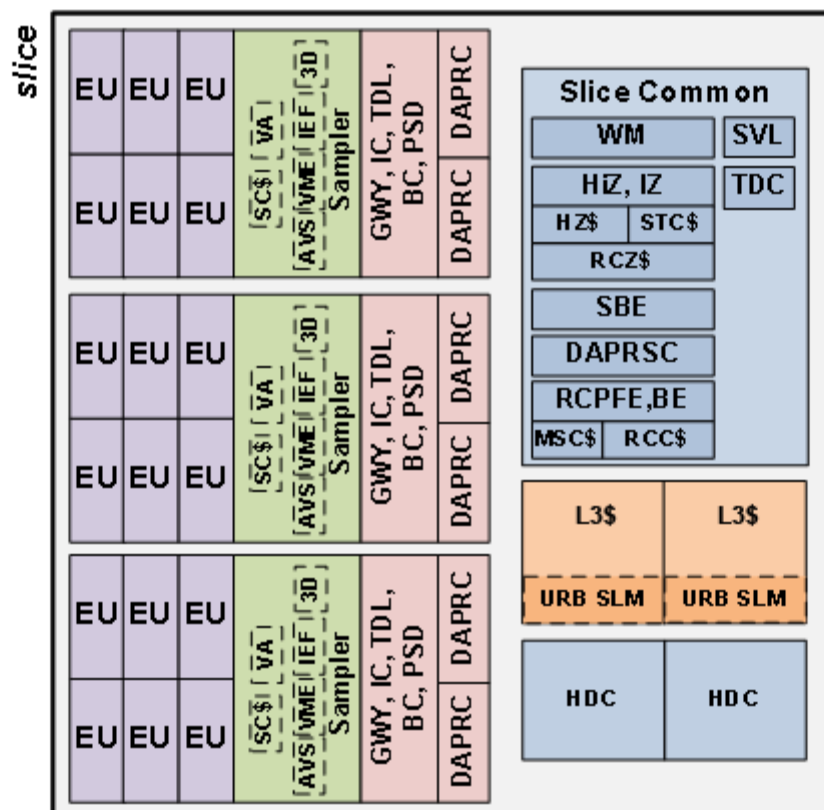
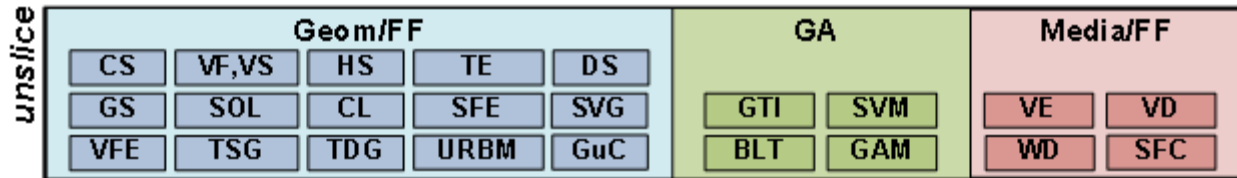
- Top Level Block Diagrams - Show basic feature blocks of the project's graphics architecture, for GT configurations.
- Device Attributes - List details of the graphics configuration options for each project.
- Steppings and Device IDs - Lists all of the current unique GT Die / Packages for a specific project.



Top Level Block Diagrams

This topic shows basic feature blocks of the Broxton (BXT) graphics architecture.

3x6 Configuration



This diagram is based on the following functional partitions:

- Geometry Fixed Functions (Geom/FF)
- Media Fixed Functions (Media/FF)
- Global Assets and GT Interface (GA)
- One or more Subslices (three shown)
- A Slice Common block
- An L3 Cache (L3\$) block



Note that the combination of (a), (b), and (c) is typically referred to as the “unslice”, while a combination of (d), (e), and (f) is referred to as a compute “slice”.

The functionality in each of these groupings is further broken down as follows:

- Unslicing – Fixed function pipelines for 3D, GPGPU, and Media operations, and interface to the outside world.
 - The 3D Geometry / Fixed Function (Geom/FF) block consisting of:
 - 3D fixed function pipeline (Command Stream-CS, Vertex Fetch-VF, Vertex Shader-VS, Hull Shader-HS, Tessellation Engine-TE, Domain Shader-DS, Geometry Shader-GS, Stream Output Logic-SOL, Clipper-CL, Strip/Fan Engine-SF, State Variable Global-SVG)
 - Video Front-End unit (VFE)
 - Thread Spawner unit (TSG) and the global Thread Dispatcher unit (TDG)
 - Unified Return Buffer Manager (URBM)
 - Media fixed function assets:
 - Video Decode (VD) Box
 - Video Encode (VE) Box
 - Wireless Display (WD) BOX
 - SFC
 - The Global Assets (GA) block as the primary interface and memory stream gateway to the outside world, consisting of:
 - GT Interface (GTI)
 - State Variable Manager (SVM)
 - Blitter (BLT)
 - Graphics Arbiter (GAM)
- Subslice (three shown) – A compute unit with supporting fixed- or shared-function assets sufficient for the EU capability.
 - A bank of Execution Units (EUs) – eight per subslice shown
 - Sampler, supporting both media and 3D functions
 - Gateway (GWY)
 - Instruction cache (IC)
 - Local Thread Dispatcher (TDL)
 - Barycentric Calculator (BC)
 - Pixel Shader Dispatcher (PSD)
 - Data Cluster (HDC)
 - Dataport Render Cache (DAPRC) - two per subslice
- Slice Common – Scalable fixed function assets which support the compute horsepower provided two or more subslices.
 - 3D Fixed Function:



- Windower/Mask unit (WM)
- Hi-Z (HZ) and Intermediate Z (IZ)
- Setup Backend (SBE)
- RCPFE, BE
- 3D stream caches (RCC\$, MSC\$, HZ\$, STC\$, RCZ\$)
- Media Fixed Functions:
 - DAPRSC
 - SVL
 - TDC
- L3 Cache – backing L3 cache for certain memory streams emanating from subslices.
 - L3 Data cache with support for data, URB, and shared local memory (SLM)



Device Attributes

The following table lists detailed GT device attributes for proposed BXT SKUs.

Product Configuration Attribute Table

Product Family	BXT
Architectural Name *	3x6
SKU Name	
Slice count	1
Subslice Count	3
EU/Subslice	6
EU count (total)	18
Thread Count	6
Thread Count (Total)	108
FLOPs/Ck - Half Precision, MAD (peak)	576
FLOPs/Ck - Single Precision, MAD (peak)	288
FLOPs/Ck - Double Precision, MAD (peak) [a]	36
Unslice clocking (coupled/decoupled from Cr slice) [b]	coupled
GTI / Ring Interfaces	1
GTI bandwidth (bytes/unslice-clk)	64: R
	64: W
Graphics Virtual Address Range	48 bit
Graphics Physical Address Range	39 bit
L3 Cache, total size (bytes)	384K
L3 Cache, bank count	2
L3 Cache, bandwidth (bytes/clk)	4x 64: R W
L3 Cache, D\$ Size (Kbytes)	192K-256K
URB Size (kbytes)	128K-192K
SLM Size (kbytes)	0, 128K
LLC/L4 size (bytes)	N/A
Instruction Cache (IC, bytes)	3x 48K
Color Cache (RCC, bytes)	24K
MSC Cache (MSC, bytes)	16K
HiZ Cache (HZC, bytes)	8K
Z Cache (RCZ, bytes)	32K
Stencil Cache (STC, bytes)	8K
FMAD, SP (ops/EU/clk)	8
FMUL, SP (ops/EU/clk)	8



FADD, SP (ops/EU/clock)	8
MIN,MAX, SP (ops/EU/clock)	8
CMP, SP (ops/EU/clock)	8
INV, SP (ops/EU/clock)	2
SQRT, SP (ops/EU/clock)	2
RSQRT, SP (ops/EU/clock)	2
LOG, SP (ops/EU/clock)	2
EXP, SP (ops/EU/clock)	2
POW, SP (ops/EU/clock)	1
IDIV, SP (ops/EU/clock)	1-6
TRIG, SP (ops/EU/clock)	2
FDIV, SP (ops/EU/clock)	1
Data Ports (HDC) [c]	2
L3 Load/Store - same addresses within msg (dwords/clock)	2x 32
L3 Load/Store - unique addresses within msg (dwords/clock)	
SLM Load//Store - same addresses within msg (dwords/clock)	
SLM Load//Store - unique addresses within msg (dwords/clock)	
Atomic, Local 32b - same addresses within msg (dwords/clock)	
Atomic, Global 32b - unique addresses within msg (dwords/clock)	
Geometry pipes	1
Samplers (3D)	3
Texel Rate, point, 32b (tex/clock)	12
Texel Rate, point, 64b (tex/clock)	12
Texel Rate, point, 128b (tex/clock)	12
Texel Rate, bilinear, 32b (tex/clock)	12
Texel Rate, bilinear, 64b (tex/clock)	12
Texel Rate, bilinear, 128b (tex/clock)	6
Texel Rate, trilinear, 32b (tex/clock)	12
Texel Rate, trilinear, 64b (tex/clock)	6
Texel Rate, trilinear, 128b (tex/clock)	1.5
Texel Rate, aniso 2x, MIP Linear, 32b (tex/clock)	3
Texel Rate, aniso 4x, MIP Linear, 32b (tex/clock)	1.5
Texel Rate, aniso 8x, MIP Linear, 32b (tex/clock)	0.75
Texel Rate, aniso 16x, MIP Linear, 32b (tex/clock)	0.375
HiZ Rate, (ppc)	32
IZ Rate, (ppc)	16
Stencil Rate (ppc)	32



<i>(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)</i>	
Pixel Rate, fill, 32bpp (pix/clock, RCC hit)	8
Pixel Rate, fill, 32bpp (pix/clock, LLC hit @ 1.0x unslice clock)	N/A
Pixel Rate, fill, 32bpp (pix/clock, LLC hit, @ 1.5x unslice clock)	N/A
Pixel Rate, fill, 32bpp (pix/clock, memory, @ 1.0x unslice clock)	8
Pixel Rate, fill, 32bpp (pix/clock, memory, @ 1.5x unslice clock)	N/A
<i>(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)</i>	
Pixel Rate, blend, 32bpp (p/clock, RCC hit)	8
Pixel Rate, blend, 32bpp (p/clock, LLC hit, @ 1.0x unslice clock)	N/A
Pixel Rate, blend, 32bpp (p/clock, LLC hit, @ 1.5x unslice clock)	N/A
Pixel Rate, blend, 32bpp (pix/clock, memory, @ 1.0x unslice clock)	8
Pixel Rate, blend, 32bpp (pix/clock, memory, @ 1.5x unslice clock)	N/A
Samplers (media)	3
VDBox Instances	1
VEBox Instances	1
SFC Instances	1
WGBox Instances	1
Display Pipes	3
Display Planes per Pipe	4+4+3

Notes:

* Architectural Name = Subslice Count x EUs per Subslice

A brief explanation of the listed SKUs is as follows:

- 3x6 has three subslices, with six EUs each for a total of $3 \times 6 = 18$ EUs.

Programming Note	
Context:	Device Attributes
Double precision support in hardware is TBD.	

Programming Note	
Context:	Device Attributes
Unslice clock and slice clock are coupled; independent frequency control is not supported.	

Programming Note	
Context:	Device Attributes
Unlike other Gen variants, this version shares HDCs units across subslices.	



Steppings and Device IDs

Broxton GT Unique Devices

The following table lists current unique GT Die / Packages steppings for BXT. Prior to manufacturing, this information is subject to change at any time.

SOC SKU	GT SKU	SOC Stepping	GT/Disp Stepping	Native Device2 ID	GT Device2 Revision ID	Comments	Project
BXT	3x6	C0	D0	0x1A84 (18EU) 0x1A85 (12EU)	0x0C	PRQ Base Candidate	BXT:3x6
APL	3x6	B1	C0	0x5A84 (18 EU) 0x5A85 (12 EU)	0x0A	ApolloLake PRQ Base Candidate	BXT:3x6
APL	3x6	B2	C0	0x5A84 (18 EU) 0x5A85 (12 EU)	0x0B	ApolloLake PRQ for CCG	BXT:3x6
APL	3x6	E0	D0	0x5A84 (18 EU) 0x5A85 (12 EU)	0x0C	ApolloLake PRQ stepping for IOTG	BXT:3x6



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Volume 4: Memory Views

May 2017, Revision 1.0



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Graphics Memory Address Spaces

The *Graphics Memory Address Spaces* table lists the five supported Graphics Memory Address Spaces. Note that the Graphics Memory Range Removal function is automatically performed to transform system addresses to internal, zero-based Graphics Addresses.

Graphics Memory Address Types

Address Type	Description	Range	Gen9
GMADR	Address range allocated via the Device 2 (integrated graphics device) GMADR register. The processor and other peer (DMI) devices utilize this address space to read/write graphics data that resides in Main Memory. This address is internally converted to a GM_Address.	This is a 4 GB bar above physical memory.	128 MB, 256 MB, 512 MB, 1GB, 2GB, 4GB
GTTMMADR	The combined Graphics Translation Table Modification Range and Memory Mapped Range. The range requires 16 MB combined for MMIO and Global GTT aperture, with 8MB of that used by MMIO and 8MB used by GTT. GTTADR will begin at GTTMMADR + 8MB while the MMIO base address will be the same as GTTMMADR. For the Global GTT, this range is defined as a memory bar in graphics device config space. It is an alias into which software is required to write Page Table Entry values PTEs. Software may read PTE values from the global Graphics Translation Table GTT. PTEs cannot be written directly into the global GTT memory area.	This is a 16MB bar above physical memory.	16 MB (2 MB MMIO + 6 MB reserved + 8 MB GGTT)
GTTMMADR	The MMIO allocation will either be : 2MB MMIO + 6MB reserved..	This is a 16MB bar above physical memory.	16MB (2MB MMIO + 6MB reserved + 8MB GGTT)
GSM	GTT Stolen Memory. It is an 8 MB (max) region taken out of physical memory to store the Global GTT entries for page translations specific to GFX driver use. It is accessible via GTTMMADR from the CPU path however GPU/DE can access the same region directly.	This is an 8 MB region in physical memory not visible to OS.	1 MB, 2 MB, 4 MB, 8 MB

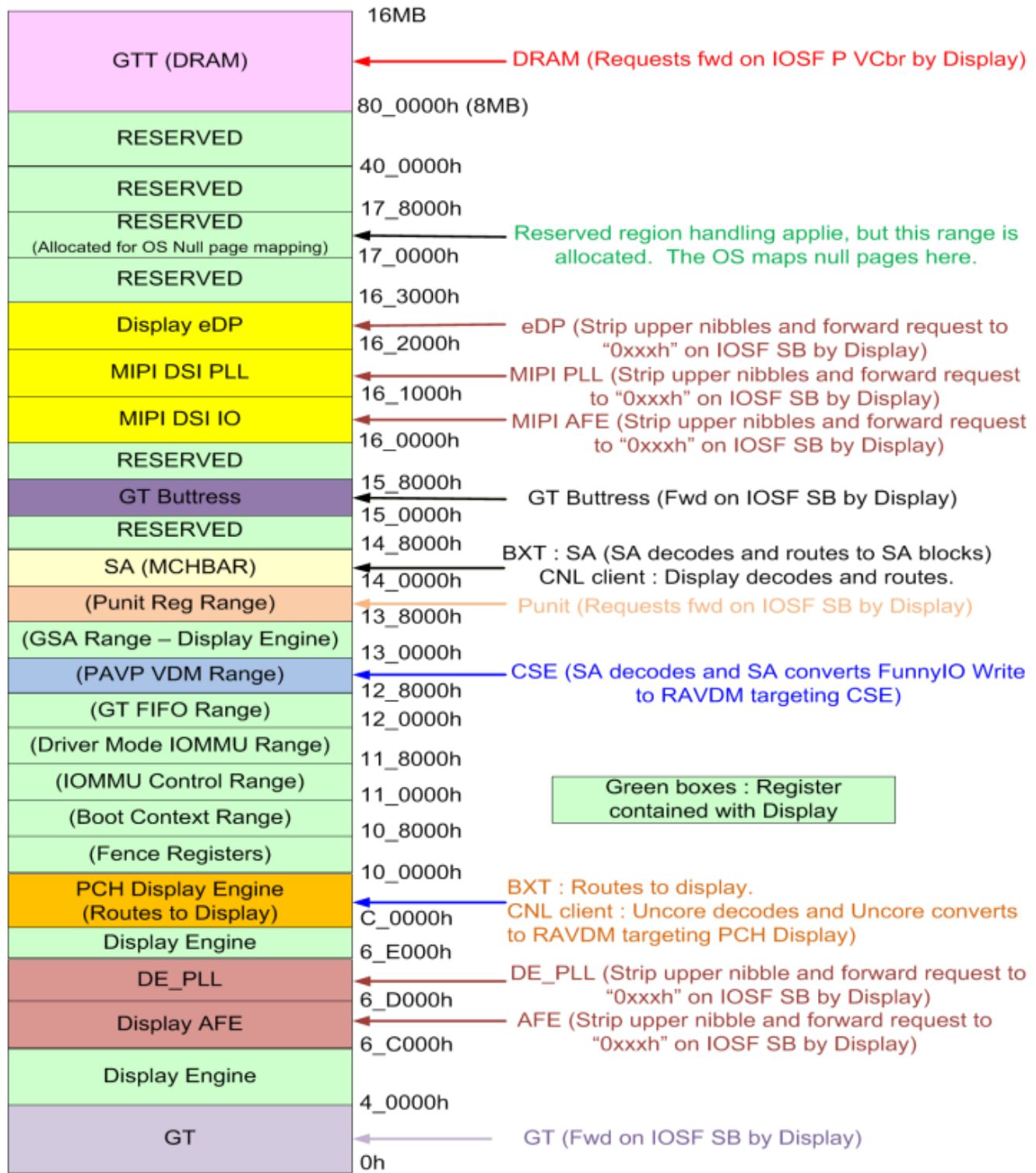


Address Type	Description	Range	Gen9
DSM	Data stolen memory, the size is determined with GMS filed (8 bits) with MAX size of 4 GB. This is a stolen memory which can be accessed via GMADR for CPU and directly for GPU/DE. Size is programmable with 32 MB multiplier. First 4KB of DSM has to be reserved for GFX hardware use.	This is a max of 4 GB stolen physical memory for GFX data structures.	0 MB, 32 MB, 64 MB, 96 MB, ...4096MB
PCM/WOPCM	Reserved within the DSM for protected content functions.	Limited by the DWM size, base is programmable.	

Next level breakdown for GTTMMADR is given below.

Software is allowed to use range x17_0000 to x17_FFFF as the Null range.

GTTMMADR targets





TLB – Final Page Entry

The size of the TLBs has been increased over the previous generation and should be targeting using the following list:

- L3 TLB: 768 TLB entries – This is where all HDC, I\$, Constant, State, and Sampler streams are stored.
- MFX: 512 TLB entries – All Media streams (split 256/256 between two media engines).
- BLT: 32 entries.
- Z: 512 TLB entries – All depth accesses.
- C: 256 (256 TLB entries) – All color accesses.
- FF: 128 (128 TLB entries) – All FF accesses to memory.
- VLF: 32 (32 TLB entries) – Media surface.
- GAV: 64 (64 TLB entries) – Video enhancement.
- WiDi: 64 (64 TLB entries) – Wireless Display.

All TLB entries are increased to 48b to contain larger address as well as the page attributes attached to it.

The max size of a single TLB is 256 entries, larger quantities have to be handled as set-associative storages. Set associativity will be managed by low order page bits (i.e. address#12, address#13, ...).

Both Color and Z TLBs are designed to process a single memory request per cycle. To achieve a higher throughput where concurrent Color or Z read/write's are used, following register bit needs to be enabled: mmio0x04A30h [31]

The sizes of RCCTLB and ZTLB only have 256 entries.

Since there is a reduced number of TLB entries in BXT, *the recommended TLB entry allocation in BXT is as follows:*

- When TR-TT is enabled
 - ZTLB: STC(64), HiZ(128), RCZ(48), GATR(16)
 - RCCTLB: MSC(128), RCC(112), GATR(16)
- When TR-TT is disabled
 - ZTLB: STC(64), HiZ(128), RCZ(64)

RCCTLB: MSC(128), RCC(128)



The size of the L3 TLB is also different between projects. The default TLB entry allocations are:

- BXT (L3TLB-Gfx **512**): L3(**64**:0-63), DC(**80**:64-143), TX(**352**:144-495), GATR(**16**:496-511)
- BXT (L3TLB-GPGPU **512**): L3(**64**:0-63), DC(**368**:64-431), TX(**80**:432-511)

For giving more TLB resources for both DC and TX, the following allocations are recommended.

- BXT (L3TLB-Gfx **512**): L3(**64**:0-63), DC(**432**:64-495), TX(**432**:64-495), GATR(**16**:496-511)
- BXT (L3TLB-GPGPU **512**): L3(**64**:0-63), DC(**448**:64-511), TX(**448**:64-511)



Intel® Open Source HD Graphics

Programmer's Reference Manual

For the 2016 Intel Atom™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Apollo Lake" Platform (Broxton Graphics)

Volume 5: Command Stream Programming

May 2017, Revision 1.0



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User Mode Privileged Commands..... 1



User Mode Privileged Commands

A subset of the commands are privileged. These commands may be issued only from a privileged batch buffer or directly from a ring. Batch buffers in GGTT memory space are privileged and batch buffers in PPGTT memory space are non-privileged. On parsing privileged command from a non-privileged batch buffer, a Command Privilege Violation Error is flagged and the command is dropped. Command Privilege Violation Error is logged in Error identity register of command streamer which gets propagated as "Command Parser Master Error" interrupt to SW. Privilege access violation checks in HW can be disabled by setting "Privilege Check Disable" bit in GFX_MODE register. When privilege access checks are disabled HW executes the Privilege command as expected.

User Mode Privileged Commands

User Mode Privileged Command	Function in Non-Privileged Batch Buffers	Source
MI_UPDATE_GTT	Command is converted to NOOP.	*CS
MI_STORE_DATA_IMM	Command is converted to NOOP if Use Global GTT is enabled.	*CS
MI_STORE_DATA_INDEX	Command is converted to NOOP.	*CS
MI_STORE_REGISTER_MEM	Register read is always performed. Memory update is dropped if Use Global GTT is enabled.	*CS
MI_BATCH_BUFFER_START	Command when executed from a batch buffer can set its "Privileged" level to its parent batch buffer or lower. Chained or Second level batch buffer can be "Privileged" only if the parent or the initial batch buffer is "Privileged". This is HW enforced.	*CS
MI_LOAD_REGISTER_IMM	Command is converted to NOOP if the register accessed is privileged.	*CS
MI_LOAD_REGISTER_MEM	Command is converted to NOOP if Use Global GTT is enabled. Command is converted to NOOP if the register accessed is privileged.	*CS
MI_LOAD_REGISTER_REG	Register write to a Privileged Register is discarded.	*CS
MI_REPORT_PERF_COUNT	Command is converted to NOOP if Use Global GTT is enabled.	Render CS
PIPE_CONTROL	Still send flush down, Post-Sync Operation is NOOP if Use Global GTT or Use "Store Data Index" is enabled. Post-Sync Operation LRI to Privileged Register is discarded.	Render CS
MI_SET_CONTEXT	Command is converted to NOOP.	Render CS



User Mode Privileged Command	Function in Non-Privileged Batch Buffers	Source
MI_ATOMIC	Command is converted to NOOP if Use Global GTT is enabled.	Render CS
MI_COPY_MEM_MEM	Command is converted to NOOP if Use Global GTT is used for source or destination address.	*CS
MI_SEMAPHORE_WAIT	Command is converted to NOOP if Use Global GTT is enabled.	*CS
MI_SEMAPHORE_WAIT	Command is converted to NOOP, if Register Poll is enabled	*CS
MI_ARB_ON_OFF	Command is converted to NOOP.	*CS
MI_DISPLAY_FLIP	Command is converted to NOOP.	*CS
MI_CONDITIONAL_BATCH_BUFFER_END	Command is converted to NOOP if Use Global GTT is enabled.	*CS
MI_FLUSH_DW	Still send flush down, Post-Sync Operation is converted to NOOP if Use Global GTT or Use "Store Data Index" is enabled.	Blitter CS, Video CS, Video Enhancement CS

Parsing one of the commands in the table above from a non-privileged batch buffer flags an error and converts the command to a NOOP.

The tables below list the non-privileged registers that can be written to from a non-privileged batch buffer executed from various command streamers.

User Mode Non-Privileged Registers for Blitter Command Streamer (BCS)

MMIO Name	MMIO Offset	Size in DWords
BCS_GPR	0x22600	32
BCS_SWCTRL	0x22200	1

This table represents the Base offset for Video Command Streamers and Media Engine message range:

Unit	MMIO Base Offset	Description
VCS/MFC	0x12000	Video Command Streamer 0
VCS1/MFC1	0x1C000	Video Command Streamer 1
VECS	0x1A000	Video Enhancement Command Streamer
HUC	0xD000	
HEVC	0x1E900	

**User Mode Non-Privileged Registers for Video Enhancement Command Streamer (VECS)**

MMIO Name	MMIO Base	MMIO Offset	Size in DWords
VECS_GPR	VECS	0x600	32

User Mode Non-Privileged Registers for Video Command Streamer (ALL VCS)

MMIO Name	Unit Base	MMIO Range	Size in DWords
VCS_GPR	VCS	0x600	32
MFC_VDBOX1	VCS	0x800-0xFFF	512
HuC	HUC	0x0A0	4
HuC	HUC	0x064	1
HuC	HUC	0x080	1
HEVC	HEVC	0x00	64
HEVC-Enc	HEVC	0x00	64



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Shared Functions

3D Sampler

State

The 3D sampler uses both surface state objects (RENDER_SURFACE_STATE) as well as sampler state objects (SAMPLER_STATE). These objects are cached locally in the sampler state cache for improved performance as it is assumed that many sampler messages will utilize the same surface and sampler states.

Surface State Fetch

Surface state is fetched from system memory using a Binding Table Pointer (**BTP**). The **BTP** is a 16-bit value provided by the command stream (not directly by the shader) which determines the binding-table to be used. An 8-bit Binding Table Index (**BTI**) is then provided by the shader via the message descriptor, which indicates the offset into the Binding Table. The BTP and BTI are relative to the **Surface State Base Address** and the binding table itself resides in system memory. The contents of the Binding Table is a list of pointers to surface state objects. The pointer from the Binding Table is also relative to the **Sampler State Base Address**, and points directly to a 256-bit **RENDER_SURFACE_STATE** object which sampler will fetch and store in its internal state cache.

Sampler State Fetch

SAMPLER_STATE objects are fetched independently of surface state and cached locally in the 3D sampler independently (there may one or more **SAMPLER_STATE** objects associates with one or more **RENDER_SURFACE_STATE** objects). The sampler state is fetched using the **Sampler State Pointer (SSP)** which is provided either in the message header or directly from the command stream (message headers are not required). The **SSP** is an offset relative to the **Dynamic_State_Base_Address** and selects a table of 16 sampler states. The 4-bit **Sampler Index (SI)** in the message descriptor is used to select the specific **SAMPLER_STATE** object to be fetched from system memory and cached locally in the 3D sampler.

Bindless Sampler State

The sampler supports a "Bindless" sampler model. Bindless in this case does not actually refer to the lack of a Binding table since the legacy Sampler State model also did not have a Binding Table. However, the mechanism is similar to bindless surfaces in that the pointer provided directly selects a **SAMPLER_STATE** object. The sampler uses the same **Sampler State Pointer (SSP)**, but it is relative to the **Bindless_Surface_State_Base_Address** rather than the **Dynamic_State_Base_Addr**. Bindless Samplers can only be used in conjunction with Bindless Surfaces. The Sampler Index (SI) in the message descriptor is not used, and can be set to 0. The **SAMPLER_STATE** object is cached locally in the 3D sampler.



State Caching

As mentioned above, the 3D Sampler allows for automatic caching of **RENDER_SURFACE_STATE** objects and **SAMPLER_STATE** objects to provide higher performance. Coherency with system memory in the state cache, like the texture cache is handled partially by software. It is expected that the command stream or shader will issue Cache Flush operation or Cache_Flush sampler message to ensure that the L1 cache remains coherent with system memory.

Programming Note	
Context:	State Cache Coherency
Whenever the value of the Dynamic_State_Base_Addr, Surface_State_Base_Addr are altered, the L1 state cache must be invalidated to ensure the new surface or sampler state is fetched from system memory. Whenever the RENDER_SURFACE_STATE object in memory pointed to by the Binding Table Pointer (BTP) and Binding Table Index (BTI) is modified or SAMPLER_STATE object pointed to by the Sampler State Pointer (SSP) and Sampler Index (SI) is modified, the L1 state cache must be invalidated to ensure the new surface or sampler state is fetched from system memory.	

Messages

Message Header

The message header for the sampling engine is the same regardless of the message type. The message header is optional. If the header is not present, the behavior is as if the message was sent with all fields in the header set to zero and the write channel masks are all enabled and offsets are zero. However, if the header is not included in the message, the Sampler State Pointer will be obtained from the command stream input for the given thread.

When Response length is 0 for sample_8x8 message then the data from sampler is directly written out to memory using media write message.

DWord	Bits	Description
M0.5	31:5	Reserved
M0.5	4:0	Output format. Only for Sample_8x8 message with direct HDC write:
		0 YCRCB_NORMAL
		1 YCRCB_SWAPUVY
		2 YCRCB_SWAPUV
		3 YCRCB_SWAPY
		4 PLANAR_420_8 (NV12 only)
		5 Y8_UNORM
		6 Y16_SNORM
7-16	Reserved	

DWord	Bits	Description				
		<table><tr><td>17</td><td>Y32_UNORM</td></tr><tr><td>18</td><td>Reserved</td></tr></table>	17	Y32_UNORM	18	Reserved
17	Y32_UNORM					
18	Reserved					
M0.4	31:16	Destination Y Address (u16)				
M0.4	15:0	Destination X Address in bytes (u16) X Address should always be DWord-aligned.				
M0.3	31:4	Sampler State Pointer: Specifies the 16-byte aligned pointer to the sampler state table. This field is ignored for <i>ld</i> and <i>resinfo</i> message types. This pointer is relative to the Dynamic State Base Address or Bindless Surface State Base Address depending on the setting of Bindless Surface Base Address Select bit in the GT_Mode Register. Format = StateOffset[31:4] The Sampler State Pointer does not have to be defined by the Message Header (many messages do not require a message header). The Sampler State Pointer may be delivered from the Command Streamer without the need for a Message Header.				
M0.3	3:0	Ignored				
M0.2	31:24	Render Target or Destination Binding Table Index Specifies the index into the binding table for the render target or HDC for messages with response length of zero (the binding table index for the sampler surface is in the message descriptor). Format = U8 Range = [0,255]				
M0.2	23	Pixel Null Mask Enable Specifies whether the writeback message includes an extra phase indicating the pixel null mask. Refer to the <i>Writeback Message</i> section for details on format. This field must be disabled for sample+killpix and all SIMD32/64 messages. Format = Enable Ignored for Sample_8x8 message				
M0.2	22	SIMD Mode Extension If SIMD Mode in the message descriptor is set to SIMD8D/SIMD4x2, this field specifies which mode is used. For other SIMD Modes, this field is ignored. 0: SIMD8D 1: SIMD4x2				
M0.2	21	Reserved				
M0.2	20	Reserved				



DWord	Bits	Description						
M0.2	19:18	SIMD32/64 Output Format Control Specifies the output format of SIMD32/64 messages (sample_unorm* and sample_8x8). Ignored for other message types. Refer to the writeback message formats for details on how this field affects returned data. This field is ignored for sample_8x8 messages if the Function is not AVS and MinMaxFilter. For MinMaxFilter only 16 bit Full and 8 bit Full modes are supported. This field is ignored and not used for HDC write message. 0: 16 bit Full 1: 16 bit Chrominance Downsampled 2: 8 bit Full 3: 8 bit Chrominance Downsampled This feature should be programmed to 0h because non-0 values may cause data corruption in returned values.						
M0.2	17:16	Gather4 Source Channel Select: Selects the source channel to be sampled in the gather4* messages. Ignored for other message types. 0: Red channel 1: Green channel 2: Blue channel 3: Alpha channel For gather4*_c messages, this field must be set to 0 (Red channel).						
M0.2	15	Alpha Write Channel Mask: Enables the alpha channel to be written back to the originating thread. 0: Alpha channel is written back. 1: Alpha channel is not written back. <table><tr><th colspan="2">Programming Note</th></tr><tr><td>Context:</td><td>3D Sampler Messages</td></tr><tr><td colspan="2"> - A message with all four channels masked is not allowed. - This field must be set to zero for sample_8x8 in VSA mode. - For Sample_8x8 messages, Alpha/Blue/Red channels should be always masked (set to 1) and only Green channel is enabled (set to 0). - This field must be set to zero for all gather4* messages. </td></tr></table>	Programming Note		Context:	3D Sampler Messages	- A message with all four channels masked is not allowed. - This field must be set to zero for sample_8x8 in VSA mode. - For Sample_8x8 messages, Alpha/Blue/Red channels should be always masked (set to 1) and only Green channel is enabled (set to 0). - This field must be set to zero for all gather4* messages.	
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M0.2	14	Blue Write Channel Mask: See Alpha Write Channel Mask.						
M0.2	13	Green Write Channel Mask: See Alpha Write Channel Mask.						

DWord	Bits	Description												
M0.2	12	Red Write Channel Mask: See Alpha Write Channel Mask.												
M0.2	11:8	U Offset: The u offset from the <code>_aoffimmi</code> modifier on the <i>sample</i> or <i>ld</i> instruction in DX10. Must be zero if the Surface Type is SURFTYPE_CUBE or SURFTYPE_BUFFER. Must be set to zero if <code>_aoffimmi</code> is not specified. Format is S3 2's complement. <table><tr><th colspan="2">Programming Note</th></tr><tr><td>Context:</td><td>3D Sampler Messages</td></tr><tr><td colspan="2"> - This field is ignored for the <code>sample_unorm*</code>, <code>sample_8x8</code>, and deinterlace messages. - This field is ignored if the <i>offu</i> parameter is included in the <code>gather4*</code> messages. </td></tr></table>	Programming Note		Context:	3D Sampler Messages	- This field is ignored for the <code>sample_unorm*</code>, <code>sample_8x8</code>, and deinterlace messages. - This field is ignored if the <i>offu</i> parameter is included in the <code>gather4*</code> messages.							
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M0.2	7:4	V Offset: The v offset from the <code>_aoffimmi</code> modifier on the <i>sample</i> or <i>ld</i> instruction in DX10. Must be zero if the Surface Type is SURFTYPE_CUBE or SURFTYPE_BUFFER. Must be set to zero if <code>_aoffimmi</code> is not specified. Format is S3 2's complement. <table><tr><th colspan="2">Programming Note</th></tr><tr><td>Context:</td><td>3DSampler Messages</td></tr><tr><td colspan="2"> - This field is ignored for the <code>sample_unorm*</code>, <code>sample_8x8</code>, and deinterlace messages. - This field is ignored if the <i>offu</i> parameter is included in the <code>gather4*</code> messages. </td></tr></table> <table><tr><th colspan="2">Programming Note</th></tr><tr><td>Context:</td><td>Non-Normalized Floating-Point Coordinates</td></tr><tr><td colspan="2">Texel offsets can only be applied to messages with floating-point normalized coordinates or integer non-normalized coordinates.</td></tr></table>	Programming Note		Context:	3DSampler Messages	- This field is ignored for the <code>sample_unorm*</code>, <code>sample_8x8</code>, and deinterlace messages. - This field is ignored if the <i>offu</i> parameter is included in the <code>gather4*</code> messages.		Programming Note		Context:	Non-Normalized Floating-Point Coordinates	Texel offsets can only be applied to messages with floating-point normalized coordinates or integer non-normalized coordinates.	
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Texel offsets can only be applied to messages with floating-point normalized coordinates or integer non-normalized coordinates.														
M0.2	3:0	R Offset: The r offset from the <code>_aoffimmi</code> modifier on the <i>sample</i> or <i>ld</i> instruction in DX10. Must be zero if the Surface Type is SURFTYPE_CUBE or SURFTYPE_BUFFER. Must be set to zero if <code>_aoffimmi</code> is not specified. Format is S3 2's complement. <table><tr><th colspan="2">Programming Note</th></tr><tr><td>Context:</td><td>3D Sampler Messages</td></tr><tr><td colspan="2">This field is ignored for the <code>sample_unorm*</code>, <code>sample_8x8</code>, and deinterlace messages.</td></tr></table>	Programming Note		Context:	3D Sampler Messages	This field is ignored for the <code>sample_unorm*</code> , <code>sample_8x8</code> , and deinterlace messages.							
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M0.1	31:0	Reserved												
M0.0	31:0	Reserved												



Message Gateway

Message Payload

DWord	Bits	Description
M0.5	31:0	Ignored
M0.4	31:0	Ignored
M0.3	31:0	Predicate Mask. This field has a bit set per SIMD channel that passes the predicate. For SIMD8 and SIMD16 the rest of the bits must be 0. This field is ignored for non-predicated barriers.
M0.2	31	Barrier ID MSB. This field is bit[4] of the BarrierID, for full 5-bit barrier ID it should be combined with Barrier ID[3:0]. Format: U1
M0.2	30	Ignored
	27:24	BarrierID. This field indicates which one from the 16 Barrier States is updated. There is a fifth bit for the BarrierID, in bit 31. Format: U4 Note: This field location matches with that of R0 header.
	23:16	Ignored
	15	Barrier Count Enable. Allows the message to reprogram the terminating barrier count. If set, the stored value of the terminating barrier count is set to the value of Barrier Count field (below), and used for this barrier operation. If clear, the stored value of the terminating barrier count is not modified and the stored value is used for this barrier operation. Programming Note: This control is intended only for Hull Shader threads. Do not use this control if the barrier is linked with other barriers in other subslices (i.e. pooled EU thread groups in BXT). Format: Enable
	14:9	Barrier Count. If Barrier Count Enable is set, this field specifies the terminating barrier count. Otherwise this field is ignored. All threads that belong to a single barrier must deliver the same value for this field for a particular barrier iteration.
	8:0	Ignored
M0.1	31:0	Ignored
M0.0	31:4	Ignored



Media GPGPU Pipeline

This section discusses Programming the GPGPU Pipeline, Thread Group Tracking, Generic Media, and other related topics.

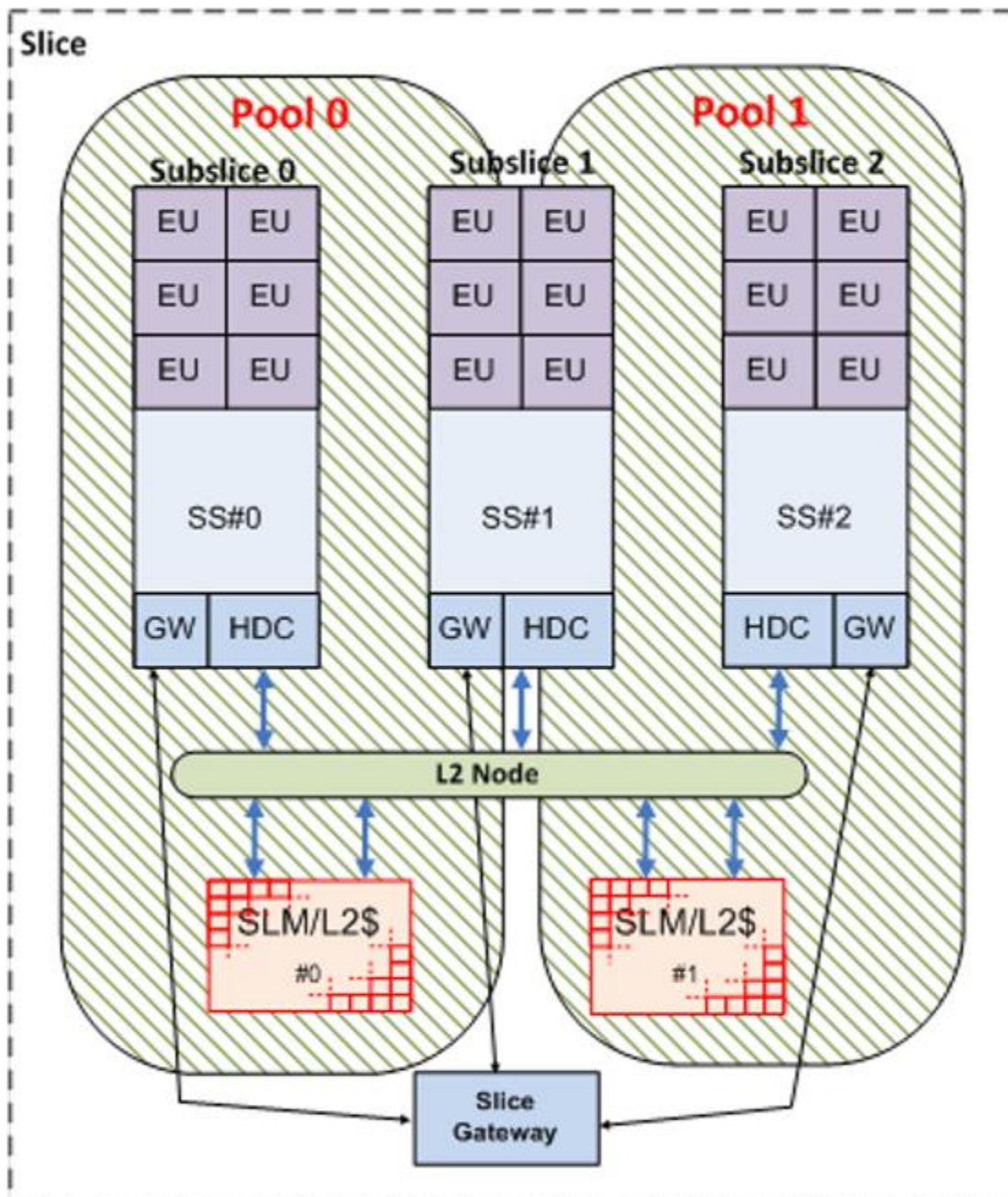
Thread Pools

Overview

Earlier project generations imposed a hardware-enforced restriction on the dispatching of workgroups to the EU array. Specifically a workgroup, broken down into threads, was dispatched in whole, entirely to a single subslice; no spanning of subslices was allowed. As long as an implementation's subslice size (EU * thread count) was sufficiently large, multiple workgroups of reasonably large sizes could be loaded onto a single subslice, filling the subslice's threads, providing good latency coverage leading to good performance. But for configurations with smaller subslice sizes, either in thread count per EU and/or EU count, and depending on workgroup size, this workgroup-per-subslice restriction could pose non-optimal thread loading and non-optimal performance.

The BXT project improves this situation by relaxing the workgroup-to-subslice coupling by aggregating EUs from different subslices into one or more 'virtual pools' to which a workgroup can be dispatched. For example, a configuration which has 3 subslices, each with 6 EUs, may create two virtual pools with 9 and 9 EUs each (see figure below). In terms of threads, if each EU has 6 threads, then the two pools have $9 \times 6 = 54$ threads each, vs. the three pools of $6 \times 6 = 36$ threads in previous architectural generations. Depending on the workgroup size, the pooled and larger aggregated pools allow for a larger integer number of workgroups to be active in the EU array at any instance, and minimize quantization problems in thread occupancy.

The creation of pools, and mapping of EUs into them, is done through the new MEDIA_POOL_STATE command. This command should be issued as part of context initialization. The setting is maintained as part of context state and preserved across context switch operations.



JIT Impact

Note that other than possibly providing more flexibility in the simd-ness of the JIT, this feature is kernel-transparent. The kernel itself is oblivious of thread-pools.

Pool Configuration Rules

The restrictions on pool configurations are described in MEDIA_POOL_STATE command.



Legacy-Mode

Primarily for the purposes of backward compatibility of drivers, a 'LegacyMode' is defined where the new thread-pools feature is disabled. In LegacyMode the workgroups are dispatched such that they are contained to only a single subslice. Additionally the subslice is coupled to a single bank of SLM, and all barriers of that thread-group remain local to the subslice.

LegacyMode may be set through a field in the MEDIA_POOL_STATE command. By default this mode is enabled. Only a single 'enable' bit is defined for the entire GT device, thus selection of PooledMode or LegacyMode is global setting across all slices in the implementation.

The performance while in LegacyMode may be significantly less than the architectural capability of the device. For example it may be that there is insufficient SLM banks to guarantee peak performance of kernels which stress Local Memory. Or it may be that there is insufficient total thread count in the subslice to handle large thread groups at the more desirable simd-8 or simd-16 execution width, and that simd-32 is required to handle the workgroup, and/or load/store operations are required and thereby introduce instruction overhead. Thus LegacyMode should be used intelligently with the understanding of its device-specific limitations.

GPGPU Commands

This section contains various commands for GPGPU, including a number of them shared with media mode.

MEDIA_VFE_STATE with varying definitions for different generations and projects:

MEDIA_CURBE_LOAD

MEDIA_INTERFACE_DESCRIPTOR_LOAD [

Interface Descriptor Data payload as pointed to by the Interface Descriptor Data Start Address, with varying definitions for different generations and projects:

MEDIA_STATE_FLUSH

MEDIA_POOL_STATE

SubslicePool

GPGPU Context Switch

Context switch allows the switch to take place in the middle of a thread group to provide better response time.

The command sequence has been simplified – MEDIA_STATE_FLUSH and MI_ARB_CHECK are now optional between commands for preemption to occur. MEDIA_STATE_FLUSH is now only needed before MEDIA_LOAD_CURBE commands to ensure CURBE is done being read before reloading it. The watermark bit in MEDIA_STATE_FLUSH is not needed, since the check is done automatically before a thread group is started.

Preemption can occur on commands listed here:



- **MI_ARB_CHECK**
- **MEDIA_STATE_FLUSH**
- **PIPE_CONTROL**
- **MI_WAIT_FOR_EVENT**
- **MI_SEMAPHORE_WAIT**
- **GPGPU_WALKER** – Preemption can occur at any time, with thread groups partially complete; the system state is saved/restored for context save and restore
- **MI_WAIT_FOR_EVENT**
- **MI_SEMAPHORE_WAIT**

Messages to the Sampler must use headers (controlled by bit 19 of the Message Descriptor) when preemption is enabled.

Note that command preemption is not supported for MEDIA_OBJECT_* commands for MI_ARB_ON/OFF should be used to prevent preemption except at frame boundaries, where an MI_ARB_CHECK should be inserted.

The memory map of the context image that is saved from GPGPU pipeline includes SLM and EU State. A contiguous space is allocated to save the SLM and EU State starting from the address provided in GPGPU_CSR_BASE_ADDRESS.

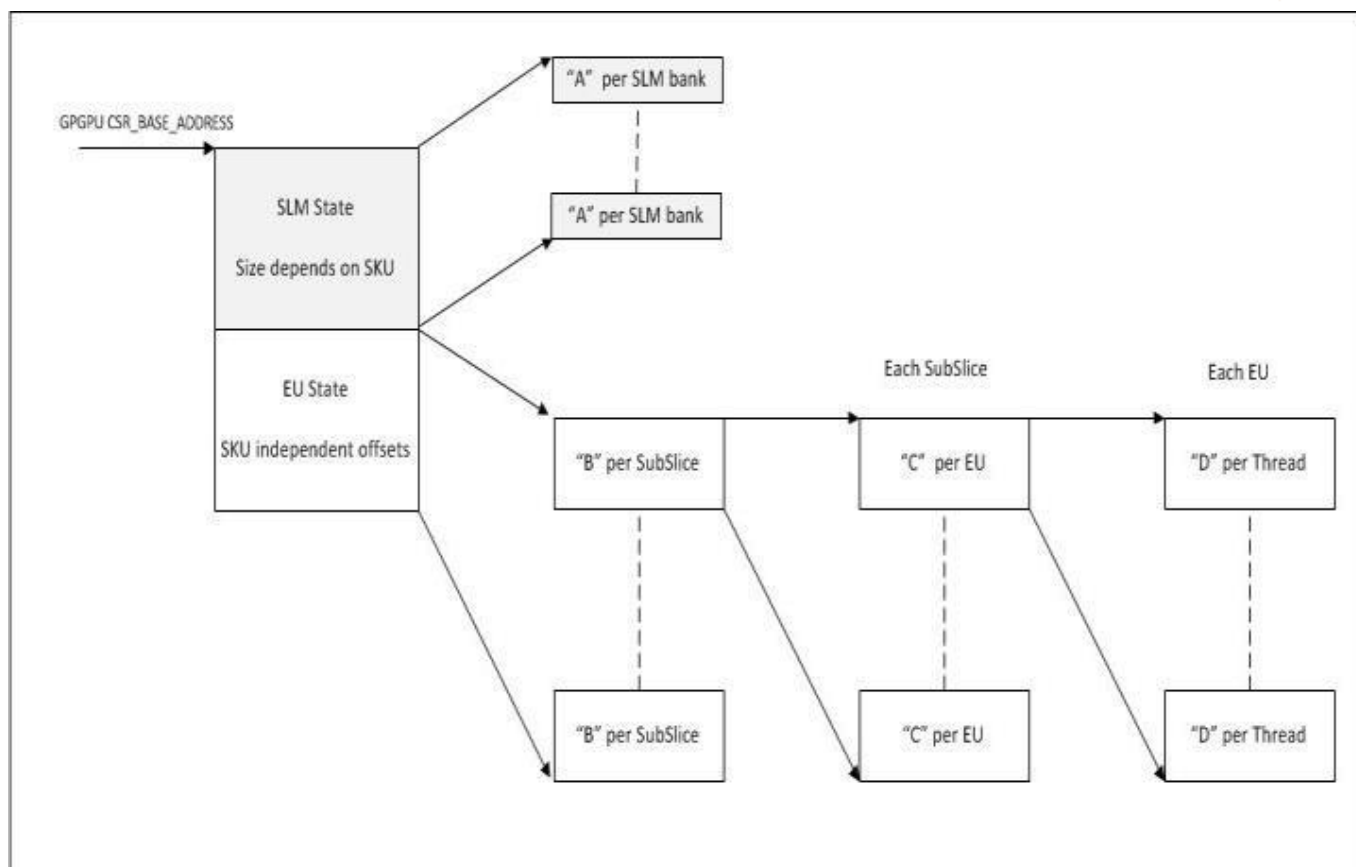
Maximum Upper Bound

Description
The maximum upper bound is set to 2MB for BXT-C.

In GPGPU context save/restore mode, hardware writes to this location and does NOT use the surface state or scratch space.

Memory Map of the GPGPU Context Image

The address offsets computed by hardware depend on the number of slices, subslices, EUs, and threads.



Base Address Calculation

Base Address = CSR_Base_Address + A * [Config.NumSImBanks] + B * SubSliceId + C * Euld + D * ThreadId + Message_Offset

A = 0x10000 // 64K SLM per SubSlice

B = C * [Config.NumEusPerSubSlice]

C = D * [Config.NumThreadsPerEu]

D = 0x2000 // 8KB

Note: The slicenumber and EUIDs may require re-mapping such that a contiguous space is used with no gaps inbetween.



Generic Media

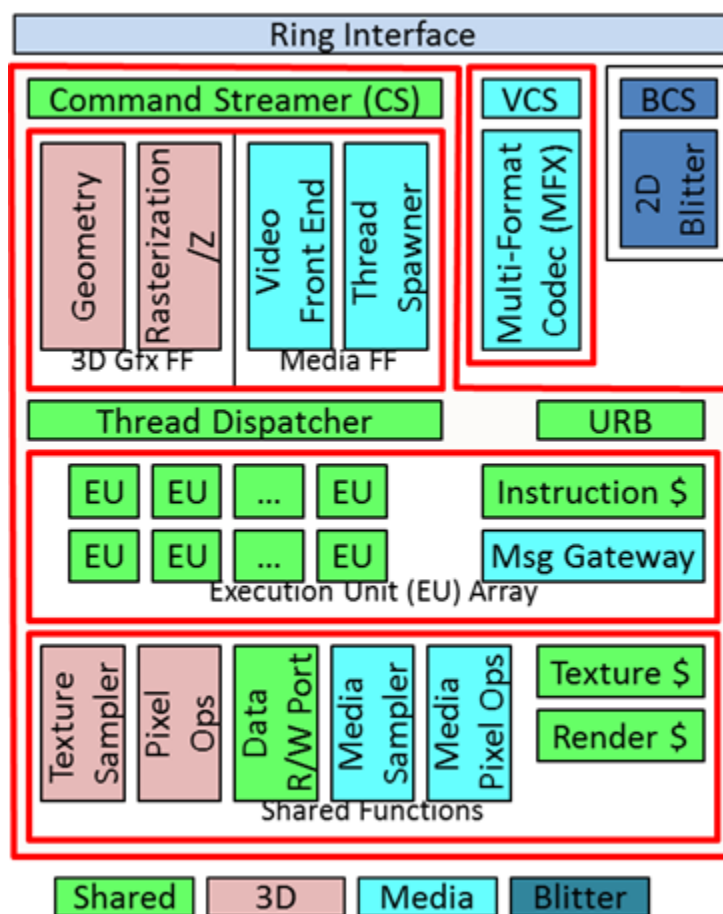
This introduction provides a brief overview of the Media product features. It includes Media functions, feature benefits, and how the features fit into graphics products as part of a whole solution.

Media product features include:

- Multi-format codec engine
- Video front end
- Media fixed functions
- Video encoding
- Video decoding
- Sampling

These product features support specific applications, such as interactive gaming, videogames, social media, virtual reality, and augmented reality.

The following block diagram shows the Main Render Engine, unified for 3D graphics and Media.



- **Fixed Function (FF) pipelines:** Provide thread generation and control.



- **3D graphics or Media FF:** Controls EU array at a given time. The EU (Execution Unit) array is shared between 3D and Media; ISA is optimized for both.
- **Shared functions:** Are accelerators to run filtered load, scatter, gather, and filter/blended store operations.
- **MXF:** Is a parallel codec engine that runs in a separate context.

Media State and Primitive Commands

This section contains various commands for media, all with the RenderCS source.

MEDIA_CURBE_LOAD

MEDIA_INTERFACE_DESCRIPTOR_LOAD

Interface Descriptor Data payload as pointed to by the Interface Descriptor Data Start Address:

The MEDIA_OBJECT command is the basic media primitive command for the media pipeline. It supports loading of inline data as well as indirect data. At least one form of payload (either inline, indirect, or CURBE) must be sent with the MEDIA_OBJECT.

MEDIA_OBJECT

MEDIA_OBJECT_PRT

The MEDIA_OBJECT_WALKER command uses the hardware walker in VFE for generating threads associated with a rectangular shaped object. It only supports loading of inline data or CURBE but not indirect data. At least one form of payload must be sent. Control of scoreboards (up to 8) is implicit based on the (X, Y) address of the generated thread and the scoreboard control state.

The command can be used only in Generic modes.

When **Use Scoreboard** field is set, the (X, Y) address and the Color field of the generated thread are used in the hardware scoreboard and the thread dependencies are set by states from the MEDIA_VFE_STATE command.

One or more threads may be generated by this command. This command does not support indirect object load. When inline data is present, it is repeated for all threads it generates. Unlike CURBE, which requires pipeline flush for change, continued change of this kind of 'global' (in the sense of shared by multiple threads from this command) data is supported when MEDIA_OBJECT_WALKER commands are issued without a pipeline flush in between.

MEDIA_POOL_STATE

SubslicePool



Media State and Primitive Command Workarounds

Media State and Primitive Commands have some subtle programming restrictions and workarounds, as listed below.

Programming Note
When a media walker/media object group id with either a local or global barrier is used, then a stalling PIPE_CONTROL is required before the next MEDIA_VFE_STATE (instead of the usual MEDIA_STATE_FLUSH).
Global barriers should not be used at the same time as linked barriers. A PIPE_CONTROL with CS Stall should be placed between work that uses linked barriers and work that uses global barriers. Global and local barriers can be used together only if the Thread Dispatch Selection Policy in MEDIA_VFE_STATE is set to Legacy.

L3 Cache and URB

This is the volume for BXT L3/URB/SLM. Much of the content is identical to Gen8, with important changes to enhance performance.

Overview

The overall organization of the L3 and theory of operation have not changed. It retains all the performance enhancements from previous generations with some additional improvements.

To provide the bandwidth needed L3 is still organized into independent banks which can be accessed concurrently. Clocking remains 2X in the arrays to balance bandwidth with incoming requests. The L3\$ and URB data for all L3 banks are shared as a contiguous memory space for all products regardless of how many banks or slices.

- Each Bank 192KB in size.
- Each logical bank consists of:
 - Data Array
 - Tag Array
 - LRU Array (implements a Pseudo Least Recently Used algorithm)
 - State Array
 - SuperQ Buffer
 - Atomic Processing Units
- The rest of the support logic around L3 consists of:
 - SuperQ (main scheduler).
 - Ingress/Egress queues to L3/SQ (L3 arbiter).
 - CAM structures to maintain coherency.
 - Crossbars for data routing.
- Use of 2x/1x clocking.
- L3 can operate concurrently in GFX and IA coherent domain.
- A portion of L3 can be allocated as highly banked memory and/or unified buffer (URB).



L3 Bank Configuration

Each L3 bank is identical as described below. In products where there is only a single L3 bank supported, the bank will be different to support a larger data array. The Multi-bank describes the L3 Bank configuration for all other products.

Multi-Bank: 192KB data-array and 96 logical ways:

- Up to 64 ways, up to 128KB, tagged for L3\$, remaining is treated as memory.
- 64KB or 96KB allocated for URB (does not use tag).
- Shared local memory (SLM) capable (64KB)
 - Uses Highly-banked memory to allow up to 16 32-bit accesses in parallel within a 64KB space per sub-slice.
 - Highly-banked memory formed from 16x4KB arrays

Single-Bank: 320KB data-array and 160 logical ways:

- Up to 96 ways, up to 192KB, tagged for L3\$, remaining is treated as memory.
- 64KB or 128KB allocated for URB (does not use tag).
- Shared local memory (SLM) capable (64KB)
 - Uses Highly-banked memory to allow up to 16 32-bit accesses in parallel within a 64KB space per sub-slice.
 - Highly-banked memory formed from 16x4KB arrays.

All Bank Implementations:

- 64B Cacheline.
- Interface 64B to SQDB for the fill/write path, 64B Read/Evict path to SQDB. Additional 64B read and 64B write capability for SLM.
- Data protection via ECC.
- TAG/LRU/STATE (using gen-ram via RLS flows):
 - 39/48-bit addressing support in TAG.
 - 6-bit state (2-bits of MESI, 2-bits of Surface type, 1 bit Phys/Virtual, 1-bit Global/Local).
 - Intel pseudo-LRU implementation for selecting the line to be replaced or 1b LRU (added for Gen9).

Bandwidth and Throughput Capability

L3 Blocks Overview

L3 is formed via some number of logical banks that are identical to each other. The major blocks in each logical bank are:

- L3 Cache Arrays & Controller



- Super Q and related data buffer
- Ingress queues and related CAMs with arbitration
- Atomics Block/SLM pipeline & crossbar for data routing

Our vision is to build a compute scalable cache where with each additional compute both the size and bandwidth are scaled while maintaining the functional single cache concept. Each added bank becomes an additional cache rather than an independent content. The concept is to be able to keep a single copy of a line and service all requesters via distributing their accesses over many physical caches.

Size of L3 Bank and Allocations

Multi-Bank Allocation Options

The table below shows the size of the L3 bank and the ranges of allocation for L3\$, URB, and SLM. Below is a table of all validated configurations supported.

No Shared Local Memory Mode (KBytes)						
			L3			
Config	SLM	URB	Rest	DC	RO(I/S/C/T)	Sum
0	0	96	96	0	0	192
1	0	96	0	32	64	192
2	0	64	0	128	0	192
3	0	64	0	0	128	192
4	0	64	128	0	0	192
Shared Local Memory Mode (KBytes)						
			L3			
Config	SLM	URB	Rest	DC	RO(I/S/C/T)	Sum
1	64	32	96	0	0	192
2	64	32	0	32	64	192
3	64	32	0	64	32	192
4	64	16	112	0	0	192

Essentially, the L3 block can either support SLM or not. When SLM is supported, each slice provides 64KB of its 192KB data array for SLM. When SLM is not supported, the 64KB is allocated to URB or split equally between URB and L3\$.

The number of L3 Banks will vary for different products and SKUs. The number of banks supported for each product is defined in the Configurations section of the BSPEC. The total amount of L3\$, URB, and SLM supported by a product can be calculated by multiplying the number of banks by the values in the above tables.



Single-Bank Allocation Options

The table below shows the size of the L3 bank and the ranges of allocation for L3\$, URB, and SLM in the case of a product with a single bank (e.g. BXT:*:C).

No Shared Local Memory Mode (KBytes)						
			L3			
Config	SLM	URB	Rest	DC	RO(I/S/C/T)	Sum
0	0	128	192	0	0	320
1	0	128	0	32	160	320
2	0	128	0	128	64	320
Shared Local Memory Mode (KBytes)						
			L3			
Config	SLM	URB	Rest	DC	RO(I/S/C/T)	Sum
1	64	64	192	0	0	320
2	64	64	0	160	32	320
3	64	64	0	64	128	320

The table above describes the allocation of the data array for a single-bank BXT:*:C.

Shared Local Memory

Shared local memory (SLM, also known as highly-banked memory) is a portion of L3 which will be dedicated to EUs as a local memory when enabled.

SLM Behavior and Software Usage

For Gen9LP (BXT derivatives), the SLM in an L3 is not dedicated for use by a single sub-slice. Because there may be more sub-slices than there are L3 banks, the SLM is shared across all EUs in all sub-slices within a slice. Each SLM bank is shared by some sub-set of the EUs as determined in the HDC by software. See the volume on HDC for more details on how SLM is allocated to different EUs/threads.

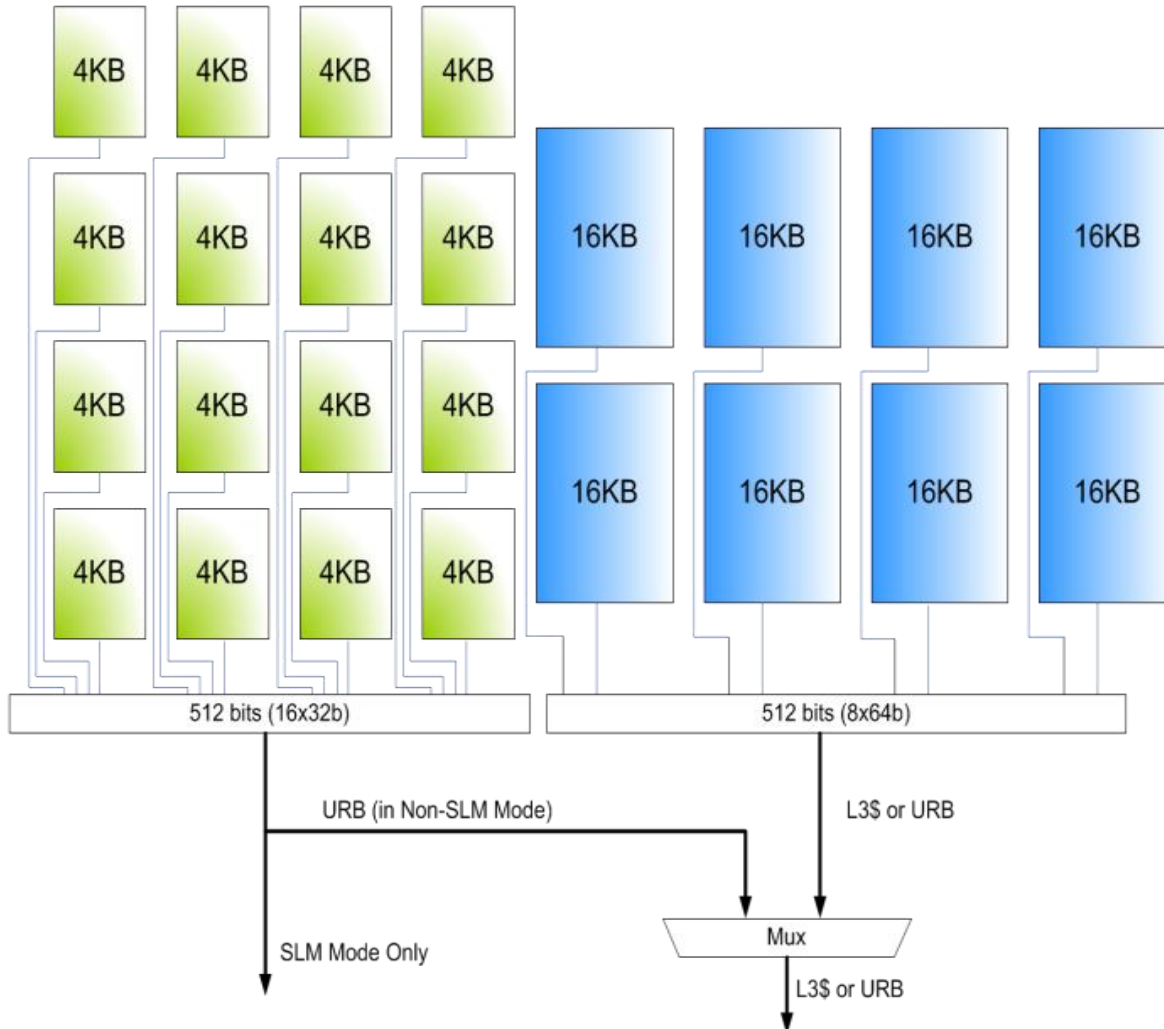
SLM is enabled statically by the application. When enabled, it uses a fixed 64K block in each L3 Bank. When SLM is enabled, URB will not use this 64K block of memory. URB accesses will automatically be moved to a different location in the L3 bank.

SLM is implemented to allow for highly parallel applications. 16 DWord-accesses (all read or all write) can be done simultaneously to different locations in the 64K space. Atomic operations as described in the Atomic Operation section of this volume can be performed on the output of the SLM and written back in one operation.

SLM Bank Hardware Implementation

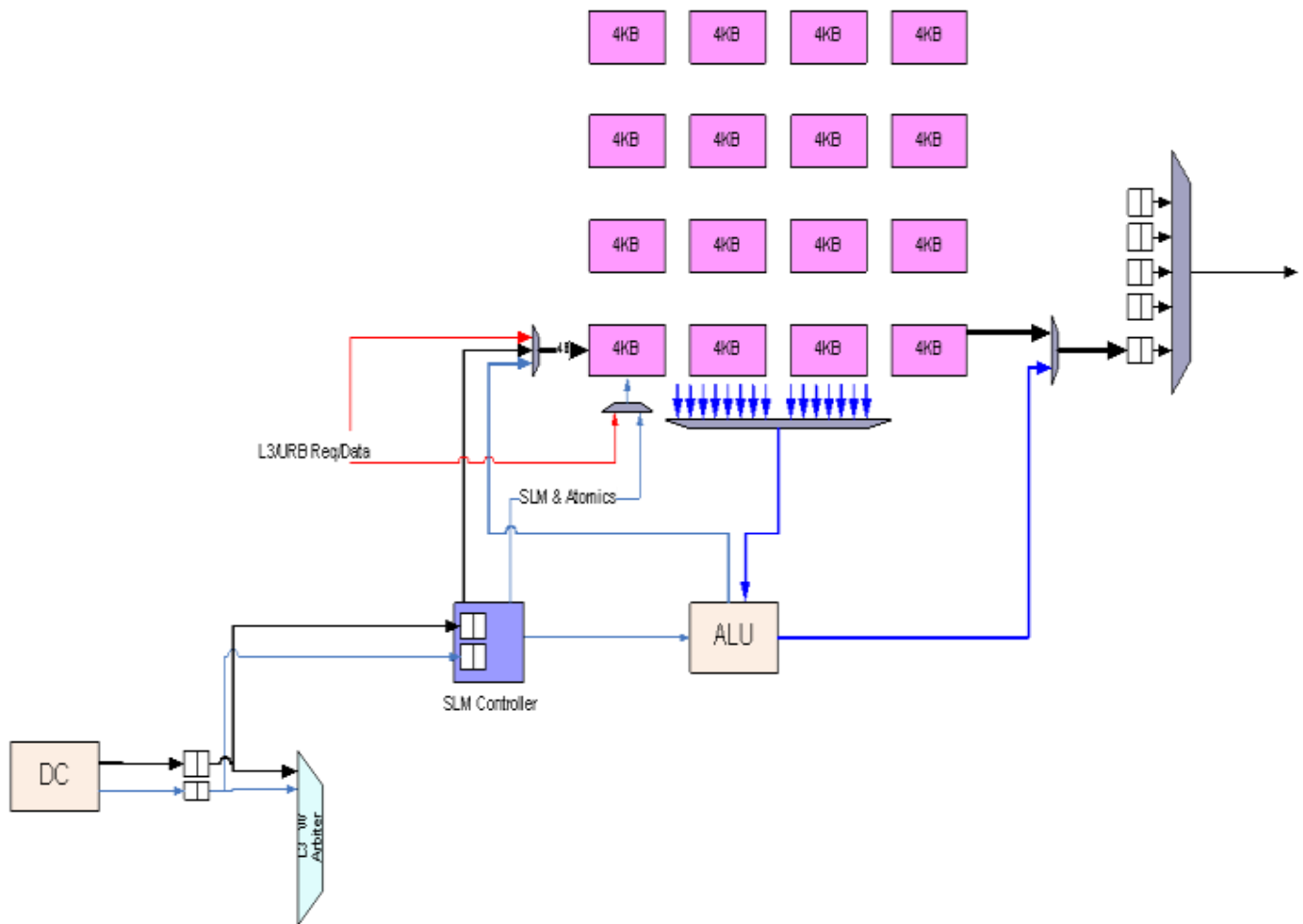
The accesses are only possible through data cluster with the destination flag set as SLM. To support a highly banked design, each of the L3 banks are structured to have 16x4KB portion which could be accessed independently per clock. This part of the L3 can support 16 DW size accesses (per SLM) in a

given clock cycle. Each bank's SLM is dedicated to a single sub-slice. The diagram below shows the organization of data for a 192KB L3 Bank.



These 16 banks can either be used as URB or used as shared local memory with parallel accesses to all banks. The choice of enabling SLM mode is done through MMIO programming

Bits	Access	Default Value	Description
0	RW/C	0	Enable Shared Local Memory: When set, it enables the use of 2 banks of L3 as shared local memory which allows 64KB of L3 to be banked as 16x4KB and allows independent accesses to all banks within the same clock cycle. Note: This mode can only be enabled once L3 content is completely flushed.





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EU Overview

The GEN instruction set is a general-purpose data-parallel instruction set optimized for graphics and media computations. Support for 3D graphics API (Application Programming Interface) Shader instructions is mostly native, meaning that GEN efficiently executes Shader programs. Depending on Shader program operation modes (for example, a Vertex Shader may be executed on a base of a vertex pair, while a Pixel Shader may be executed on a base of a 16-pixel group), translation from 3D graphics API Shader instruction streams into GEN native instructions may be required. In addition, there are many specific capabilities that accelerate media applications. The following feature list summarizes the GEN instruction set architecture:

- SIMD (single instruction multiple data) instructions. The maximum number of data elements per instruction depends on the data type.
- SIMD parallel arithmetic, vector arithmetic, logical, and SIMD control/branch instructions.
- Instruction level variable-width SIMD execution.
- Conditional SIMD execution via destination mask, predication, and execution mask.
- Instruction compaction.
- An instruction may be executed in multiple cycles over a SIMD execution pipeline.
- Most GEN instructions have three operands. Some instructions have additional implied source or destination operands. Some instructions have explicit dual destinations.
- Region-based register addressing.
- Direct or indirect (indexed) register addressing.
- Scalar or vector immediate source operand.
- Higher precision accumulator registers are architecturally visible.
- Self-modifying code is not allowed (instruction streams, including instruction caches, are read-only).

Accumulator Registers

Accumulator Registers Summary

Attribute	Value
ARF Register Type Encoding (RegNum[7:4]):	0010b
Number of Registers:	10
Default Value:	None
Normal Access:	RW

Accumulator registers can be accessed either as explicit or implied source and/or destination registers. To a programmer, each accumulator register may contain either 8 DWords or 16 Words of data elements. However, as described in the Implementation Precision Restriction notes below, each data element may have higher precision with added guard bits not indicated by the numeric data type.



Accumulator capabilities vary by data type, not just data size, as described in the Accumulator Channel Precision table below. For example, D and F are both 32-bit data types, but differ in accumulator support.

See the Accumulator Restrictions section for information about additional general accumulator restrictions and also accumulator restrictions for specific instructions.

Accumulator Registers
There are 10 accumulator registers. The accumulator registers are of two types.

Register and Subregister Numbers for Accumulator Registers

RegNum[3:0]	SubRegNum[4]	SubRegNum[3:0]
0000b-1001b = acc0-acc9 All other encodings are reserved.	0 : Lower half 1 : Upper half	Reserved: MBZ

- Accumulators are updated implicitly only if the AccWrCtrl bit is set in the instruction. The Accumulator Disable bit in control register cr0.0 allows software to disable the use of AccWrCtrl for implicit accumulator updates. The write enable in word granularity for the instruction is used to update the accumulator. Data in disabled channels is not updated.
- When an accumulator register is an implicit source or destination operand, hardware always uses acc0 by default and also uses acc1 if the execution size exceeds the number of elements in acc0. When implicit access to acc1 is required, QtrCtrl is used. Note that QtrCtrl can be used only if acc1 is accessible for a given data type. If acc1 is not accessible for a given data type, QtrCtrl defaults to acc0.

Description
acc0 and acc1 are supported for half-precision (HF, Half Float) and single-precision (F, Float). Use QtrCtrl of Q2 or Q4 to access acc1 for Float. use QtrCtrl of H2 to access acc1 for Half Float.

Examples:

```
// Updates acc0 and acc1 because it is SIMD16:
add (16) r10:f r11:f r12:f {AccWrEn}
// Updates acc0 because it is SIMD8:
add (8) r10:f r11:f r12:f {AccWrEn}
// Updates acc1. Implicit access to acc1 using QtrCtrl:
add (8) r10:f r11:f r12:f {AccWrEn, Q2}
// Updates acc1 for Half Floats using QtrCtrl:
add (16) r10:hf r11:hf r12:hf {AccWrEn, H2}
```

- It is illegal to specify different accumulator registers for source and destination operands in an instruction (e.g. "*add (8) acc1:f acc0:f*"). The result of such an instruction is unpredictable.

Limits on SIMD16 Float Operations
Accumulator registers may be accessed explicitly as src0 operands only.

- Swizzling is not allowed when an accumulator is used as an implicit source or an explicit source in an instruction.



- Reading accumulator content with a datatype different from the previous write will result in undeterministic values.
- Word datatype write to accumulator is not allowed when destination is odd offset strided by 2.
- For any DWord operation, including DWord multiply, accumulator can store up to 8 channels of data, with only acc0 supported.
- When an accumulator register is an explicit destination, it follows the rules of a destination register. If an accumulator is an explicit source operand, its register region must match that of the destination register with the exception(s) described below.

Exceptions
Half floats can be written to either the lower or the upper word of the accumulator. However, this is not supported for integer word operations.
acc1 must not be used with half-float and word datatypes

Implementation Precision Restriction: As there are only 64 bits per channel in DWord mode (D and UD), it is sufficient to store the multiplication result of two DWord operands as long as the post source modified sources are still within 32 bits. If any one source is type UD and is negated, the negated result becomes 33 bits. The DWord multiplication result is then 65 bits, bigger than the storage capacity of accumulators. Consequently, the results are unpredictable.

Implementation Precision Restriction: As there are only 33 bits per channel in Word mode (W and UW), it is sufficient to store the multiplication result of two Word operands with and without source modifier as the result is up to 33 bits. Integers are stored in accumulator in 2's complement form with bit 32 as the sign bit. As there is no guard bit left, the accumulator can only be sourced once before running into a risk of overflowing. When overflow occurs, only modular addition can generate a correct result. But in this case, conditional flags may be incorrect. When saturation is used, the output is unpredictable. This is also true for other operations that may result in more than 33 bits of data. For example, adding UD (FFFFFFFFh) with D (FFFFFFFFh) results in 1FFFFFFFFh. The sign bit is now at bit 34 and is lost when stored in the accumulator. When it is read out later from the accumulator, it becomes a negative number as bit 32 now becomes the sign bit.

Accumulator Channel Precision

Data Type	Accumulator Number	Number of Channels	Bits Per Channel	Description
DF	acc0	4	64	When accumulator is used for Double Float, it has the exact same precision as any GRF register.
F	acc0/acc1	8	32	When accumulator is used for Float, it has the exact same precision as any GRF register.
Q	N/A	N/A	N/A	Not supported data type.
D (UD)	acc0	8	33/64	When the internal execution data type is doubleword integer, each accumulator register contains 8 channels of (extended) doubleword



Data Type	Accumulator Number	Number of Channels	Bits Per Channel	Description
				integer values. The data are always stored in accumulator in 2's complement form with 64 bits total regardless of the source data type. This is sufficient to construct the 64-bit D or UD multiplication results using an instruction macro sequence consisting of <i>mul</i> , <i>mach</i> , and <i>shr</i> (or <i>mov</i>).
W (UW)	acc0	16	33	When the internal execution data type is word integer, each accumulator register contains 16 channels of (extended) word integer values. The data are always stored in accumulator in 2's complement form with 33 bits total. This supports single instruction multiplication of two word sources in W and/or UW format.
B (UB)	N/A	N/A	N/A	Not supported data type.

Accumulators

Accumulators acc2-acc9

These are accumulator registers defined for a special purpose. They are used to emulate IEEE-compliant *fdv* and *sqrt* macro operations. The access is different from *acc0* and *acc1*. Each of these accumulator registers are defined as 256-bit registers having 8 DWords. These may be accessed explicitly or implicitly.

- These registers may be accessed explicitly only by a *mov* operation, with no source modifiers, condition modifiers, or saturation. When accessed explicitly, the datatype must be D. On reads, the low 2 bits of each DWord are valid data. The other bits are undefined. On writes, the low two bits are updated and other bits are dropped.

Example:

```
// Move 256 bits from acc2 to r10. Just low two bits of each DWord are valid:
mov (8) r10:ud acc2:ud

// Move 256 bits from r10 to acc2. Just low two bits of each DWord are updated:
mov (8) acc2:ud r10:ud
```

- These registers are accessed implicitly by three opcodes defined for the macro operations. **Note:** These macro operations are defined under the *math* opcode section. The macro descriptions also define the restrictive implicit uses of these registers.

Description

Implicit access across accumulator registers is required for each source operand for these macro instructions. These opcodes are accessed in Align16 mode only. The Channel Select bits in the instruction are used to implicitly address

Description	
the different accumulators for each source. Similarly the Channel Enable bits are used to implicitly address the accumulators for destination. The noacc value is specified when no write to accumulator is required; think of it as a null.	
Encoding	Accumulator Register
00000001b	acc3
00000010b	acc4
00000011b	acc5
00000100b	acc6
00000101b	acc7
00000110b	acc8
00000111b	acc9
00001000b	noacc

Register Region Restrictions

A register region is described as *packed* if its elements are adjacent in memory, with no intervening space, no overlap, and no replicated values. If there is more than one element in a row, elements must be adjacent. If there is more than one row, rows must be adjacent. When two registers are used, the registers must be adjacent and both must exist.

The following register region rules apply to the GEN implementation.

1. General Restrictions Based on Operand Types

There are these general restrictions based on operand types:

1. Where n is the largest element size in bytes for any source or destination operand type, $ExecSize * n$ must be ≤ 64 .
2. When the Execution Data Type is wider than the destination data type, the destination must be aligned as required by the wider execution data type and specify a *HorzStride* equal to the ratio in sizes of the two data types. For example, a *mov* with a D source and B destination must use a 4-byte aligned destination and a *Dst.HorzStride* of 4.

2. General Restrictions on Regioning Parameters

The mapping of data elements within the region of a source operand is in row-major order and is determined by the region description of the source operand, the destination operand, and the *ExecSize*, with these restrictions:

1. *ExecSize* must be greater than or equal to *Width*.
2. If $ExecSize = Width$ and $HorzStride \neq 0$, *VertStride* must be set to $Width * HorzStride$.
3. If $ExecSize = Width$ and $HorzStride = 0$, there is no restriction on *VertStride*.
4. If $Width = 1$, *HorzStride* must be 0 regardless of the values of *ExecSize* and *VertStride*.
5. If $ExecSize = Width = 1$, both *VertStride* and *HorzStride* must be 0.

6. If *VertStride* = *HorzStride* = 0, *Width* must be 1 regardless of the value of *ExecSize*.
 7. *Dst.HorzStride* must not be 0.
 8. *VertStride* must be used to cross GRF register boundaries. This rule implies that elements within a '*Width*' cannot cross GRF boundaries.
3. **Region Alignment Rules for Direct Register Addressing**
1. In Direct Addressing mode, a source cannot span more than 2 adjacent GRF registers.
 2. A destination cannot span more than 2 adjacent GRF registers.
 3. When a source or destination spans two registers, there are restrictions that vary by project, described in the following table. If you are viewing a version of the BSpec limited to other particular projects, the table may appear with no data rows.
4. **Special Cases for Byte Operations**
1. When the destination type is byte (UB or B) only a 'raw move' using the *mov* instruction supports a packed byte destination register region: *Dst.HorzStride* = 1 and *Dst.DstType* = (UB or B). This packed byte destination register region is not allowed for any other instructions, including a 'raw move' using the *sel* instruction, because the *sel* instruction is based on Word or DWord wide execution channels.
 2. There is a relaxed alignment rule for byte destinations. When the destination type is byte (UB or B), destination data types can be aligned to either the lowest byte or the second lowest byte of the execution channel. For example, if one of the source operands is in word mode (a signed or unsigned word integer), the execution data type will be signed word integer. In this case the destination data bytes can be either all in the even byte locations or all in the odd byte locations.

This rule has two implications illustrated by this example:

```
// Example:
mov (8) r10.0<2>:b r11.0<8;8,1>:w
mov (8) r10.1<2>:b r11.0<8;8,1>:w

// Dst.HorzStride must be 2 in the above example so that the destination
// subregisters are aligned to the execution data type, which is :w.
// However, the offset may be .0 or .1.
// This special handling applies to byte destinations ONLY.
```

5. Special Cases for Word Operations

There are some special cases for word operations for specific projects, described in the following table. If you are viewing a version of the BSpec limited to other particular projects, the table may not show and there are no special cases in this category.

There is a relaxed alignment rule for word destinations. When the destination type is word (UW, W, HF), destination data types can be aligned to either the lowest word or the second lowest word of the execution channel. This means the destination data words can be either all in the even word locations or all in the odd word locations.

```
// Example:
add (8) r10.0<2>:hf r11.0<8;8,1>:f r12.0<8;8,1>:hf
```



```
add (8) r10.1<2>:hf r11.0<8;8,1>:f r12.0<8;8,1>:hf
```

// Note: The destination offset may be .0 or .1 although the destination subregister
// is required to be aligned to execution datatype.

6. Special Requirements for Handling Double Precision Data Types

There are special requirements for handling double precision data types that vary by project, described in the following table. If you are viewing a version of the BSpec limited to other particular projects, the table may appear with no data rows.

Special Requirements for Handling Double Precision Data Types

Requirement
When source or destination datatype is 64b or operation is integer DWord multiply, regioning in Align1 must follow these rules: - Source and Destination horizontal stride must be aligned to the same qword. Example: <pre>// mov (4) r10.0:df r11.0<16;8,2>:f // Source stride must be 2 since datatype is smaller. // mov (4) r10.0<2>:f r11.0<4;4,1>:df // Destination stride must be 2 since datatype is smaller. // mul (4) r10.0<2>:d r11.0<8;4,2>:d r12.0<8;4,2>:d // Source and Destination stride must be 2 since the execution type is Qword.</pre> - Regioning must ensure $\text{Src.Vstride} = \text{Src.Width} * \text{Src.Hstride}$. - Source and Destination offset must be the same, except the case of scalar source.
When source or destination datatype is 64b or operation is integer DWord multiply, indirect addressing must not be used.
ARF registers must never be used with 64b datatype or when operation is integer DWord multiply.
When source or destination datatype is 64b or operation is integer DWord multiply, DepCtrl must not be used.

7. Special Requirements for Handling Mixed Mode Float Operations

There are some special requirements for handling mixed mode float operations for specific projects, described in the following table. If you are viewing a version of the BSpec limited to other particular projects, the table may appear with no data rows.

Requirement
In Align16 mode, when half float and float data types are mixed between source operands OR between source and destination operands, the register content are assumed to be packed. In such cases the execution size reflects the number of float elements. Since a stride of 1 is assumed, source is selected in packed form and 16 bit packed data is updated on the destination operand, if the datatype is half-float.
For Align16 mixed mode, both input and output packed f16 data must be oword aligned, no oword crossing in packed f16.



Requirement
Examples: <pre> Case (a) mad (8) r10.0.xy:hf r11.0.xxxx:f r12.xyzw:hf r13.yyyy:hf // The 16b of each word (r12.0, r12.1, r12.2, r12.3.. and so on) forms the source operand. // r13.1 and r13.5 is replicated for source operand. // The lower 16b of a Dword is updated for destination. With channel enables .xy , r10.0, r10.1, r10.4 and r10.5 are updated. Case (b) mad (8) r10.0.xy:f r11.0.xxxx:f r12.xyzw:hf r13.yyyy:hf // The example is similar to Case(a), except that entire DWord is updated on the destination. </pre>
In Align16 mode, replicate is supported and is coissueable. <pre> mad(8) r20.xyzw:hf r3.0.r:f r6.0.xyzw:hf r6.0.xyzw:hf {Q1} </pre>
No SIMD16 in mixed mode when destination is packed f16 for both Align1 and Align16. <pre> mad(8) r3.xyzw:hf r4.xyzw:f r6.xyzw:hf r7.xyzw:hf add(8) r20.0<1>:hf r3<8;8,1>:f r6.0<8;8,1>:hf {Q1} </pre>
No accumulator read access for Align16 mixed float.
When source is float or half float from accumulator register and destination is half float with a stride of 1, the source must register aligned. i.e., source must have offset zero.
No swizzle is allowed when an accumulator is used as an implicit source or an explicit source in an instruction. i.e. when destination is half float with an implicit accumulator source, destination stride needs to be 2. <pre> mac(8) r3<2>:hf r4.0<8;8,1>:f r6.0<8;4,2>:hf mov(8) r3<1>:f acc0.0<8;4,2>:hf </pre>
In Align16, vertical stride can never be zero for f16 <pre> add(8) r3.xyzw:hf r4.0<4>xyzw:f r6.0<0>.xyzw:hf </pre>
Math operations for mixed mode: - In Align16, only packed format is supported <pre> math(8) r3.xyzw:hf r4.0.<4>xyzw:f r6.0<0>.xyzw:hf 0x09 </pre> - In Align1, f16 inputs need to be strided <pre> math(8) r3<1>:hf r4.0<8;8,1>:f r6.0<8;4,2>:hf </pre>

Requirement

In Align1, destination stride can be smaller than execution type. When destination is stride of 1, 16 bit packed data is updated on the destination. However, output packed f16 data must be oword aligned, no oword crossing in packed f16.

```
add(8) r3<1>:hf r4.0<8;8,1>:f r6.0<8;4,2>:hf
```

8. Regioning Rules for Register Indirect Addressing

Regioning rules for register indirect addressing vary for specific projects, described in the following table. If you are viewing a version of the BSpec limited to other particular projects, the table may appear with no data rows.

Rules

1. When the execution size and destination regioning parameters require two adjacent registers, these registers are accessed using one index register ONLY.

```
// Example:
mov (16) r[a0.0]:f r10:f
// The above instruction behaves the same as the following two instructions:
mov (8) r[a0.0]:f r10:f
mov (8) r[a0.0, 8*4]:f r11:f
```

2. When the destination requires two registers and the sources are 1x1 indirect mode, the sources must be assembled from two GRF registers accessed by a single index register. The data for each destination GRF register is entirely derived from one source register. This is ensured by appropriate use of regioning parameters. The exception to this is the use of indirect scalar sources, where the same element is used across the execution size.

```
// Example:
// Case (a)
add (16) r[a0.0]:f r[a0.2]:f r[a0.4]:f
// The above instruction behaves the same as the following two instructions:
add (8) r[a0.0]:f r[a0.2]:f r[a0.4]:f
add (8) r[a0.0, 8*4]:f r[a0.2, 8*4]:f r[a0.4, 8*4]:f
// Note that the immediate for the second instruction is based on regioning.
// In this case, it is 8 DWs.
```

```
// Case (b)
add (16) r[a0.0]:ud r[a0.2]<4;8,1>:w r10<8;8,1>:ud
// The above instruction behaves the same as the following two instructions:
add (8) r[a0.0]:f r[a0.2]<4;8,1>:w r10<8;8,1>:ud
add (8) r[a0.0, 8*4]:f r[a0.2, 4*2]<4;8,1>:w r11<8;8,1>:ud
// Note that the immediate for the second instruction is based on regioning.
// VertStride of 4 with data type of word.
```

```
// Case (c):
add (16) r[a0.0]:f r[a0.2]:f r[a0.4]<0;1,0>:f
// The above instruction behaves the same as the following two instructions:
add (8) r[a0.0]:f r[a0.2]:f r[a0.4]<0;1,0>:f
add (8) r[a0.0, 8*4]:f r[a0.2, 8*4]:f r[a0.4]<0;1,0>:f
// Note that the src1 indirect address does not change.
```

3. Indirect addressing on src1 must be a 1x1 indexed region mode.

Rules
4. When a Vx1 or a VxH addressing mode is used on src0, the destination may use one or two registers. <pre>// Example: // Case (a) add (16) r[a0.0]<1>:d r[a0.0]<4,1>:ud r16.0<8;8,1>:ud // The above instruction behaves the same as the following two instructions: add (8) r[a0.0]<1>:d r[a0.0]<4,1>:ud r16.0<8;8,1>:ud add (8) r[a0.0, 8*4]<1>:d r[a0.2]<4,1>:ud r17.0<8;8,1>:ud // Since the pointer (index register) is incremented every 4 elements // (width), the second instruction moves from a0.0 to a0.2. // Case (b) add (16) r10.0<2>:uw r[a0.0, 0]<1,0>:uw r16.0<8;8,1>:uw // The above instruction behaves the same as the following two instructions: add (8) r10.0<2>:uw r[a0.0, 0]<1,0>:uw r16.0<8;8,1>:uw add (8) r11.0<2>:uw r[a0.8, 0]<1,0>:uw r17.0<8;8,1>:uw // Since the pointer (index register) is incremented every 1 element // (width), the second instruction moves from a0.0 to a0.8.</pre> 5. Indirect addressing on the destination must be a 1x1 indexed region mode.
Execution size of 32 is NOT supported in Vx1 or VxH modes.

1. Special Restrictions

There are some special restrictions on register region access for specific projects, described in the following table. If you are viewing a version of the BSpec limited to other particular projects, the table may appear with no data rows.

Restriction
All flow control (branching) instructions must use the Align1 access mode.
When using Align16 mode for conversion of data elements of different sizes, both source and destination must be one register each.
In Align16 mode, each destination register gets all data from one source register. This means, the data for one destination register is never scattered across two source registers. <pre>// Example: // Allowed - all sources are contained within one register. mul (8) r10.0:f r11.0:f r12.4<0>:f // NOT Allowed - src1 (r14) is scattered across two registers. mad (8) r10.0:f r12.0<0>:f r14.4:f r16.0:f</pre>

**Restriction**

Conversion between Integer and HF (Half Float) must be DWord-aligned and strided by a DWord on the destination.

```
// Example:  
add (8) r10.0<2>:hf r11.0<8;8,1>:w r12.0<8;8,1>:w  
// Destination stride must be 2.  
mov (8) r10.0<2>:w r11.0<8;8,1>:hf  
// Destination stride must be 2.
```

The src, dst overlapping behavior with the second half src and the first half destination to the same register must not be used with any compressed instruction.

In mid-thread pre-emptible contexts, if a compressed instruction uses vx1 or vxh addressing modes, then the second half of the compressed instruction must use more than one index register to access source0.



Intel® Open Source HD Graphics

Programmer's Reference Manual

For the 2016 Intel Atom™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Apollo Lake" Platform (Broxton Graphics)

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Display Audio Codec Verbs

Programming

Programming of the codec is performed by "verbs" as described in the HD Audio specification. These verbs travel over the internal HD Audio link at a rate of 1 verb per frame. A verb can either come from the CORB, with responses using the RIRB, or using an immediate command and response mechanism (ICR). Device 2 contains its own copy of an ICR mechanism as a back-door into the audio codec.

Node ID 00h Root Node Verbs

The root node only contains a single verb - the "Get Parameters" verb at F00h.

F00h - Get Parameters

Parameter	Symbol	Register Name
00h	PARAM_VID	Vendor ID
02h	PARAM_RID	Revision ID
04h	PARAM_SNC	Subordinate Node Count

Parameter 00h: VID - Vendor ID

Bit	Reset	Description
31:16	8086h	Vendor ID (VID): Indicates the 16-bit Vendor ID values used to identify the codec to the PnP subsystem.
15:00	2809h	Device ID (DID): Indicates the 16-bit Device ID values used to identify the codec to the PnP subsystem. It is 280Ah for BXT
15:00	2809	Device ID (DID): Indicates the 16-bit Device ID values used to identify the codec to the PnP subsystem.

Parameter 02h: RID - Revision ID

Bit	Reset	Description
31:24	0	<i>Reserved</i>
23:20	1h	Major Revision (MJR): Indicates the major revision number (left of the decimal) of the High Definition Audio Specification to which the codec is fully compliant.
19:16	0h	Minor Revision (MNR): Indicates the minor revision number (right of the decimal) or "dot number" of the High Definition Audio Specification to which the codec is fully compliant.
15:08	00h	Revision ID (RID): Indicates the vendor's revision number for this given Device ID.
07:00	00h	Stepping ID (SID): Indicates optional vendor stepping number within the revision.



Parameter 04h: PARAM_SNC - Subordinate Node Count

Bit	Reset	Description
31:24	0	Reserved
23:16	0h	Starting Node Number (SNN): Indicates the first sub-node's ID is 01h.
15:08	00h	Reserved
07:00	01h	Total Number of Nodes (TNN): Indicates one sub-node

North Display Engine Registers

MIPI

MIPI Configurations

Configuration	Supported
Isolated MIPI-A (single display using single link)	Yes
Isolated MIPI-C	No
Isolated MIPI-A & Isolated MIPI-C (dual independent display using dual MIPI)	No
Dual Link Mode with MIPI-A as primary (single display using dual links)	Yes
Dual Link Mode with MIPI-C as primary	No

MIPI DSI Registers

Note
These registers must all be written only as full 32 bit Dwords. Byte or word writes are not supported.
MIPI DSI clocks MUST be running in order to read any of the MIPI registers.

Dual Link Programming	
Dual Link Operation	Bit/Register
MIPI dual link enable	Bit 0 of MIPI_PORT_CTL
MIPI dual link mode	Bit 26 of MIPI_PORT_CTL
Z-inversion count	Bit [13:10] of MIPI_CTRL

Address	Name
6B000h	MIPIA_DEVICE_READY_REG
6B004h	MIPIA_INTR_STAT_REG
6B008h	MIPIA_INTR_EN_REG

Address	Name
6B00Ch	MIPIA_DSI_FUNC_PRG_REG
6B010h	MIPIA_HS_TX_TIMEOUT_REG
6B014h	MIPIA_LP_RX_TIMEOUT_REG
6B018h	MIPIA_TURN_AROUND_TIMEOUT_REG
6B01Ch	MIPIA_DEVICE_RESET_TIMER
6B020h	MIPIA_DPI_RESOLUTION_REG
6B024h	MIPIA_DBI_FIFO_THRTL_REG
6B028h	MIPIA_HORIZ_SYNC_PADDING_COUNT
6B02Ch	MIPIA_HORIZ_BACK_PORCH_COUNT
6B030h	MIPIA_HORIZ_FRONT_PORCH_COUNT
6B034h	MIPIA_HORIZ_ACTIVE_AREA_COUNT
6B038h	MIPIA_VERT_SYNC_PADDING_COUNT
6B03Ch	MIPIA_VERT_BACK_PORCH_COUNT
6B040h	MIPIA_VERT_FRONT_PORCH_COUNT
6B044h	MIPIA_HIGH_LOW_SWITCH_COUNT
6B048h	MIPIA_DPI_CTRL_REG
6B04Ch	MIPIA_DPI_DATA_REGISTER
6B050h	MIPIA_INIT_COUNT_REGISTER
6B054h	MIPIA_MAX_RETURN_PKT_SIZE_REGISTER
6B058h	MIPIA_VIDEO_MODE_FORMAT_REGISTER
6B05Ch	MIPIA_EOT_DISABLE_REGISTER
6B060h	MIPIA_LP_BYTECLK_REGISTER



Address	Name
6B064h	MIPIA_LP_GEN_DATA_REGISTER
6B068h	MIPIA_HS_GEN_DATA_REGISTER
6B06Ch	MIPIA_LP_GEN_CTRL_REGISTER
6B070h	MIPIA_HS_GEN_CTRL_REGISTER
6B074h	MIPIA_GEN_FIFO_STAT_REGISTER
6B078h	MIPIA_HS_LS_DBI_ENABLE_REG
6B07Ch	MIPI_HS_READ_TRANSFER_COUNT
6B080h	MIPIA_DPHY_PARAM_REG
6B084h	MIPIA_DBI_BW_CTRL_REG
6B088h	MIPIA_CLK_LANE_SWITCHING_TIME_CNT
6B08Ch	MIPIA_STOP_STATE_STALL
6B090h	MIPIA_INTR_STAT_REG_1
6B094h	MIPIA_INTR_EN_REG_1
6B098h	MIPIA_CLK_LANE_TIMING
6B09Ch	MIPIA_PLL_LOCK_COUNT
6B0A0h	MIPIA_DATA_LANE_POLARITY
6B0A4h	MIPIA_TLPX_TIME_COUNT
6B0C0h	MIPIA_PORT_CTRL
6B0C4h	MIPIA_STATUS
6B0C8h	MIPIA_AUTOPWG
6B0CCh	MIPIA_WR_DATA 0
6B0D0h	MIPIA_WR_DATA 1

Address	Name
6B0D4h	MIPIA_WR_DATA 2
6B0D8h	MIPIA_WR_DATA 3
6B0DCh	MIPIA_WR_DATA 4
6B0E0h	MIPIA_WR_DATA 5
6B0E4h	MIPIA_WR_DATA 6
6B0E8h	MIPIA_WR_DATA 7
6B0ECh	MIPIA_WR_COMMAND
6B0F0h	MIPIA_WR_DATA_CTRL
6B0F4h	MIPIA_EN_DLY_CNTR
6B0F8h	MIPIA_TRANS_HACTIVE
6B0FCh	MIPIA_TRANS_VACTIVE
6B100h	MIPIA_TRANS_VTOTAL
6B104h	MIPIA_CTRL
6B108h	MIPIA_TE_CTR
6B118h	MIPIA_RD_DATA_RETURN 0
6B11Ch	MIPIA_RD_DATA_RETURN 1
6B120h	MIPIA_RD_DATA_RETURN 2
6B124h	MIPIA_RD_DATA_RETURN 3
6B128h	MIPIA_RD_DATA_RETURN 4
6B12Ch	MIPIA_RD_DATA_RETURN 5
6B130h	MIPIA_RD_DATA_RETURN 6
6B134h	MIPIA_RD_DATA_RETURN 7



Address	Name
6B138h	MIPIA_RD_DATA_VALID
6B13Ch	MIPIA_CRC_CTL
6B140h	MIPIA_CRC_RESULT
6B144h	MIPIA Dual Link Buffer Control
6B800h	MIPIC_DEVICE_READY_REG
6B804h	MIPIC_INTR_STAT_REG
6B808h	MIPIC_INTR_EN_REG
6B80Ch	MIPIC_DSI_FUNC_PRG_REG
6B810h	MIPIC_HS_TX_TIMEOUT_REG
6B814h	MIPIC_LP_RX_TIMEOUT_REG
6B818h	MIPIC_TURN_AROUND_TIMEOUT_REG
6B81Ch	MIPIC_DEVICE_RESET_TIMER
6B820h	MIPIC_DPI_RESOLUTION_REG
6B824h	MIPIC_DBI_FIFO_THRTL_REG
6B828h	MIPIC_HORIZ_SYNC_PADDING_COUNT
6B82Ch	MIPIC_HORIZ_BACK_PORCH_COUNT
6B830h	MIPIC_HORIZ_FRONT_PORCH_COUNT
6B834h	MIPIC_HORIZ_ACTIVE_AREA_COUNT
6B838h	MIPIC_VERT_SYNC_PADDING_COUNT
6B83Ch	MIPIC_VERT_BACK_PORCH_COUNT
6B840h	MIPIC_VERT_FRONT_PORCH_COUNT
6B844h	MIPIC_HIGH_LOW_SWITCH_COUNT

Address	Name
6B848h	MIPIC_DPI_CTRL_REG
6B84Ch	MIPIC_DPI_DATA_REGISTER
6B850h	MIPIC_INIT_COUNT_REGISTER
6B854h	MIPIC_MAX_RETURN_PKT_SIZE_REGISTER
6B858h	MIPIC_VIDEO_MODE_FORMAT_REGISTER
6B85Ch	MIPIC_EOT_DISABLE_REGISTER
6B860h	MIPIC_LP_BYTECLK_REGISTER
6B864h	MIPIC_LP_GEN_DATA_REGISTER
6B868h	MIPIC_HS_GEN_DATA_REGISTER
6B86Ch	MIPIC_LP_GEN_CTRL_REGISTER
6B870h	MIPIC_HS_GEN_CTRL_REGISTER
6B874h	MIPIC_GEN_FIFO_STAT_REGISTER
6B878h	MIPIC_HS_LS_DBI_ENABLE_REG
6B87Ch	MIPI_HS_READ_TRANSFER_COUNT
6B880h	MIPIC_DPHY_PARAM_REG
6B884h	MIPIC_DBI_BW_CTRL_REG
6B888h	MIPIC_CLK_LANE_SWITCHING_TIME_CNT
6B88Ch	MIPIC_STOP_STATE_STALL
6B890h	MIPIC_INTR_STAT_REG_1
6B894h	MIPIC_INTR_EN_REG_1
6B898h	MIPIC_CLK_LANE_TIMING
6B89Ch	MIPIC_PLL_LOCK_COUNT



Address	Name
6B8A0h	MIPIC_DATA_LANE_POLARITY
6B8A4h	MIPIC_TLPX_TIME_COUNT
6B8C0h	MIPIC_PORT_CTRL
6B8C4h	MIPIC_STATUS
6B8C8h	MIPIC_AUTOPWG
6B8CCh	MIPIC_WR_DATA 0
6B8D0h	MIPIC_WR_DATA 1
6B8D4h	MIPIC_WR_DATA 2
6B8D8h	MIPIC_WR_DATA 3
6B8DCh	MIPIC_WR_DATA 4
6B8E0h	MIPIC_WR_DATA 5
6B8E4h	MIPIC_WR_DATA 6
6B8E8h	MIPIC_WR_DATA 7
6B8ECh	MIPIC_WR_COMMAND
6B8F0h	MIPIC_WR_DATA_CTRL
6B8F4h	MIPIC_EN_DLY_CNTR
6B8F8h	MIPIC_TRANS_HACTIVE
6B8FCh	MIPIC_TRANS_VACTIVE
6B900h	MIPIC_TRANS_VTOTAL
6B904h	MIPIC_CTRL
6B908h	MIPIC_TE_CTR
6B918h	MIPIC_RD_DATA_RETURN 0

Address	Name
6B91Ch	MIPIC_RD_DATA_RETURN 1
6B920h	MIPIC_RD_DATA_RETURN 2
6B924h	MIPIC_RD_DATA_RETURN 3
6B928h	MIPIC_RD_DATA_RETURN 4
6B92Ch	MIPIC_RD_DATA_RETURN 5
6B930h	MIPIC_RD_DATA_RETURN 6
6B934h	MIPIC_RD_DATA_RETURN 7
6B938h	MIPIC_RD_DATA_VALID
6B93Ch	MIPIC_CRC_CTL
6B940h	MIPIC_CRC_RESULT
6B944h	MIPIC Dual Link Buffer Control

**DSC****Note**

These registers must all be written only as full 32 bit Dwords. Byte or word writes are not supported.

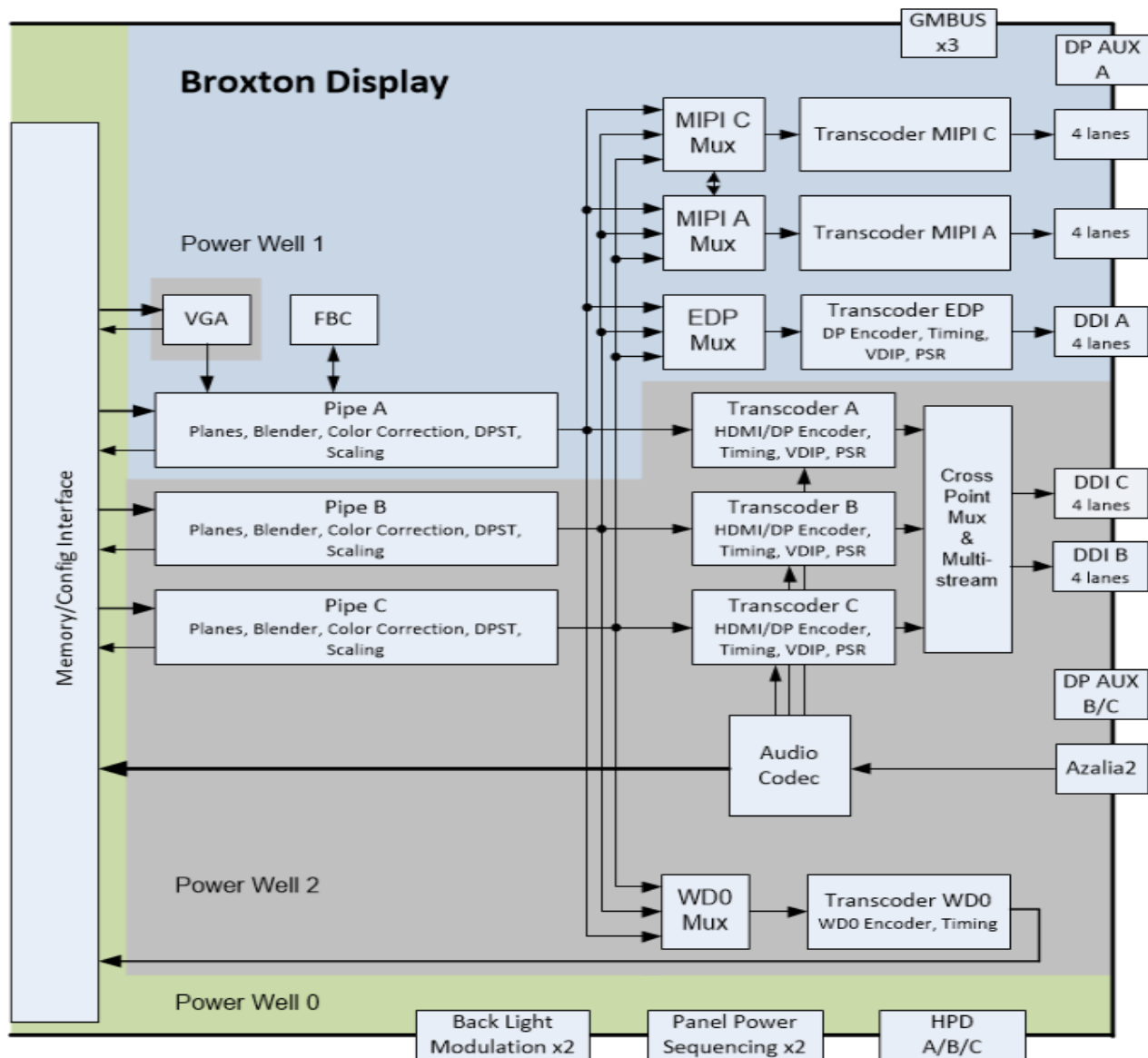
Address	Name
6B200h	DSCA_PICTURE_PARAMETER_SET_0
6B204h	DSCA_PICTURE_PARAMETER_SET_1
6B208h	DSCA_PICTURE_PARAMETER_SET_2
6B20Ch	DSCA_PICTURE_PARAMETER_SET_3
6B210h	DSCA_PICTURE_PARAMETER_SET_4
6B214h	DSCA_PICTURE_PARAMETER_SET_5
6B218h	DSCA_PICTURE_PARAMETER_SET_6
6B21Ch	DSCA_PICTURE_PARAMETER_SET_7
6B220h	DSCA_PICTURE_PARAMETER_SET_8
6B224h	DSCA_PICTURE_PARAMETER_SET_9
6B228h	DSCA_PICTURE_PARAMETER_SET_10
6B22Ch	DSCA_PICTURE_PARAMETER_SET_11
6B230h	DSCA_RC_BUF_THRESH_0
6B238h	DSCA_RC_BUF_THRESH_1
6B240h	DSCA_RC_RANGE_PARAMETERS_0
6B248h	DSCA_RC_RANGE_PARAMETERS_1
6B250h	DSCA_RC_RANGE_PARAMETERS_2
6B258h	DSCA_RC_RANGE_PARAMETERS_3
6B260h	DSCA_PICTURE_PARAMETER_SET_12

Address	Name
6B264h	DSCA_PICTURE_PARAMETER_SET_13
6B268h	DSCA_PICTURE_PARAMETER_SET_14
6B26Ch	DSCA_PICTURE_PARAMETER_SET_15
6B270h	DSCA_PICTURE_PARAMETER_SET_16
6B280h	Reserved
6B284h	DSC_CRC_CTL_A
6B288h	DSC_CRC_RES_A
6B28Ch	Reserved
6B290h	Reserved
6B294h	Reserved
6B298h	Reserved
6B29Ch	Reserved
6B2A0h	Reserved
6B2A4h	Reserved
6B2A8h	Reserved
6BA00h	DSCC_PICTURE_PARAMETER_SET_0
6BA04h	DSCC_PICTURE_PARAMETER_SET_1
6BA08h	DSCC_PICTURE_PARAMETER_SET_2
6BA0Ch	DSCC_PICTURE_PARAMETER_SET_3
6BA10h	DSCC_PICTURE_PARAMETER_SET_4
6BA14h	DSCC_PICTURE_PARAMETER_SET_5
6BA18h	DSCC_PICTURE_PARAMETER_SET_6
6BA1Ch	DSCC_PICTURE_PARAMETER_SET_7
6BA20h	DSCC_PICTURE_PARAMETER_SET_8
6BA24h	DSCC_PICTURE_PARAMETER_SET_9



Address	Name
6BA28h	DSCC_PICTURE_PARAMETER_SET_10
6BA2Ch	DSCC_PICTURE_PARAMETER_SET_11
6BA30h	DSCC_RC_BUF_THRESH_0
6BA38h	DSCC_RC_BUF_THRESH_1
6BA40h	DSCC_RC_RANGE_PARAMETERS_0
6BA48h	DSCC_RC_RANGE_PARAMETERS_1
6BA50h	DSCC_RC_RANGE_PARAMETERS_2
6BA58h	DSCC_RC_RANGE_PARAMETERS_3
6BA60h	DSCC_PICTURE_PARAMETER_SET_12
6BA64h	DSCC_PICTURE_PARAMETER_SET_13
6BA68h	DSCC_PICTURE_PARAMETER_SET_14
6BA6Ch	DSCC_PICTURE_PARAMETER_SET_15
6BA70h	DSCC_PICTURE_PARAMETER_SET_16
6BA80h	Reserved
6BA84h	DSC_CRC_CTL_C
6BA88h	DSC_CRC_RES_C
6BA8Ch	Reserved
6BA90h	Reserved
6BA94h	Reserved
6BA98h	Reserved
6BA9Ch	Reserved
6BAA0h	Reserved
6BAA4h	Reserved
6BAA8h	Reserved

Broxton Display Connections

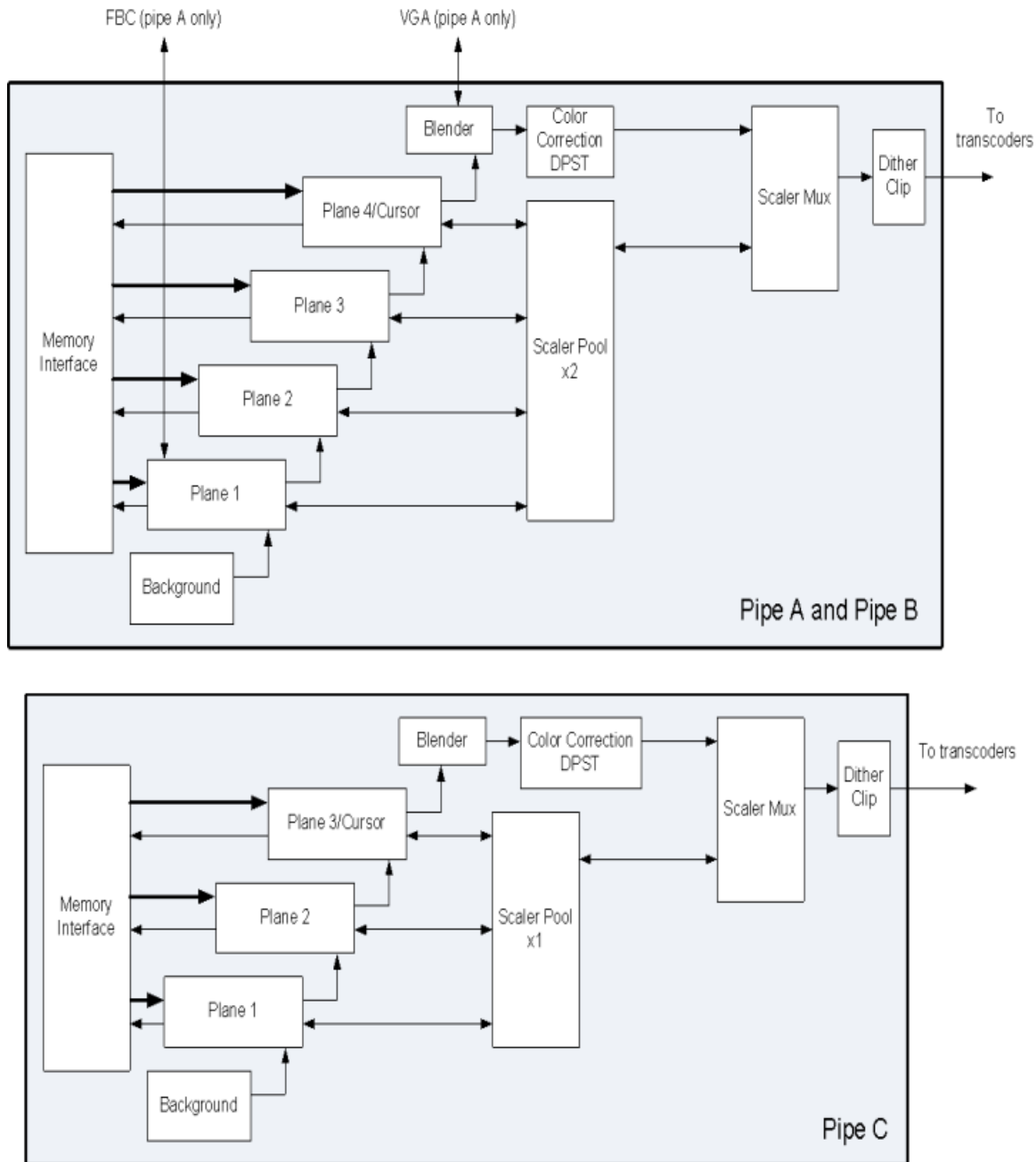


The front end of the display contains the pipes. There are three instances which are referred to as Pipe A, Pipe B, and Pipe C.

The pipes connect to the transcoders. There are seven instances which are referred to as Transcoder A, Transcoder B, Transcoder C, Transcoder EDP, Transcoder WD0, Transcoder MIPIA, and Transcoder MIPI C.

The transcoders connect to the DDIs. There are three instances which are referred to as DDI A, DDI B, and DDI C.

Display Pipes



The display pipes contain the planes, blending, color correction, DPST, scaling, dithering, and clipping.

Pipe A and Pipe B have four planes and a cursor. Each plane can be used as a sprite, primary, or overlay.

Pipe C has three planes and a cursor. Each plane can be used as a sprite, primary, or overlay.

The background color that is seen under the bottom most plane is programmable.

The plane blending follows a fixed Z-order. Plane 1 is the bottom most plane and higher numbered planes stack on top of it.



The cursor and top most plane are mutually exclusive and cannot be both enabled at the same time.

Pipe A and Pipe B each have two pipe scalers. Pipe C has one pipe scaler.

Each pipe scaler can be assigned to scale an individual plane or scale the blended output.

Display Transcoders

The display transcoders contain the timing generators and port encoders.

Transcoders A, B, and C also contain Audio/Video mixers, Video Data Island Packet mixers, and Panel Self Refresh controllers.

Transcoder EDP also contains a Video Data Island Packet mixer and Panel Self Refresh controllers. It does not support HDMI, DVI, or Audio.

Transcoder WD0 only supports display capture and write back to memory.

Transcoders MIPIA and MIPIC only supports MIPI DSI.

Audio

The Azalia interface provides data to the audio codec.

The audio codec connects to the Audio/Video mixers in the transcoders.

The audio codec connects to memory write back for wireless audio.

DDIs

The DDIs contain the DisplayPort transport control and other port logic to interface to the DDI physical pins.

DDI A, DDI B, and DDI C support lane reversal where the internal lane to package lane mapping is swapped.

DDI A does not support DisplayPort multistream.

DisplayPort A, B, and C Lane Mapping:

Package Pin	Non-Reversed	Reversed
DDI 3	Main Link Lane 3	Main Link Lane 0
DDI 2	Main Link Lane 2	Main Link Lane 1
DDI 1	Main Link Lane 1	Main Link Lane 2
DDI 0	Main Link Lane 0	Main Link Lane 3

HDMI/DVI TMDS Lane Mapping:

Package Pin	Non-Reversed	Reversed
DDI 3	TMDS Clock	TMDS Data2
DDI 2	TMDS Data0	TMDS Data1



Package Pin	Non-Reversed	Reversed
DDI 1	TMDS Data1	TMDS Data0
DDI 0	TMDS Data2	TMDS Clock

DDI Equivalent Names:

DDI Name	Equivalent Names
DDI A	DDI-A, DDIA, Port A, eDP
DDI B	DDI-B, DDIB, Port B
DDI C	DDI-C, DDIC, Port C

Broxton 0 and Broxton 1 Board Mapping:

DDI Name in Display Engine	Display PHY Name	Die Bump Name	Board Connection
DDI A main link	Port 0 of the single port PHY	DDI-2	eDP
DDI B main link	Port 0 of the dual port PHY	DDI-0	DP/HDMI
DDI C main link	Port 1 of the dual port PHY	Not connected (DDI-1)	Not connected

Broxton P Board Mapping:

DDI Name in Display Engine	Display PHY Name	Die Bump Name	Board Connection
DDI A main link	Port 0 of the single port PHY	EDP	eDP
DDI B main link	Port 0 of the dual port PHY	DDI-0	DP/HDMI
DDI C main link	Port 1 of the dual port PHY	DDI-1	DP/HDMI

Pipe to Transcoder to DDI Mappings

Twin modes are not supported.

Any pipe can drive any single DDI.

With DisplayPort multistream it is possible to have multiple pipes driving a single DDI. DDI B and DDI C support multistream. DDI A does not support multistream.

Any pipe can connect to any transcoder, but not more than one simultaneously.

Transcoder A is tied to Pipe A.

Transcoder B is tied to Pipe B.

Transcoder C is tied to Pipe C.

Transcoders EDP, WD0, MIPIA, and MIPIC can connect to Pipe A, Pipe B, or Pipe C, but only one at a time.

Transcoders A, B, and C can connect to DDI B or DDI C, but only one at a time.

Transcoder EDP can connect only to DDI A.

Transcoder WD0 does not connect to any DDI. Transcoder WD0 output only goes to memory write back.



Transcoders MIPIA and MIPIC does not connect to any DDI. Transcoders MIPIA and MIPIC output only goes to MIPI.

DDI A can connect only to Transcoder EDP. DDI A does not support DisplayPort multistream.

DDI B can connect to Transcoder A, B, or C, individually or simultaneously if DisplayPort multistream is used.

DDI C can connect to Transcoder A, B, or C, individually or simultaneously if DisplayPort multistream is used.

Mode Set

Broxton Sequences to Initialize Display

These sequences are used to initialize the display engine before any display engine functions can be enabled.

Most display engine functions will not operate while display is not initialized. Only basic PCI, I/O, and MMIO register read/write operations are supported when display is not initialized.

Initialize Sequence

1. Disable PCH Reset Handshake
 - a. Clear NDE_RSTWRN_OPT RST PCH Handshake En to 0b.
2. Enable Power Well 1 (PG1)
 - a. Poll for FUSE_STATUS Fuse PG0 Distribution Status == 1b.
 - Timeout and fail after 5 μ s.
 - b. Set PWR_WELL_CTL Power Well 1 Request to 1b.
 - c. Poll for PWR_WELL_CTL Power Well 1 State == 1b.
 - Timeout and fail after 10 μ s.
 - d. Poll for FUSE_STATUS Fuse PG1 Distribution Status == 1b.
 - Timeout and fail after 5 μ s.
3. Enable CD clock following the Sequences for Changing CD Clock Frequency
4. Enable DBUF
 - a. Set DBUF_CTL DBUF Power Request to 1b.
 - b. Poll for DBUF_CTL DBUF Power State == 1b.
 - Timeout and fail after 10 μ s.
5. If DDIA/EDP, DDIB, or DDIC will be used, follow DDI Buffer DDI PHY Initialization Sequence to initialize DDI PHY
6. If MIPI will be used, follow Mode Set Sequences for MIPI to initialize MIPI PHY



7.

Workaround

If MIPI will not be used, power down DSI regulator to save power.

- a. Set P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR MIPIO_RST_CTRL to 0x1 to bring MIPI IO out of reset
- b. Write 0x160020 = 0x00000001 (DSI_CFG: STAP_SELECT 0x1)
- c. Write 0x160054 = 0x00000001 (DSI_TXCNTRL: HS_IO_CONTROL_SELECT 0x1)
- d. Set P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR MIPIO_RST_CTRL to 0x0 to put MIPI IO back into reset

Un-initialize Sequence

1. Disable all display engine functions using the full mode set disable sequence on all pipes, transcoders, ports, planes, and power well 2 (PG2).
2. Clear both PHY_CTL_FAMILY_EDP and PHY_CTL_FAMILY_DDI Common Reset to 0b (Disable)
3. Clear P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR to 0x0
4. Disable DBUF
 - a. Clear DBUF_CTL DBUF Power Request to 0b.
 - b. Poll for DBUF_CTL DBUF Power State == 0b.
 - Timeout and fail after 10 μ s.
5. Disable CD clock following the Sequences for Changing CD Clock Frequency
6. Disable Power Well 1 (PG1)
 - a. Clear PWR_WELL_CTL Power Well 1 Request to 0b.
 - b. Wait for 10us. Do not poll for the power well to disable. Other clients may be keeping it enabled.

Sequences for MIPI

This topic describes the sequences for MIPI enable, disable, commands, and DBI frames.

Programming Note**Context:**

DBI Mode

(BXT:*:A) In DBI mode there must always be at least one plane enabled on the pipe attached to MIPI.

Enable Sequence

Display must already be initialized.

1. **If using pipe B or pipe C - Enable Power Well 2**
 - a. Enable PWR_WELL_CTL Power Well 2 Request

- b. Wait for PWR_WELL_CTL Power Well 2 State == Enabled, timeout after 20 us
- c. Wait for FUSE_STATUS FUSE PG2 Distribution Status == Done, timeout after 1 us
- 2. **If using hardware panel power control - Enable Panel Power**
 - a. Enable panel power sequencing
 - b. Wait for panel power sequencing to reach the enabled state
- 3. **If DSI PLL not already enabled - configure and enable MIPI clocks**
 - a. Configure dividers in MIPI_CLOCK_CTL
 - b. Follow MIPI DSI PLL Enabling Sequence.
- 4. **Exit Low Power Mode**
 - a. Set P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR MIPIO_RST_CTRL to 0x1 to bring MIPI IO out of reset and start RCOMP
 - b. BXT A0: Set DSI_RCOMP_CFG1 mipA_dphy_defeature_en and mipC_dphy_defeature_en to 0x1 and configure mip<A,C>_lane_count to the number of lanes that will be used
 - c.

Workaround
Power up DSI regulator i. Write 0x160020 = 0x00000001 (DSI_CFG: STAP_SELECT 0x1) ii. Write 0x160054 = 0x00000000 (DSI_TXCNTRL: HS_IO_CONTROL_SELECT 0x0)

- | |
|---|
| Power up DSI regulator <ul style="list-style-type: none"> i. Write 0x160020 = 0x00000001 (DSI_CFG: STAP_SELECT 0x1) ii. Write 0x160054 = 0x00000000 (DSI_TXCNTRL: HS_IO_CONTROL_SELECT 0x0) |
|---|
- d. If currently in Low Power mode, follow the Exit Low Power Mode sequence
 - e. Enable transparent latch - Set MIPI_PORT_CTRL LPOUTPUT_HOLD to 0x1
 - 5. **If needed - Send Manufacturer DCS Commands to Initialize DSI Controller**
 - a. Set MIPI_DEVICE_READY_REG DEVICE_READY to 0x1
 - b. Follow Command Sequence for Generic/Manufacturer Writes/Reads
 - 6. **Enable Planes and Pipe Scaler**
 - a. Configure and enable planes (VGA or hires). This can be done later if desired.
 - b. If VGA, clear VGA I/O register SR01 bit 5
 - c. Enable pipe scaler if needed (must be enabled for VGA)
 - d. Configure pipe settings
 - 7. **Prepare Port**
 - a. Clear MIPI_DEVICE_READY_REG DEVICE_READY to 0x0
 - b. Configure MIPIA_DPHY_PARAM_REG and MIPIC_DPHY_PARAM_REG (both must be configured regardless of single or dual link mode in order to allow ULPS to be entered later)
 - c. Configure MIPI_TRANS_HACTIVE and MIPI_TRANS_VACTIVE
 - d. If DPI, configure MIPI_TRANS_VTOTAL, MIPI_DPI_RESOLUTION_REG, back porch, front porch, and sync padding registers
 - e. Configure other timing parameters, timeouts, switch count, byteclk



- f. Configure MIPIA_INIT_COUNT_REGISTER and MIPIC_INIT_COUNT_REGISTER (both must be configured regardless of single or dual link mode in order to allow ULPS to be entered later)
 - g. If DBI, configure MIPI_HS_LS_DBI_ENABLE_REG, MIPI_DBI_FIFO_THRTL_REG, and MIPI_DBI_BW_CTRL_REG
 - h. Configure MIPI_DSI_FUNC_PRG_REG format
 - i. Configure MIPI_CTRL Pipe Select
 - j. Configure MIPI_EOT_DISABLE_REGISTER CLOCKSTOP, depending on panel type.
 - k. BXT B0 onwards: Set MIPI_EOT_DISABLE_REGISTER DPHY_DEFEATURE_EN to 0x1.
 - l. If DPI, set MIPI_EOT_DISABLE_REGISTER DEFEATURE_DPI_FIFO_CTR to 0x1.
 - m. If DPI, set MIPI_VIDEO_MODE_FORMAT_REGISTER IP_TG_CONFIG to 0x1.
 - n. If DBI dual link, configure MIPI_DLBUFFER_CTRL
 - o. If DBI using tearing, configure MIPI_PORT_CTRL EFFECT
 - p. If DBI using tearing and a tear delay is needed, configure MIPI_TE_CTR and set MIPI_PORT_CTRL DELAY to 0x1
 - q. Set MIPI_DEVICE_READY_REG DEVICE_READY to 0x1
 - r. If DPI, set MIPI_DPI_CTRL_REG TURN_ON to 0x1
 - s. If DPI, wait for the SPL_PKT_SENT_INTERRUPT. Timeout after 1ms.
 - t. Configure MIPI_MAX_RETURN_PKT_SIZE_REGISTER
8. **Send Display On MCS Commands**
- a. If DBI using tearing, send the set_tear_on or set_tear_scanline command
 - b. If DBI using backlight control in the panel, send the backlight enable command
 - c. Send Display On Commands, depending on the panel type
9. **Enable Timing Generator**
- a. If DPI, set MIPI_PORT_CTRL EN to 0x1 to start the timing generator
10. **Enable Backlight**
- a. If DPI, wait for data on to backlight enable delay
 - b. If DPI, enable panel backlight

Interrupt Usage

MIPI interrupt events are enabled by setting bits in MIPI_INTR_EN_REG and MIPI_INTR_EN_REG_1. When an enabled interrupt event occurs, it sets a sticky bit in MIPI_INTR_STAT_REG or MIPI_INTR_STAT_REG_1. The sticky bits are OR'd together to create the consolidated interrupts for MIPI A and MIPI C in the DE Port Interrupt, which propagates to the internal graphics interrupt. To detect a MIPI event, software can either poll on the MIPI status bit or use the internal graphics interrupt. The sticky bit should be cleared by writing a 1 to it.

Command Sequence for DBI Writes/Reads

1. Poll for MIPI_WR_DATA_CTRL COMMAND_VALID = 0x0 to ensure no command is being processed.
2. Configure MIPI_WR_COMMAND with the command byte to be sent to the panel.
3. Configure MIPI_WR_DATA registers with the data bytes to be sent to the panel.
4. Configure MIPI_WR_DATA_CTL WR_BYTE_LENGTH and set COMMAND_VALID to 0x1 to execute the write command, hardware will deassert the bit when done.
5. If doing a read, poll for MIPI_RD_DATA_VALID READ_DATA_VALID == count of number of registers expected to be read.
6. If doing a read, get read data from MIPI_RD_DATA_RETURN registers.

Command Sequence for Generic/Manufacturer Writes/Reads

1. If long, write data bytes to MIPI_<HS,LP>_GEN_DATA_REG. If more than 4 bytes, continue to write data to the same register where it will be placed into a FIFO.
2. If short, configure MIPI_<HS,LP>_GEN_CTRL_REG WORD_COUNT with the 0-2 parameters.
3. If long, configure MIPI_<HS,LP>_GEN_CTRL_REG WORD_COUNT with the data byte count.
4. Configure MIPI_<HS,LP>_GEN_CTRL_REG DATA_TYPE
5. If doing a read, wait for the GEN_READ_DATA_AVAIL interrupt. Timeout after 1ms.
6. If doing a read, get read data from MIPI_<HS,LP>_GEN_DATA_REGISTERS. If more than 4 bytes, continue to read the same register until all data is received.

DBI Frame Sequence

MIPI Enable Sequence must be completed first.

Repeat this sequence for each frame to be sent.

1. Poll for MIPI_WR_DATA_CTRL COMMAND_VALID == 0x0 to ensure no command is being processed.
2. Configure MIPI_WR_COMMAND with the command to be sent to the panel.
3. Set MIPI_WR_DATA_CTL COMMAND_VALID to 0x1 to execute the write command. Hardware will deassert the bit when done.
4. If using tearing command, set MIPI_DEVICE_READY_REG BUS_POSSESSION to 0x1 to give bus possession to the panel. If using the tearing pin, the bus possession does not have to be given.
5. If using tearing command, wait until the start of vertical blank, then clear MIPI_DEVICE_READY_REG BUS_POSSESSION to 0x0.

Disable Sequence

1. **Disable Backlight**
 - a. Disable panel backlight

**2. If DPI, Send DPI Shutdown Packet**

- a. Set MIPI_DPI_CTRL_REG SHUT_DOWN to 0x1
- b. Wait for SPL_PKT_SENT_INTERRUPT. Timeout after 1ms.

3. Disable Planes

- a. If VGA
 - i. Set VGA I/O register SR01 bit 5 for screen off
 - ii. Wait for 100 us
- b. Disable planes (VGA or hires)
- c. Disable pipe scaler

4. Disable Port

- a. If DBI, poll for MIPI_WR_DATA_CTRL COMMAND_VALID == 0x0 to ensure command is done
- b. If DBI, poll for MIPI_GEN_FIFO_STAT_REGISTER DPI_FIFO_EMPTY and DBI_FIFO_EMPTY == 0x1 to ensure data is done
 - If dual link mode, only poll on MIPI C FIFO empties.
- c. If DPI, clear MIPI_PORT_CTRL EN to 0x0

5. Send Manufacturer DCS Commands

- a. If DBI using tearing, send set_tear_off command
- b. Send Display Off Commands, depending on the panel type
 - Note: If LP commands need to be sent as part of the Display Off commands, and MIPI is NOT running in clock stopping mode (MIPI_EOT_DISABLE_REGISTER CLOCKSTOP==0), then clock stopping mode needs to be enabled before the LP commands can be sent.
 - i. Clear MIPI_DEVICE_READY_REG DEVICE_READY to 0x0
 - ii. Set MIPI_EOT_DISABLE_REGISTER CLOCKSTOP to 0x1
 - iii. Set MIPI_DEVICE_READY_REG DEVICE_READY to 0x1
 - iv. Send LP commands as needed
- c. Poll for MIPI_GEN_FIFO_STAT_REGISTER HS_CTRL_FIFO_EMPTY, HS_DATA_FIFO_EMPTY, LP_CTRL_FIFO_EMPTY, and LP_DATA_FIFO_EMPTY == 0x1 to ensure all commands have been sent

6. If using hardware panel power control - Disable Panel Power

- a. Disable panel power sequencing
- b. Wait for power down delay and power cycle delay

7. If all MIPI ports disabled and low power mode requested - Enter Low Power Mode

- a. Follow the Enter Low Power Mode sequence
- b.

Workaround

Power down DSI regulator to save power.

Workaround

- a. Write 0x160020 = 0x00000001 (DSI_CFG: STAP_SELECT 0x1)
- b. Write 0x160054 = 0x00000001 (DSI_TXCNTRL: HS_IO_CONTROL_SELECT 0x1)
- c. Clear P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR MIPIO_RST_CTRL to 0x0 to put MIPI IO into reset and stop RCOMP
- d. Follow the MIPI DSI PLL Disabling Sequence

Enter Low Power Mode

1. Set MIPIA_DEVICE_READY_REG and MIPIC_DEVICE_READY_REG DEVICE_READY to 0x1
2. Enable transparent latch - Set MIPIA_PORT_CTRL LPOUTPUT_HOLD to 0x1
3. Wait for 10us
4. Enter ULPS - Set MIPIA_DEVICE_READY_REG and MIPIC_DEVICE_READY_REG DEVICE_READY to 0x1 and ULPS_STATE to 0x2
5. Poll for MIPIA_PORT_CTL AFE_LATCHOUT == 0x0
6. Disable transparent latch - Set MIPIA_PORT_CTRL LPOUTPUT_HOLD to 0x0
- Device ready must be kept at 0x1 while in low power mode

Exit Low Power Mode

1. Wait for at least 2.5ms while in the ULPS state
2. Enter ULPS - Set MIPIA_DEVICE_READY_REG and MIPIC_DEVICE_READY_REG DEVICE_READY to 0x1 and ULPS_STATE to 0x2
3. Wait for 2us for ULPS to complete
4. Enable transparent latch - Set MIPIA_PORT_CTRL LPOUTPUT_HOLD to 0x1
5. Exit ULPS - Set MIPIA_DEVICE_READY_REG and MIPIC_DEVICE_READY_REG DEVICE_READY to 0x1 and ULPS_STATE to 0x1
6. Wait for 1ms
7. Enter normal mode - Set MIPIA_DEVICE_READY_REG and MIPIC_DEVICE_READY_REG DEVICE_READY to 0x1 and ULPS_STATE to 0x0

Overall Flow

1. Initialization Sequence (ULPS exited by default, latch out disabled)
2. Enable PLL with dividers setup for any future use for both MIPI ports (can't change dividers after PLL is enabled)
3. Exit Low Power Mode if not already exited from boot



4. Enable and disable MIPI ports as needed (enable sequence and disable sequence, while keeping PLL enabled and not entering Low Power Mode)
5. If all MIPI ports disabled and low power requested, Enter Low Power Mode and Disable PLL
6. If MIPI needs to be enabled again, go to step 2. Else, display can be un-initialized or configured for DC9.

Sequences for DisplayPort

This topic describes how to enable and disable DisplayPort.

Enable Sequence

Display must already be initialized

DDIA Lane Capability Control must be configured prior to enabling any ports or port clocks

1. **If not PipeA+DDIA - Enable Power Well 2**
 - a. Enable PWR_WELL_CTL Power Well 2 Request
 - b. Wait for PWR_WELL_CTL Power Well 2 State = Enabled, timeout after 20 us
 - c. Wait for FUSE_STATUS FUSE PG2 Distribution Status = Done, timeout after 1 us
2. **If panel power sequencing is required - Enable Panel Power**
 - a. Enable panel power sequencing
 - b. Wait for panel power sequencing to reach the enabled state
3. **Enable Port PLL**
 - a. If PLL is not already enabled, follow port clock programming sequence from Clocks section
 - b. If PLL to port mapping is flexible, configure PLL to port mapping to direct the PLL output to the DDI
4. **If IO power is controlled through PWR_WELL_CTL - Enable IO Power**
 - a. Enable PWR_WELL_CTL DDI IO Power Request for the DDI that will be used
 - b. Wait for PWR_WELL_CTL DDI IO Power Request = Enabled, timeout after 20 us
5. **Enable and Train DisplayPort**
 - a. Configure and enable DP_TP_CTL with link training pattern 1 selected
 - b. Configure voltage swing and related IO settings. Refer to DDI Buffer section.
 - c. Configure and enable DDI_BUF_CTL
 - d. Follow DisplayPort specification training sequence (see notes for failure handling)
 - e. If DisplayPort multi-stream - Set DP_TP_CTL link training to Idle Pattern, wait for 5 idle patterns (DP_TP_STATUS Min_Idles_Sent) (timeout after 800 us)
 - f. Set DP_TP_CTL link training to Normal.
6. **Enable Planes, Pipe, and Transcoder (repeat to add multiple pipes on a single port for multi-streaming)**



- a. If DisplayPort multi-stream - use AUX to program receiver VC Payload ID table to add stream
- b. Configure Transcoder Clock Select to direct the Port clock to the Transcoder
- c. Configure and enable planes (VGA or hires). This can be done later if desired.
- d. If VGA - Clear VGA I/O register SR01 bit 5
- e. Enable panel fitter if needed (must be enabled for VGA)
- f. Configure transcoder timings, M/N/TU/VC payload size, and other pipe and transcoder settings
- g. Configure and enable TRANS_DDI_FUNC_CTL
- h. If DisplayPort multistream - Enable pipe VC payload allocation in TRANS_DDI_FUNC_CTL
- i. If DisplayPort multistream - Wait for ACT sent status in DP_TP_STATUS and receiver DPCD (timeout after >410us)
- j. Configure and enable TRANS_CONF
- k. If panel power sequencing is required - Enable panel backlight

SRD and/or Audio can be enabled after everything is complete. Follow the audio enable sequence in the audio registers section.

Notes

Changing voltage swing during link training:

- Change the swing setting following the DDI Buffer section. The port does not need to be disabled.

Changing port width (lane count) or frequency during link training:

1. Follow Disable Sequence for DisplayPort to Disable Port
2. If PLL frequency needs to change, Follow Disable Sequence for DisplayPort to Disable PLL, then follow Enable Sequence for DisplayPort to Enable PLL, using the new frequency settings
3. Follow Enable Sequence for DisplayPort to Enable and Train DisplayPort, using the new port width settings

If the mode set fails, follow the disable sequence to disable everything that had been enabled up to the failing point.

Enabling DisplayPort Sync Mode

See TRANS_DDI_FUNC_CTL Port Sync Mode Enable for restrictions.

1. Follow the enable sequence for the DisplayPort slave, but skip the step that sets DP_TP_CTL link training to Normal (stay in Idle Pattern).
 - Set TRANS_DDI_FUNC_CTL Port Sync Mode Master Select and Port Sync Mode Enable when configuring and enabling TRANS_DDI_FUNC_CTL.



2. Follow the enable sequence for the DisplayPort master, but skip the step that sets DP_TP_CTL link training to Normal (stay in Idle Pattern).
3. Set DisplayPort slave DP_TP_CTL link training to Normal.
4. Wait 200 μ S.
5. Set DisplayPort master DP_TP_CTL link training to Normal.

Software may need to use DOUBLE_BUFFER_CTL to ensure updates to plane and pipe registers will take place in the same frame.

For example: If pipe A and pipe B are synchronized together and software needs the surface addresses for two planes to update at the same time, software should use DOUBLE_BUFFER_CTL when writing the surface address registers for both planes, otherwise there is a possibility that the updates could be split across a vertical blank such that one plane would update on the current vertical blank and the other plane would update on the next vertical blank.

Disable Sequence

SRD and Audio must be disabled first. Follow the audio disable sequence in the audio registers section.

1. **If panel power sequencing is required - Disable panel backlight**
2. **Disable Planes, Pipe, and Transcoder (repeat to remove multiple pipes from a single port for multi-streaming)**
 - a. If VGA
 - i. Set VGA I/O register SR01 bit 5 for screen off
 - ii. Wait for 100 μ s
 - b. Disable planes (VGA or hires)
 - c. Disable TRANS_CONF
 - d. Wait for off status in TRANS_CONF, timeout after two frame times
 - e. If DisplayPort multistream - use AUX to program receiver VC Payload ID table to delete stream
 - f. If done with this VC payload
 - i. Disable VC payload allocation in TRANS_DDI_FUNC_CTL
 - ii. Wait for ACT sent status in DP_TP_STATUS and receiver DPCD
 - g. Disable TRANS_DDI_FUNC_CTL with DDI_Select set to None
 - h. Disable panel fitter
 - i. Configure Transcoder Clock Select to direct no clock to the transcoder
3. **Disable Port (all pipes and VC payloads on this port must already be disabled)**
 - a. Disable DDI_BUF_CTL
 - b. Disable DP_TP_CTL (do not set port to idle when disabling)
 - c. BXT: Wait 16 μ s for buffers to return to idle

4. **If panel power sequencing is required - Disable Panel Power**
 - a. Disable panel power sequencing
5. **If IO power is controlled through PWR_WELL_CTL - Disable IO Power**
 - a. Disable PWR_WELL_CTL DDI IO Power Request for the DDI that was used
6. **Disable Port PLL**
 - a. If PLL to port mapping is flexible, configure PLL to port mapping to direct no clock to the DDI
 - b. If this PLL is no longer needed, follow PLL disable sequence from Clocks section
7. **Disable Power Wells**
 - a. If no required resource is in the power well - Disable PWR_WELL_CTL Power Well 2 Request

Disabling DisplayPort Sync Mode

1. Follow the disable sequence for the DisplayPort slave.
2. Follow the disable sequence for the DisplayPort master.

Sequences for HDMI and DVI

This topic describes how to enable and disable HDMI and DVI.

Enable Sequence

Display must already be initialized

1. Enable Power Wells

- | |
|--|
| <ol style="list-style-type: none"> a. Enable PWR_WELL_CTL Power Well 2 Request b. Wait for PWR_WELL_CTL Power Well 2 State = Enabled, timeout after 20 us c. Wait for FUSE_STATUS FUSE PG2 Distribution Status = Done, timeout after 1 us |
|--|

2. Enable Port PLL

- a. If PLL is not already enabled, follow port clock programming sequence from Clocks section
- b. If PLL to port mapping is flexible, configure PLL to port mapping to direct the PLL output to the DDI

3. If IO power is controlled through PWR_WELL_CTL - Enable IO Power

- a. Enable PWR_WELL_CTL DDI IO Power Request for the DDI that will be used
- b. Wait for PWR_WELL_CTL DDI IO Power Request = Enabled, timeout after 20 us

4. Enable Planes, Pipe, and Transcoder

- a. Configure Transcoder Clock Select to direct the Port clock to the Transcoder
- b. Configure and enable planes (VGA or hires). This can be done later if desired.



- c. If VGA - Clear VGA I/O register SR01 bit 5
- d. Enable panel fitter if needed (must be enabled for VGA)
- e. Configure transcoder timings and other pipe and transcoder settings
- f. Configure and enable TRANS_DDI_FUNC_CTL
- g. Configure and enable TRANS_CONF

5. **Enable Port**

- a. Configure voltage swing and related IO settings. Refer to the DDI Buffer section.
- b. Configure and enable DDI_BUF_CTL

Audio can be enabled after everything is complete. Follow the audio enable sequence in the audio registers section.

Notes

If the mode set fails, follow the disable sequence to disable everything that had been enabled up to the failing point.

Disable Sequence

Audio must be disabled first. Follow the audio disable sequence in the audio registers section.

1. **Disable Planes, Pipe, and Transcoder**

- a. If VGA
 - i. Set VGA I/O register SR01 bit 5 for screen off
 - ii. Wait for 100 us
- b. Disable planes (VGA or hires)
- c. Disable TRANS_CONF
- d. Wait for off status in TRANS_CONF, timeout after two frame times
- e. Disable TRANS_DDI_FUNC_CTL with DDI_Select set to None
- f. Disable panel fitter
- g. Configure Transcoder Clock Select to direct no clock to the transcoder

2. **Disable Port**

- a. Disable DDI_BUF_CTL
- b. BXT: Wait 16 us for buffers to return to idle

3. **If IO power is controlled through PWR_WELL_CTL - Disable IO Power**

- a. Disable PWR_WELL_CTL DDI IO Power Request for the DDI that was used

4. **Disable Port PLL**

- a. If PLL to port mapping is flexible, configure PLL to port mapping to direct no clock to the DDI
- b. If this PLL is no longer needed, disable it



5. Disable Power Wells

- | |
|---|
| a. If no required resource is in the power well - Disable PWR_WELL_CTL Power Well 2 Request |
|---|

Sequences for Display C5 and C6

Display C5 (DC5) is a power saving state where hardware dynamically disables power well 1 and the CDCLK PLL and saves the associated registers.

DC5 can be entered when software allows it, power well 2 is disabled, and hardware detects that all pipes are disabled or pipe A is enabled with PSR active.

Display C6 (DC6) is a deeper power saving state where hardware dynamically disables power well 0 and saves the associated registers.

DC6 can be entered when software allows it, the conditions for DC5 are met, and the PCU allows DC6.

DC6 cannot be used if the backlight is being driven from the display utility pin.

Core CPUs support DC5 and DC6.

The context save and restore program is reset on cold boot, warm reset, PCI function level reset, and hibernate/suspend.

Atom CPUs support DC5 and not DC6. They also support DC9, which has a separate sequence.

The context save and restore program is reset on DC9, cold boot, warm reset, PCI function level reset, and hibernate/suspend.

The MIPI DSI related registers are not saved and restored by hardware.



Sequence to Allow DC5 or DC6

1. Load the correct stepping specific Display Context Save and Restore (CSR) program from the binary package.
 - a. Read the package header and extract the correct individual firmware. Binary package format details can be found in sections below.
 - b. Skip the header section at the start of the program binary.
 - c. Copy the payload into Display CSR Program Storage.
 - d. Perform the MMIO writes specified in the header section.
2. Configure display engine to have power well 2 disabled, following the appropriate mode set disable sequences for any ports using power well 2. This can be done earlier if desired.
3. Set display register 0x45520 bit 1 to 1b. It does not need to be cleared at any time.
4. Set DC_STATE_EN Dynamic DC State Enable = "Enable up to DC5" for DC5 or "Enable up to DC6" for DC6.

Programming Note

Context:

Display C5 and C6

Do not switch between "Enable up to DC5" and "Enable up to DC6" without moving to "Disable" and reloading the CSR program in between.

Disable DC5/DC6 during mode set and re-enable after the mode set programming is completed.

MMIO accesses have more latency when DC5/DC6 is enabled. For optimal performance, disable DC5/DC6 when programming a set of registers and re-enable them after the programming is completed.

Programming Note

Context:

Display C5 and C6

For atom CPUs, in step 3 also set 0x45520 bit 0 to 1b. It does not need to be cleared at any time.

Sequence to Disallow DC5 and DC6

1. Set DC_STATE_EN Dynamic DC State Enable = "Disable".

DMC Firmware Package

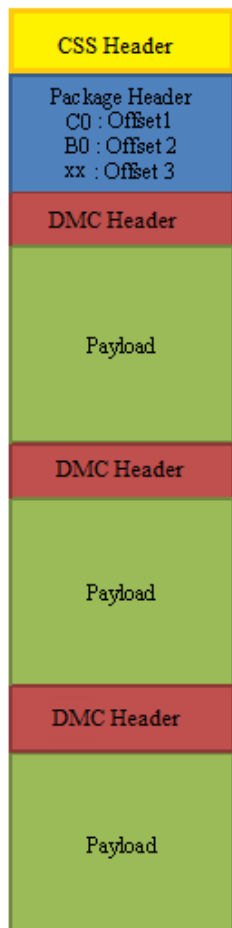
Display Micro-Controller firmware package includes all the firmwares that are required for different steppings of the product. The stepping dependent firmwares are all packaged and released as a single binary package. The package contains the CSS header, followed by the package header and the actual DMC firmwares.

Packaged firmware uses the following naming convention - <project>_dmc_ver<major>_<minor>.bin. The major version will get incremented whenever there is a change in the header layout and would require an update to the driver firmware loading module.

Major version 1

CSS Header	1.0
Package Header	1
DMC Header	1

Package Layout





CSS Header

```
typedef struct _CssHeader {
    uint32_t    moduleType;           // 0x09 for DMC
    uint32_t    headerLen;            // CSS header length in dwords
    uint32_t    headerVer;            // 0x10000
    uint32_t    moduleID;             // Not used
    uint32_t    moduleVendor;         // Not used
    uint32_t    date;                 // YYYYMMDD (YYYY « 16 + MM « 8
+ DD)
    uint32_t    size;                 // Total dmc fw binary size in
dwords - (CSS_HeaderLen + PackageHeaderLen + dmc FWsLen)/4
    uint32_t    keySize;              // Not used
    uint32_t    modulusSize;          // Not used
    uint32_t    exponentSize;         // Not used
    uint32_t    reserved1[12];        // Not used
    uint32_t    version;              // Major Minor
    uint32_t    reserved2[8];         // Not used
    uint32_t    uKernelHeaderInfo;    // Not used
} CssHeader;
```

Package Header

Package header contains the firmware/stepping mapping table and the corresponding firmware offsets to the individual binaries, within the package. Mapping table will list the exceptions first, followed by the default entries. An Offset value of "0xFFFFFFFF" in the mapping table indicates that there is no firmware available/supported for that stepping. The offsets to the individual binary are DWord aligned. The first individual binary starts at an offset value of "0x00000000" after the CSS Header and the Package Header.

Stepping/Version mapping example

Stepping	FW Version
A1	1.1
B*	1.6
**	2.3

```
typedef struct _PackageHeader {
    uint8_t    headerLen;             // DMC package header length
in dwords
    uint8_t    headerVer;             // 0x01
```

```

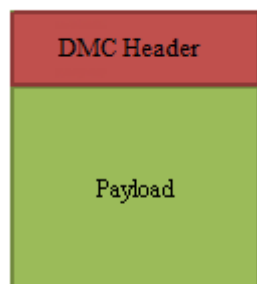
        uint8_t      reserved[10];                // Reserved
        uint32_t      numEntries;                // Number of valid entries in
the FWInfo array below
        struct _FWInfo_ {
            uint16_t    reserved1;                // Reserved
            char        stepping;                 // Stepping (A, B, C, ..., *).
* is a wildcard
            char        substepping;             // Sub-stepping (0, 1, ...,
*). * is a wildcard
            uint32_t    offset;                   // FW offset within the
package
            uint32_t    reserved2;               // Reserved
        } FWInfo[20];
    } PackageHeader;

```

DMC firmware binary

Each individual DMC firmware binary has a header followed by a payload whose size is specified in the header section. Along with the version, length, firmware size etc. the header section also specifies a list of MMIO addresses and data. These MMIO write cycles, in the 0x80000 - 0x8FFFF address range, should be executed as part of the initial CSR program setup.

DMC firmware Layout



```

for i = 1 to <mmioCount>
    Perform MMIO write to address <mmioaddr[i]> with data <mmiodata[i]>
typedef struct _DMCHdr {
    uint32_t    reserved;                // 0x40403E3E
    uint8_t     headerLen;               // DMC binary header length in bytes
    uint8_t     headerVer;               // 0x01
    uint16_t    dmccVer;                 // Reserved
    uint32_t    project;                 // Major, Minor

```




```
uint32_t    fwSize;                // Firmware program size (excluding header)
in dwords

uint32_t    fwVersion;            // Major Minor version

uint32_t    mmioCount;            // Number of valid MMIO cycles present in
the MMIO address and data arrays below.

uint32_t    mmioaddr[8];          // MMIO address

uint32_t    mmiodata[8];          // MMIO data

uint8_t     dfile[32];            // Reserved

uint32_t     reserved1[2];        // Reserved

} DMCHeader;
```

Sequences for Display C9

Display C9 (DC9) is a power saving state where the display engine is powered off.

Display software must follow certain programming sequences to allow or dis-allow DC9.

Hardware will dynamically enter and exit DC9 when allowed, saving and restoring some of the display state.

Note
Display C9 is supported on Broxton.

Sequence to Allow DC9

1. Follow Sequence to Disallow DC5
2. Disable all display engine functions using the full mode set disable sequence on all pipes, transcoders, ports, planes, and power well 2 (PG2).
3. Disable and mask all graphics interrupts in display.
 - If hotplug detection is needed during DC9, keep hotplug detection and its associated interrupts enabled and unmasked, and additionally enable and unmask the PCU Interrupt for DDI S0ix HPD. See Hotplug Detection During DC9.
4. Save state of MMIO display registers.
 - The exact registers depend on software policy.
 - Hardware will save and restore the PCI Config, DGunit registers, and hotplug related registers.
5. Follow Sequences to Initialize Display - Un-initialize Sequence.
6. Set DC_STATE_EN DC9 Allow to 1b.



Sequence to Disallow DC9

1. Clear DC_STATE_EN DC9 Allow to 0b.
2. Follow Sequences to Initialize Display - Initialize Sequence.
3. Restore state of MMIO display registers:
 - The exact registers depend on software policy.
4. Enable and unmask graphics interrupts as needed.

Hotplug Detection During DC9

Hotplug Detection (HPD) during DC9 requires special handling since the display engine hotplug detection logic is powered off.

If enabled by a BIOS configured register (DISPLAY_HPD_CTL at offset 1094h from base pmc_dev.BAR_HIGH,BAR), PMC will take over HPD when display engine is powered off, and detect a hotplug rising edge, falling edge, or any edge. Driver should determine whether HPD during DC9 is desired through BIOS VBT or some similar mechanism for OEM selection.

During DC9 hardware will dynamically transition between display engine powered on and off, so hotplug may be detected by PMC or display engine, and hardware will not reliably differentiate between short and long pulse hotplug events. If any kind of hotplug is detected, driver should use the HPD live state (Port Interrupt DDI Hotplug ISR) together with an AUX channel or GMBUS query to the receiver to determine if it was a connect, disconnect, or HPD_IRQ.

1. Display driver follows the Sequence to Allow DC9 with display engine hotplug detection logic enabled and the hotplug and DDI DC9 HPD interrupts enabled and unmasked.
2. When display is powered down, PMC wakes the system if it detects the selected edge type on the hotplug line.
3. The power controller unit forwards a DDI DC9 HPD interrupt to the display engine PCU Interrupt.
4. If the DDI DC9 HPD interrupt is enabled and unmasked, it triggers a graphics device interrupt. If it is disabled or masked, no interrupt happens and the system can re-enter DC9.
5. Display driver services the interrupt and determines if it was a connect, disconnect, or HPD_IRQ.
6. The display driver and operating system interpret the result and decide whether to disallow DC9 and enable a display output or do nothing.



Gen9 Display Resolution Support

A display resolution is only supported if it meets all the restrictions below for Maximum Pipe Pixel Rate, Maximum Port Link Rate, Maximum Memory Read Bandwidth, and Maximum Watermark.

Maximum Pipe Pixel Rate

The display resolution must fit within the maximum pixel rate output from the pipe. Make sure that the display pipe is able to feed pixels at a rate required to support the desired resolution.

For each enabled plane on the pipe {

 If plane scaling enabled {

 Horizontal down scale amount = $\text{Maximum}[1, \text{plane horizontal size} / \text{scaler horizontal window size}]$

 Vertical down scale amount = $\text{Maximum}[1, \text{plane vertical size} / \text{scaler vertical window size}]$

 Plane down scale amount = Horizontal down scale amount * Vertical down scale amount

 Plane Ratio = $1 / \text{Plane down scale amount}$

 }

 Else {

 Plane Ratio = 1

 }

 If plane source pixel format is 64 bits per pixel {

 Plane Ratio = $\text{Plane Ratio} * 8/9$

 }

}

Pipe Ratio = Minimum Plane Ratio of all enabled planes on the pipe

If pipe scaling is enabled {

 Horizontal down scale amount = $\text{Maximum}[1, \text{pipe horizontal source size} / \text{scaler horizontal window size}]$

 Vertical down scale amount = $\text{Maximum}[1, \text{pipe vertical source size} / \text{scaler vertical window size}]$

 Note: The progressive fetch - interlace display mode is equivalent to a 2.0 vertical down scale

 Pipe down scale amount = Horizontal down scale amount * Vertical down scale amount

 Pipe Ratio = $\text{Pipe Ratio} / \text{Pipe down scale amount}$

}

Pipe maximum pixel rate = CDCLK frequency * Pipe Ratio // See the display clocks section for the supported CDCLK frequencies.

Maximum Port Link Rate

The display resolution must fit within the maximum link rate for each port type.

Port Type	Maximum Link Bit Rate
eDP/DP	HBR2 5.4 GHz
HDMI	3 GHz
DVI	1.65 GHz
MIPI DSI	1.066 GHz

Maximum Memory Read Bandwidth

The display resolution must not exceed the available system memory bandwidth, considering factors like thermal throttling and bandwidth available for other memory clients.

For each pipe {

For each plane enabled on the pipe { // cursor can be ignored

Plane bandwidth MB/s = pixel rate MHz * source pixel format in bytes * plane down scale amount * pipe down scale amount

Total display bandwidth MB/s = Total display bandwidth + Plane bandwidth

}

}

Raw system memory bandwidth = (# of memory channels * memory frequency * 8 bytes)

If Total display bandwidth > system memory bandwidth available for display {Bandwidth is exceeded}

Programming Note	
Context:	Gen9 Display Resolution Support
Do not use more than 60% of raw system memory bandwidth for display.	

Maximum Watermark

The display resolution must not exceed the level 0 maximum watermark value. See the volume on Watermark Programming.



Display Resolution Capabilities

These are examples of common resolutions that meet all the resolution restrictions for up to 3 simultaneous displays, 4 primary or sprite planes with 32bpp pixel format, and 1 cursor, with no panel fitter down scaling.

Attribute	CD 624 MHz	CD 576 MHz	CD 384 MHz	CD 288 MHz	CD 144 MHz
eDP/DP x4 single stream	4096x2304 60Hz 24Bpp ⁴	4096x2160 60Hz 30Bpp ⁴	2880x1620 60Hz 30Bpp ²	4096x2160 30Hz 30Bpp ² 2560x1600 60Hz 30Bpp ¹	1920x1080 60Hz 30Bpp ¹
HDMI	Same as entry to the right	Same as entry to the right	4Kx2K 24-30Hz 24Bpp ²	1080p 59.94-60Hz 24Bpp ¹	720p 59.94-60Hz 24Bpp ¹
DVI	Same as entry to the right	Same as entry to the right	Same as entry to the right	1920x1200 60Hz 24Bpp ¹	1920x1080 60Hz 24Bpp ¹
MIPI DSI single link 1:1 compression	Same as entry to the right	Same as entry to the right	Same as entry to the right	1920x1200 60Hz 24Bpp ¹	1920x1080 60Hz 24Bpp ¹
MIPI DSI single link 2:1 compression	Same as entry to the right	Same as entry to the right	2880x1620 60Hz 24Bpp ²	2560x1600 60Hz 24Bpp ¹	Same as entry above
MIPI DSI single link 3:1 compression	Same as entry to the right	3200x2000 60Hz 24Bpp ³	Same as entry above	Same as entry above	Same as entry above
MIPI DSI dual link 1:1 compression	Same as entry to the right	Same as entry to the right	2880x1620 60Hz 24Bpp ²	2560x1600 60Hz 24Bpp ¹	1920x1080 60Hz 24Bpp ¹
MIPI DSI dual link 2:1 compression	4096x2304 60Hz 24Bpp ⁴	4096x2160 60Hz 24Bpp ⁴	Same as entry above	Same as entry above	Same as entry above
MIPI DSI dual link 3:1 compression	Same as entry above	Same as entry above	Same as entry above	Same as entry above	Same as entry above

Each entry is showing the highest common resolutions at that CD clock frequency step. Lower resolutions are also supported. Higher, less common, resolutions can also work, but need to be calculated individually.

eDP, DP, DVI, and MIPI DSI are calculated using CVT 1.2 RB1 blanking and pixel rate.

HDMI is calculated using HDMI specification blanking and pixel rate.

Bpp is referring to the port output bits per pixel.

¹Requires at least single channel DDR3 1333 for 3 simultaneous displays

²Requires at least single channel DDR3 1600 for 3 simultaneous displays

³Requires at least dual channel DDR3 1333 for 3 simultaneous displays

⁴Requires at least dual channel DDR3 1600 for 3 simultaneous displays

Examples

Example pipe pixel rate:

Plane 1 enabled at 32bpp, plane 2 enabled at 16bpp, pipe scaling enabled and down scale amount 1.12, and CDCLK 450 MHz:

Plane 1 ratio = 1

Plane 2 ratio = 1

Pipe ratio = Minimum[1, 1] = 1

Pipe ratio = $1/1.12 = 0.89$

Pipe maximum pixel rate = $450 \text{ MHz} * 0.89 = 400.5 \text{ MHz}$

Example pipe pixel rate:

Plane 1 enabled at 64bpp and plane down scale amount 1.25, plane 2 enabled at 32bpp, no panel fitting enabled, and CDCLK 540 MHz:

Plane 1 ratio = $1/1.25 * 8/9 = 0.71$

Plane 2 ratio = 1

Pipe ratio = Minimum[1, 0.71] = 0.71

Pipe maximum pixel rate = $540 \text{ MHz} * 0.71 = 383.4 \text{ MHz}$

Example memory bandwidth:

System memory bandwidth available for display = 4000 MB/s

Pipe A - Plane 1 enabled at 32bpp, plane 2 enabled at 16bpp, scaling disabled, pixel rate 148.5 MHz

Pipe B - Plane 1 enabled at 32bpp, scaling disabled, pixel rate 148.5 MHz

Pipe C - Plane 1 enabled at 32bpp, scaling disabled, pixel rate 148.5 MHz

Pipe A - Plane 1 bandwidth = $148.5 * 4 \text{ bytes} = 594 \text{ MB/s}$

Pipe A - Plane 2 bandwidth = $148.5 * 2 \text{ bytes} = 297 \text{ MB/s}$

Pipe B - Plane 1 bandwidth = $148.5 * 4 \text{ bytes} = 594 \text{ MB/s}$

Pipe C - Plane 1 bandwidth = $148.5 * 4 \text{ bytes} = 594 \text{ MB/s}$

Total display bandwidth = $594 + 297 + 594 + 594 = 2079 \text{ MB/s}$

System memory bandwidth available for display not exceeded

Example memory bandwidth:

System memory bandwidth available for display = 4000 MB/s

Pipe A - Plane 1 enabled at 32bpp, plane 2 plane enabled at 32bpp, pipe scaling enabled and down scale amount 1.12, pixel rate 414.5 MHz



Pipe B - Plane 1 enabled at 32bpp, scaling disabled, pixel rate 414.5 MHz

Pipe C - Plane 1 enabled at 32bpp, scaling disabled, pixel rate 414.5 MHz

Pipe A - Plane 1 bandwidth = $414.5 * 4 \text{ bytes} * 1.12 = 1863 \text{ MB/s}$

Pipe A - Plane 2 bandwidth = $414.5 * 4 \text{ bytes} * 1.12 = 1863 \text{ MB/s}$

Pipe B - Plane 1 bandwidth = $414.5 * 4 \text{ bytes} = 1658 \text{ MB/s}$

Pipe C - Plane 1 bandwidth = $414.5 * 4 \text{ bytes} = 1658 \text{ MB/s}$

Total display bandwidth = $1863 + 1863 + 1658 + 1658 = 7042 \text{ MB/s}$

System memory bandwidth available for display **exceeded**

Clocks

Broxton Clocks

Registers

CDCLK_CTL

DE_PLL_CTL

DE_PLL_ENABLE

MIPI_CLOCK_CTL

DSI_PLL_CTL

DSI_PLL_ENABLE

PORT_PLL_PCS_0

PORT_PCS_DW12

PORT_PLL_EBB_0

PORT_PLL_EBB_4

PORT_PLL_0

PORT_PLL_1

PORT_PLL_2

PORT_PLL_3

PORT_PLL_6

PORT_PLL_8

PORT_PLL_9

PORT_PLL_10

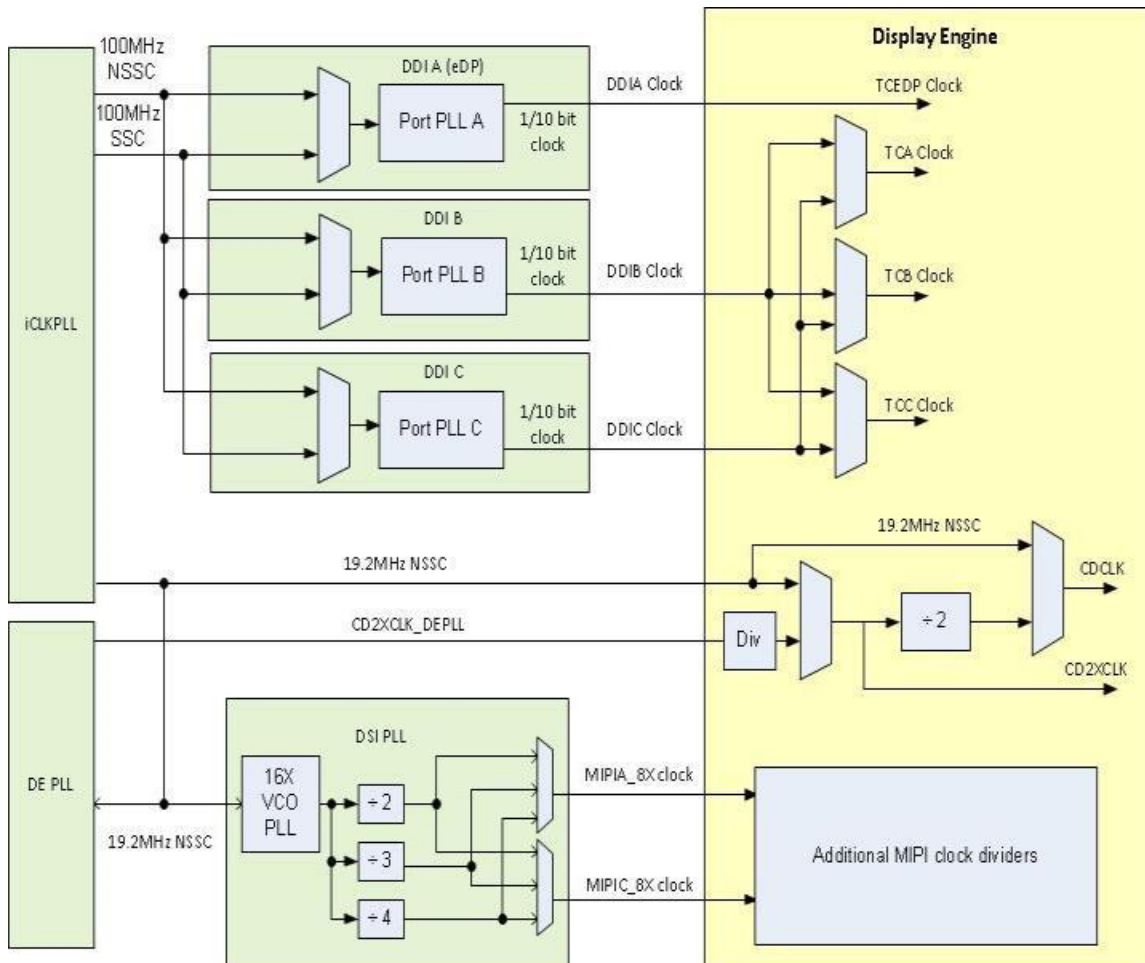
PORT_PLL_ENABLE

TRANS_CLK_SEL

TIMESTAMP_CTR

Overview of Display Clock Paths

The display engine clocking structure has multiple PLLs and clocks. The flow is from reference to PLL/DDI (port) clock to transcoder clock.





Display Engine Clock Reference

There are three display engine clock references.

	100 MHz Non-SSC (NSSC) Reference	100 MHz SSC Reference	19.2 MHz Non-SSC Reference
Usage	Non-spread spectrum reference for the port DDI PLLs	Spread spectrum reference for the port DDI PLLs	Reference for the DE PLL and DSI PLL
Frequency	100 MHz	100 MHz	19.2 MHz
Default after reset	Enabled	Enabled	Enabled
Programming	Not programmable by display software.	Not programmable by display software.	Not programmable by display software.

Display Engine PLLs

	DE PLL	PORT PLL A, PORT PLL B, PORT PLL C	DSI PLL
Usage	Source for CD clock	Sources for DDI clocks	Source for MIPI clocks
Input	19.2 MHz Non-SSC reference	100 MHz SSC and Non-SSC references	19.2 MHz Non-SSC reference
Frequency	Programmable 1152, 1248 MHz	Programmable eDP link rates: 1.62, 2.16, 2.43, 2.7, 3.24, 4.32, 5.4 GHz SSC and Non-SSC DP link rates: 1.62, 2.7, 5.4 GHz SSC and Non-SSC HDMI/DVI link rates: 0.2 to 3.0 GHz Non-SSC* *2.233 - 2.4 GHz not supported	Programmable 8X frequency: 0.288 to 1.06 GHz Non-SSC
Default after reset	Disabled	Disabled	Disabled
Programming	Enable and frequency must be programmed by software when enabling and disabling any display. May be automatically enabled and disabled by hardware for some power states.	Enable and frequency must be programmed by software when enabling and disabling a HDMI/DVI or DisplayPort display. May be automatically enabled and disabled by hardware for some power states.	Enable and frequency must be programmed by software when enabling and disabling a MIPI display. May be automatically enabled and disabled by hardware for some power states.

DDI Clocks

There is one DDI clock tied to each DDI port.

A single DDI clock output may be used by multiple transcoders simultaneously for DisplayPort Multi-streaming.

	DDI clocks A, B, C
Usage	DDI ports I/O bit clock and symbol/TMDS clock, source for transcoder clocks
Input	The associated Port PLL
Frequency	Port PLL frequency
Default after reset	Disabled
Programming	Not programmable

Transcoder Clocks

There is one Transcoder clock tied to each display transcoder, except Transcoder WD which uses only CD clock.

	Transcoder clock EDP	Transcoder clocks A, B, C	Transcoder clocks MIPI1 (MIPI A), MIPI2 (MIPI C)
Usage	Transcoder EDP symbol clock	Transcoders A, B, and C symbol/TMDS clocks	Transcoder MIPI clocks
Input	Always uses DDI A clock	Programmable selection between DDI clocks B, and C.	Always uses associated MIPI DSI output clock
Frequency	PLL output frequency divided by 5	PLL output frequency divided by 5	Multiple options from additional dividers in display engine
Default after reset	Connected to DDI A Clock	Disabled	Connected to DSI Clock
Programming	Not programmable.	Mapping of DDI to Transcoder must be programmed by software when enabling and disabling a display. Programming is done through the TRANS_CLK_SEL registers.	Dividers must be programmed by software when enabling and disabling a display. Programming is done through the MIPI_CLOCK_CTL registers.



CD Clock

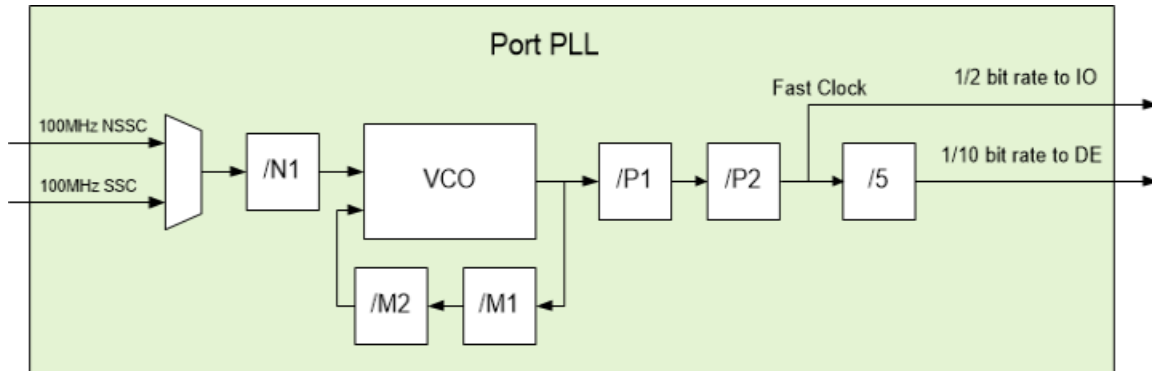
CD clock refers to the Core Display clock which includes the Core Display 1X Clock (CD clock, CDclk, cdclk, CDCLK) and the Core Display 2X Clock (CD2X clock, cd2xclk, CD2XCLK).

	CD clock
Usage	Clocking for most display engine functions
Input	DE PLL output (with two frequency options) or iCLKPLL 19.2 MHz reference. iCLKPLL 19.2 MHz is automatically selected by hardware when Power Well #1 is disabled or DE PLL is not locked.
Frequency	iCLKPLL (DE PLL disabled) - 19.2 MHz CD, 19.2 MHz CD2X DE PLL with output 1152 MHz • 144 MHz CD, 288 MHz CD2X • 288 MHz CD, 576 MHz CD2X • 384 MHz CD, 768 MHz CD2X • 576 MHz CD, 1152 MHz CD2X DE PLL with output 1248 MHz • 624 MHz CD, 1248 MHz CD2X
Default after reset	Running on the 19.2 MHz Non-SSC reference
Programming	CD clock frequency must be programmed by software when enabling and disabling a display. Programming is done through the CDCLK_CTL and DE_PLL_CTL registers. The CD clock frequency may be changed on the fly in certain cases. Follow the Sequences for Changing CD Clock Frequency..

Recommended CD Clock Frequency Selection

In order to save power, software should use the lowest CD clock frequency necessary to support the current display configuration. Software may use a higher CD clock frequency if desired to reduce the cases where an already enabled display has to be disabled and re-enabled to change CD clock frequency when a second or third display is enable or disabled.

Port PLL Formula for Divider Values



eDP link rates: 1.62, 2.16, 2.43, 2.7, 3.24, 4.32, 5.4 GHz SSC and Non-SSC

DP link rates: 1.62, 2.7, 5.4 GHz SSC and Non-SSC

HDMI/DVI link rates: 0.2 to 3.0 GHz Non-SSC

Desired Output = Port bit rate in MHz (DisplayPort HBR2 is 5400 MHz)

Fast Clock = Desired Output / 2

$VCO = \text{Fast Clock} * P1 * P2$

P1 must be 2, 3, or 4

P2 must be 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, or 20 (1 to 20, even numbers when greater than 10)

VCO must be in the range 4800 to 6700

$M2 = VCO / (M1 * \text{Reference Clock} / N)$

M1 must be 2

N must be 1

Reference Clock must be 100 MHz

With the fixed values for M1, N, and reference clock, the formulas reduce to the following:

$M2 = \text{Desired Output} * P1 * P2 / 400$

$VCO = M2 * 200$

Actual Output = $M2 * 400 / (P1 * P2)$ // Actual differs from desired due to limited M2 fractional precision



Note: If the desired output frequency cannot be achieved with the valid values of P1, P2, and M2, use a different screen resolution with a different output frequency.

Port PLL Algorithm to Find Divider Values

1. Try all valid values of P1 and P2
2. Calculate M2 for the P1, P2, and Desired Output
3. Adjust M2 for 22 bit fractional precision
4. Calculate VCO for the adjusted M2
5. Find if VCO is valid
6. Find the actual output frequency from the adjusted M2 and calculate the error PPM
7. Program PLL registers with the P1, P2, and M2 that had the lowest error and highest value of P1 * P2.

For P1 = (4,3,2)

For P2 = (20,18,16,14,12,10,9,8,7,6,5,4,3,2,1)

$$M2 = (\text{Desired Output} * P1 * P2) / 400$$

$$M2 = \text{ROUNDUP}(2^{22} * M2) / 2^{22}$$

$$\text{VCO} = M2 * 200$$

If $(\text{VCO} \geq 4800)$ AND $(\text{VCO} < 6700)$

$$\text{Actual Output} = M2 * 400 / (P1 * P2)$$

$$\text{Error} = \text{Actual Output} - \text{Desired Output}$$

$$\text{PPM} = 1,000,000 * \text{Error} / \text{Desired Output}$$

If $\text{PPM} < 100$ And $(P1 * P2) > (\text{Best P1} * \text{Best P2})$

$$\text{Best PPM} = 0$$

$$\text{Best M2} = M2$$

$$\text{Best P1} = P1$$

$$\text{Best P2} = P2$$

End If

If $\text{PPM} < (\text{Best PPM} - 10)$

$$\text{Best PPM} = \text{PPM}$$

$$\text{Best M2} = M2$$

$$\text{Best P1} = P1$$

$$\text{Best P2} = P2$$

End If

End If

Next P2

Next P1

Best M2 Integer = INT(Best M2)

Best M2 Fraction = ROUNDUP($2^{22} * (\text{Best M2} - \text{Best M2 Integer})$)

Port PLL Example Divider Values

DisplayPort HBR2

Desired Output = 5400

Resulting P1=2, P2=1, and M2=27

Actual Output = 5400

Error PPM = 0

Program P1=2, P2=1, M2 Integer=27, M2 Fraction=0, and M2 Fraction Enable=0

HDMI 297 MHz

Desired Output = 2970

Resulting P1=4, P2=1, and M2=29.7

Actual Output = 2970.00000476837158203125

Error PPM = 0.0016

Program P1=4, P2=1, M2 Integer=29, M2 Fraction=2936013, and M2 Fraction Enable=1

PORT_PLL_6, PORT_PLL_8, and PORT_PLL_10 Values

These registers are programmed based on the frequency band.

The values in the table are decimal.

PLL VCO in GHz	i_prop_coeff	i_gainctrl	i_int_coeff	i_tdc_targetcnt	i_dcoampovrden_h	i_dcoamp
$6.2 \leq \text{VCO} \leq 6.7$	4	3	9	8	1	15
$5.4 < \text{VCO} < 6.2$	5	3	11	9	1	15
$5.4 = \text{VCO}$	3	1	8	9	1	15
$4.8 \leq \text{VCO} < 5.4$	5	3	11	9	1	15



Lane Stagger Values

Port symbol rate (bit rate/10) in MHz	Lane Stagger (hex)
270 < symbol rate ≤ 540	0x18
135 < symbol rate ≤ 270	0x0D
67 < symbol rate ≤ 135	0x07
33 < symbol rate ≤ 67	0x04
25 ≤ symbol rate ≤ 33	0x02

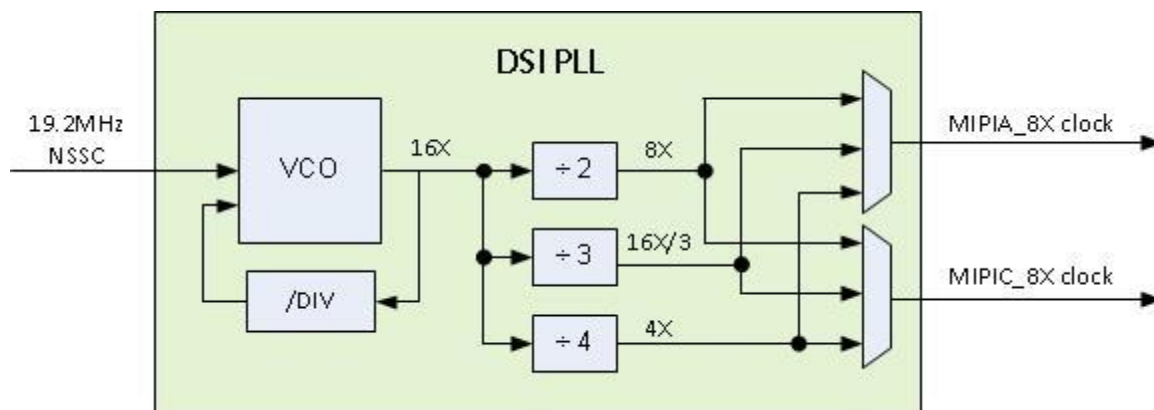
Port PLL Enabling Sequence

Step	Register	Programming	Comments
1	PORT_PLL_ENABLE	Write reference select	Select SSC or Non-SSC
2	PORT_PLL_EBB_4	Write 0 to o_dtdclkpen_h	Disable 10 bit clock to display engine
3	PORT_PLL_EBB_0	Write P1 to o_dtp1divsel Write P2 to o_dtp2divsel	
4	PORT_PLL_0	Write M2 integer portion to i_fbdivratio	INT(M2)
5	PORT_PLL_1	Write N to i_ndivratio	N is always 1
6	PORT_PLL_2	Write M2 fraction portion to i_fracdiv	ROUNDUP($2^{22} * (M2 - INT(M2))$)
7	PORT_PLL_3	Write M2 fraction enable to i_fracnen_h	M2 fraction enable = 1 if M2 fraction != 0
8	PORT_PLL_6	Write proportional coefficient to i_prop_coeff Write integral coefficient to i_int_coeff Write gain control to i_gainctrl	Values depend on frequency band
9	PORT_PLL_8	Write calibration value to i_tdctargetcnt	Values depend on frequency band
10	PORT_PLL_9	Write 5 to i_lockthresh	
11	PORT_PLL_10	Write DCO amplitude override value to i_dcoamp Write DCO amplitude override enable to i_dcoampovrden_h	Values depend on frequency band
12	PORT_PLL_EBB_4	Write 1 to o_dtafcrecal	Recalibrate with new settings
13	PORT_PLL_EBB_4	Write 1 to o_dtdclkpen_h	Enable 10 bit clock to display engine
14	PORT_PLL_ENABLE	Write 1 to PLL enable	Enable PLL
15	PORT_PLL_ENABLE	Poll for PLL lock = 1	Poll for lock
16	PORT_PCS_DW12 (use GRP instance)	Write lane stagger to reg_lanestagger_strap Write 1 to reg_lanestagger_strp_ovrd	Values depend on frequency band

Port PLL Disabling Sequence

1. Write 0 to PORT_PLL_ENABLE PLL enable
2. Poll PORT_PLL_ENABLE for PLL lock = 0
3. Timeout and fail if not unlocked after 200 us

MIPI DSI PLL



The MIPI DSI PLL block outputs the MIPI A 8X clock and MIPI C 8X clock.

A programmable divider controls the PLL 16X clock frequency, which goes through three other dividers in parallel to generate the outputs.

The DSI A clock and DSI C clock come from the 16X clock after being divided by 2 (8X), 3 (16X/3), or 4 (4X).

Example Ratios and Corresponding Frequencies (MHz)

Ratio	8X Clk	16X/3 Clk	4X Clk
34	326.4	217.6	163.2
35	336	224	168
40	384	256	192
45	432	288	216
50	480	320	240
55	528	352	264
57	547.2	364.8	273.6
60	576	384	288
63	604.8	403.2	302.4
65	624	416	312
70	672	448	336
75	720	480	360
80	768	512	384
85	816	544	408



90	864	576	432
95	912	608	456
100	960	640	480
110	1056	704	528
111	1065.5	710.4	532.8
125	1200	800	600

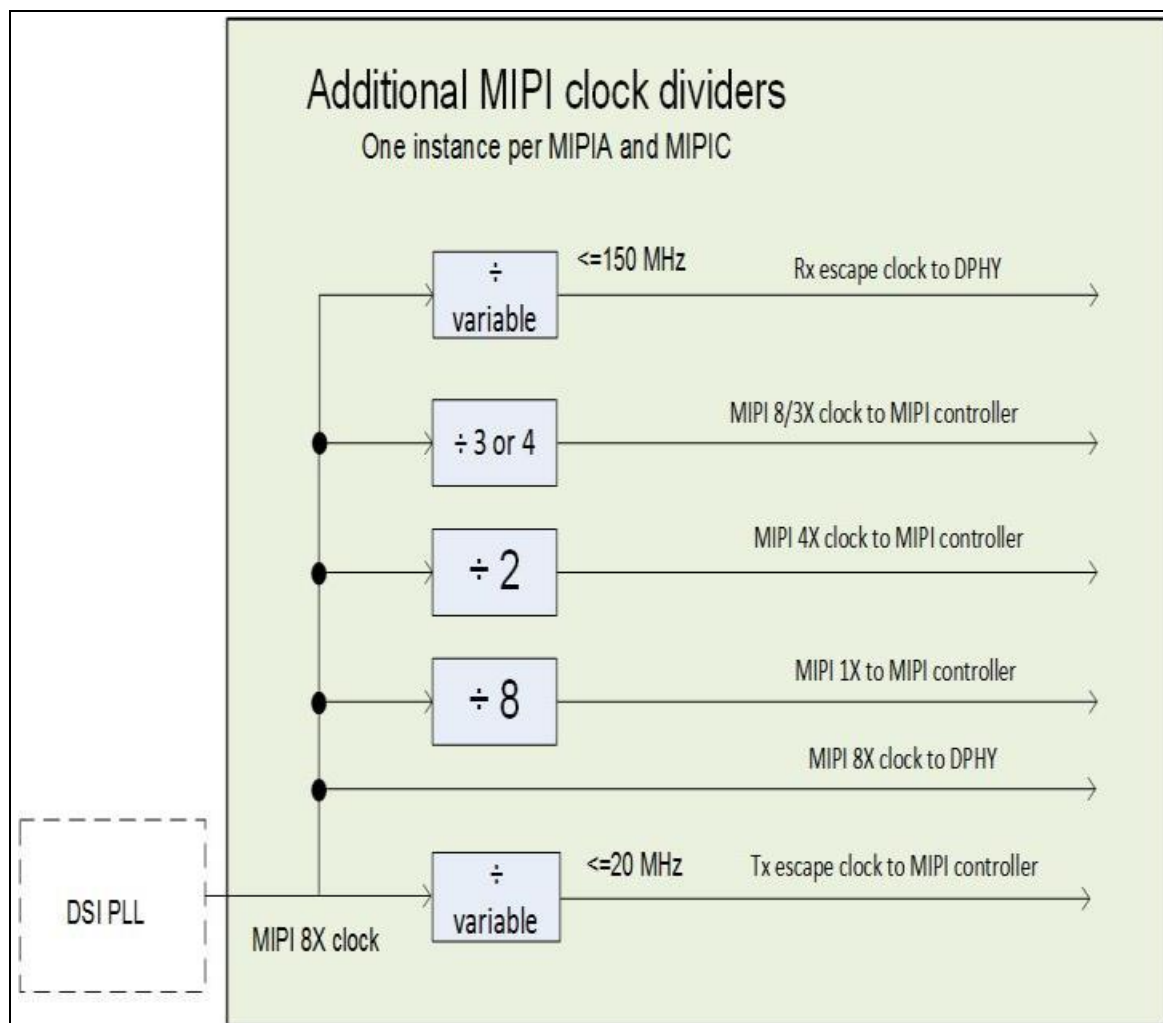
MIPI DSI PLL Enabling Sequence

1. Write DSI_PLL_CTL with the PLL ratio and output divider selections for DSI A and DSI C
 - Both output dividers must be programmed to valid values any time the PLL is enabled, even if only one output is used.
 - The dividers cannot be changed while the PLL is enabled.
2. Write 1 to DSI_PLL_ENABLE PLL enable
3. Poll DSI_PLL_ENABLE for PLL lock = 1
4. Timeout and fail if not locked after 200 us

MIPI DSI PLL Disabling Sequence

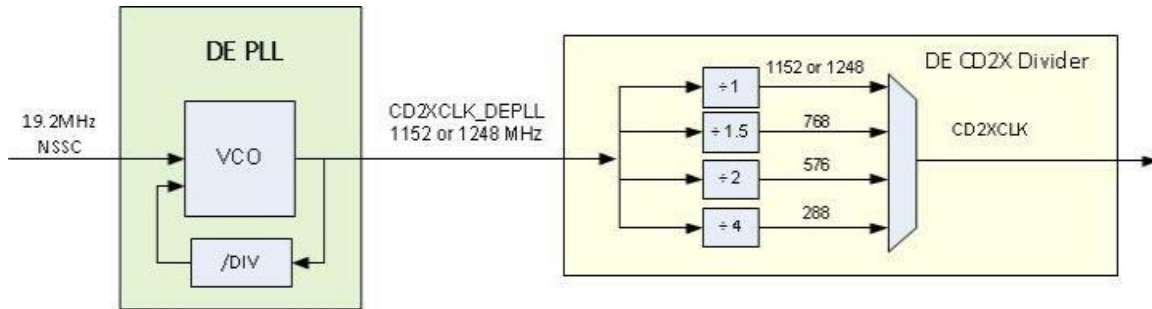
1. Write 0 to DSI_PLL_ENABLE PLL enable
2. Poll DSI_PLL_ENABLE for PLL lock = 0
3. Timeout and fail if not unlocked after 200 us

MIPI Additional Clock Dividers



The additional MIPI clock dividers further divide the MIPI PLL 8X clock to create the different clocks for the controller and I/O PHY. The dividers are programmed through the MIPI_CLOCK_CTL register and must follow the restrictions there.

DE PLL



The DE PLL outputs the CD2X DE PLL clock which is the source for CD clock.

A programmable divider, controlled by the DE_PLL_CTL register, inside the PLL controls the PLL frequency. The DE PLL CD2X Divider outside the PLL, controlled by the CDCLK_CTL register, provides additional dividing to create the CD2X clock used by the display engine.

Supported Ratios and Corresponding Frequencies (MHz)

DE PLL Ratio	DE CD2X Frequency	DE CD2X Divide	CD2XCLK	CDCLK
65	1248	1	1248	624
60	1152	1	1152	576
60	1152	1.5	768	384
60	1152	2	576	288
60	1152	4	288	144

DE PLL Sequences

- Follow the Broxton Sequences for Changing CD Clock Frequency

Broxton Sequences for Changing CD Clock Frequency

Restrictions
The CD clock frequency impacts the maximum supported pixel rate and display watermark programming. The CD clock frequency must be at least twice the frequency of the Azalia BCLK. Frequency changes required display to be disabled, except if only the DE CD2X Divider is changed.

Sequence for Changing CD Clock Frequency

1. Unless changing only the DE PLL CD2X Divider, disable all display engine functions using the full mode set disable sequence on all pipes, ports, and planes.
 - Includes Global Time Code
 - Display power wells may be left enabled
2. Inform power controller of upcoming frequency change
 - a. Ensure any previous GT Driver Mailbox transaction is complete.
 - b. Write GT Driver Mailbox Data Low = 0x80000000.
 - c. Write GT Driver Mailbox Interface = 0x80000017.
 - d. Poll GT Driver Mailbox Interface for Run/Busy indication cleared (bit 31 = 0).
 - e. Timeout after 150 us. Do not change CD clock frequency if there is a timeout.
3. Enable or change the frequency of CD clock
 - a. If enabling DE PLL
 - i. Write DE_PLL_CTL with the PLL ratio
 - ii. Set DE_PLL_ENABLE PLL Enable
 - iii. Poll DE_PLL_ENABLE for PLL lock
 - iv. Timeout and fail if not locked after 200 us
 - v. Write CDCLK_CTL with the DE PLL CD2X Divider selection, CD Frequency Decimal value, and SSA Precharge Enable to match the desired CD clock frequency
 - b. If disabling DE PLL
 - i. Clear DE_PLL_ENABLE PLL Enable
 - ii. Poll DE_PLL_ENABLE for PLL unlocked
 - iii. Timeout and fail if not unlocked after 200 us
 - c. If changing the DE PLL frequency
 - i. Follow steps above for disabling DE PLL
 - ii. Follow steps above for enabling DE PLL, using the new PLL ratio
 - d. If changing only the DE PLL CD2X Divider



- i. Write CDCLK_CTL with the DE CD2X Pipe selectoin, DE PLL CD2X Divider selection, CD Frequency Decimal value, and SSA Precharge Enable to match the desired CD clock frequency
 - ii. If pipe is enabled, wait for start of vertical blank for change to take effect
 4. Inform power controller of the selected frequency
 - Use 19.2 MHz for the frequency if DE PLL is disabled
 - a. Write GT Driver Mailbox Data Low with Ceiling[CDCLK frequency / 25].
 - For CD clock 19.2 MHz (DE PLL disabled), program 1 decimal.
 - For CD clock 79.2 MHz, program 4 decimal.
 - For CD clock 144 MHz, program 6 decimal.
 - For CD clock 288 MHz, program 12 decimal.
 - For CD clock 384 MHz, program 16 decimal.
 - For CD clock 576 MHz, program 24 decimal.
 - For CD clock 624 MHz, program 25 decimal.
 - For CD clock 156 or 158.4 MHz, program 7 decimal.
 - For CD clock 312 or 316.8 MHz, program 13 decimal.
 - b. Write GT Driver Mailbox Interface = 0x80000017.
 - There is no need to wait for the Run/Busy indication to be cleared before continuing with display programming.
 5. Update programming of functions that use the CD clock frequency
- If these features are not currently enabled, the programming can be delayed to when they are enabled.

- Wireless Display 27 MHz frequency in the WD_27_M and WD_27_N registers.
 - For CD clock 79.2 MHz, program M=15 and N=44 (decimal).
 - For CD clock 158.4 MHz, program M=15 and N=88 (decimal).
 - For CD clock 316.8 MHz, program M=15 and N=176 (decimal).
 - For CD clock 144 MHz, program M=3 and N=16 (decimal).
 - For CD clock 288 MHz, program M=3 and N=32 (decimal).
 - For CD clock 384 MHz, program M=9 and N=128 (decimal).
 - For CD clock 576 MHz, program M=3 and N=64 (decimal).
 - For CD clock 624 MHz, program M=9 and N=208 (decimal).
 - For CD clock 156 MHz, program M=9 and N=52 (decimal).
 - For CD clock 312 MHz, program M=9 and N=104 (decimal).



Resets

NDE_RSTWRN_OPT

The north and south display engines are reset by PCI Function Level Resets (FLR) and the chip level resets.

An FLR for Bus:Device:Function 0:2:0 resets the north and south display engines and audio codec and most of the related MMIO, PCI, and I/O configuration registers.

Display configuration registers that are reset by both the chip level reset and by FLR are marked as using the "soft" reset in the programming specification.

Display configuration registers that are reset only by the chip level reset and *not* by FLR are marked as using the "global" reset in the programming specification.

The south display engine runs panel power down sequencing (if configured to do so) before resetting.

This additional programming is needed to bring the display engine to the cold boot state after the FLR for Bus:Function:Device 0:2:0 completes. This is optional if software can tolerate display not being in the cold boot state after FLR.

1. Disable PWR_WELL_CTL Power Well 2 Request
2. Clear both PHY_CTL_FAMILY_EDP and PHY_CTL_FAMILY_DDI Common Reset to 0b (Disable)
3. Clear P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR to 0x0
4. Disable PWR_WELL_CTL Power Well 1 Request

**DGunit Registers (DGR)**

Address Space	Address	Name
MMIO: 0/2/0	03000h	IOMMU_DEFEATURE_CAPECAPDIS
MMIO: 0/2/0	03004h	IOMMU_DEFEATURE_TLBDIS
MMIO: 0/2/0	03008h	IOMMU_DEFEATURE_PWSWTRDIS
MMIO: 0/2/0	0300Ch	IOMMU_DEFEATURE_MISCDIS
MMIO: 0/2/0	03010h	IOMMU_DEFEATURE_PWRDNOVRD
MMIO: 0/2/0	030B0h	GT_RELOAD_FLUSH
MMIO: 0/2/0	030C0h	GT_FLUSH_BCLD_ACK
MMIO: 0/2/0	04CD8h	PRMRR_BASE_LSB
MMIO: 0/2/0	04CDCh	PRMRR_BASE_MSB
MMIO: 0/2/0	04CE0h	PRMRR_MASK_LSB
MMIO: 0/2/0	04CE4h	PRMRR_MASK_MSB
MMIO: 0/2/0	06C88h	MCHBAR_LSB
MMIO: 0/2/0	06C8Ch	MCHBAR_MSB
MMIO: 0/2/0	100000h - 1000F8h	FENCE 0-31 LSB
MMIO: 0/2/0	100004h - 1000FCh	FENCE 0-31 MSB
MMIO: 0/2/0	100100h	DPFC_CONTROL_SA
MMIO: 0/2/0	100104h	DPFC_CPU_FENCE_OFFSET
MMIO: 0/2/0	101000h	TILECTL
MMIO: 0/2/0	101008h	GFX_FLSH_CNT
MMIO: 0/2/0	10102Ch	DISPLAY_DEADLINE_CONTROL
MMIO: 0/2/0	108000h	MTOLUD

Address Space	Address	Name
MMIO: 0/2/0	108040h	MMIO Mirror of GMCH Graphics Control Register (MGGC)
MMIO: 0/2/0	108080h	MTOUUD_LSB
MMIO: 0/2/0	108084h	MTOUUD_MSB
MMIO: 0/2/0	1080C0h	MBDSM
MMIO: 0/2/0	108100h	MBGSM
MMIO: 0/2/0	108140h	Base of DMA Protected Range
MMIO: 0/2/0	108180h	MPMEN
MMIO: 0/2/0	1081C0h	MPLMBASE
MMIO: 0/2/0	108200h	MPLMLIMIT
MMIO: 0/2/0	108240h	MPHMBASE_LSB
MMIO: 0/2/0	108244h	MPHMBASE_MSB
MMIO: 0/2/0	108280h	MPHMLIMIT_LSB
MMIO: 0/2/0	108284h	MPHMLIMIT_MSB
MMIO: 0/2/0	108300h	MGCMD
MMIO: 0/2/0	108340h	MEMRR_BASE_LSB
MMIO: 0/2/0	108344h	MEMRR_BASE_MSB
MMIO: 0/2/0	108380h	MEMRR_MASK_LSB
MMIO: 0/2/0	108384h	MEMRR_MASK_MSB
MMIO: 0/2/0	110000h	SVM_DEV_MODE_CNFG
MMIO: 0/2/0	120004h	GTACK
MMIO: 0/2/0	120800h	MAILBOX0
MMIO: 0/2/0	120804h	MAILBOX1



Address Space	Address	Name
MMIO: 0/2/0	120808h	MAILBOX2
MMIO: 0/2/0	12080Ch	MAILBOX3
MMIO: 0/2/0	124810h	FLT_RPT0
MMIO: 0/2/0	124814h	FLT_RPT1
MMIO: 0/2/0	124818h	FLT_RPT2
MMIO: 0/2/0	12481Ch	FLT_RPT3
MMIO: 0/2/0	124820h	PPRO
MMIO: 0/2/0	124824h	PPPR
MMIO: 0/2/0	124830h	RTADDR_LSB
MMIO: 0/2/0	124834h	RTADDR_MSB

Fuses and Straps

DFSERROR

Hot Plug Detection

Broxton Hot Plug Detection

HOTPLUG_CTL

HPD_PULSE_CNT

HPD_FILTER_CNT

For hot plug detection during Display C9 (DC9), see Broxton Sequences for Display C9.

Broxton 0 and Broxton 1 Board Mapping for A Stepping

HPD Pin Name in Display Engine	Die Bump Name	Board Connection
DDI A HPD	DDI0_HPDP	DP/HDMI HPD
DDI B HPD	DDI1_HPDP	Not connected
DDI C HPD	DDI2_HPDP	EDP HPD

The board connections do not match the internal assignments, so software must remap how it assigns the HPDs. Software needs to activate the DDI A HPD logic and interrupts in order to check the external panel connection, and enable the DDI C HPD logic and interrupts in order to check the eDP panel connection. PSR on eDP will not automatically exit when there is a short pulse HPD_IRQ from the eDP panel. Software should set the PSR_MASK register Mask Hotplug field to prevent false PSR exits caused by the external panel.

Broxton 0 and Broxton 1 Board Mapping for E Stepping and Later

HPD Pin Name in Display Engine	Die Bump Name	Board Connection
DDI A HPD	DDI2_HPDP	EDP HPD
DDI B HPD	DDI0_HPDP	DP/HDMI HPD
DDI C HPD	DDI1_HPDP	Not connected

Broxton P Board Mapping

HPD Pin Name in Display Engine	Die Bump Name	Board Connection
DDI A HPD	DDI2_HPDP	EDP HPD
DDI B HPD	DDI0_HPDP	DP/HDMI HPD
DDI C HPD	DDI1_HPDP	DP/HDMI HPD

Backlight

This section refers to the CPU display backlight control. For PCH display backlight control, see South Display Engine Registers.

The backlight PWM output frequency is determined by the PWM clock frequency, increment, and frequency divider.

PWM output frequency = PWM clock frequency / PWM increment / PWM frequency divider



The frequency divider must be greater than or equal to the number of brightness levels required by software; typically 100 or 256.

Description
PWM clock frequency = 19.2 MHz PWM increment = 1 PWM frequency divider maximum = 2^{32} PWM output frequency range with PWM clock frequency 19.2 MHz and 100 brightness levels = 0.0004 to 192,000 Hz PWM output frequency range with PWM clock frequency 19.2 MHz and 256 brightness levels = 0.0004 to 75,000 Hz

Backlight Enabling Sequence

Description
1. Set frequency and duty cycle in BLC_PWM_FREQ Frequency and BLC_PWM_DUTY Duty Cycle. 2. Enable PWM output and set polarity in BLC_PWM_CTL PWM Enable and PWM Polarity. Polarity can be programmed earlier if needed ... 3. Change duty cycle as needed in BLC_PWM_DUTY Duty Cycle.

If needed, granularity and polarity can be programmed earlier than shown.

Backlight Registers

Description
BLC_PWM_CTL BLC_PWM_FREQ BLC_PWM_DUTY Backlight 2 BLC_PWM_*_2 uses the display utility pin for output. To use backlight 2, enable the utility pin with mode = PWM.

Panel Power

PP_STATUS

PP_CONTROL

PP_ON_DELAYS

PP_OFF_DELAYS

GMBUS and GPIO

Registers

GPIO_CTL - GPIO Control

GMBUS0 - GMBUS Clock/Port Select

GMBUS1 - GMBUS Command/Status

GMBUS2 - GMBUS Status

GMBUS3 - GMBUS Data Buffer

GMBUS4 - GMBUS Interrupt Mask

GMBUS5 - GMBUS 2 Byte Index

Pin Usage

These GPIO pins allow the support of simple query and control functions such as DDC interface protocols. The GMBUS controller can be used to run the interface protocol, or the GPIO pins can be manually programmed for a "bit banging" interface.

The following table describes the expected GPIO pin to register mapping. OEMs have the ability to remap these functions onto other pins as long as the hardware limitations are observed. The GPIO pins may also be muxed with other functions such that they are only available when the other function is not being used.

Port #	Name	Pull up/down	Description
1	DDIB CTLDATA	No (Weak pull down on reset)	DDC for DDI port B.
	DDIB CTLCLK	No	
2	DDIC CTLDATA	No (Weak pull down on reset)	DDC for DDI port C.
	DDIC CTLCLK	No	
3	MISC CTLDATA	No (Weak pull down on reset)	DDC for Miscellaneous usage.
	MISC CTLCLK	No	

Broxton 0 and Broxton 1 Board Mapping

DDI Name in Display Engine	Die Bump Name	Board Connection
DDIB CTLDATA	DDIO_DDC_SDA	DP/HDMI DDC Data
DDIB CTLCLK	DDIO_DDC_SDA	DP/HDMI DDC Clock



DDI Name in Display Engine	Die Bump Name	Board Connection
DDIC CTLDATA	DDI1_DDC_SDA	Not connected
DDIC CTLCLK	DDI1_DDC_SCL	Not connected
MISC CTLDATA	DBI_SDA	MIPI external LVDS/CRT Converter DDC Data
MISC CTLCLK	DBI_SCL	MIPI external LVDS/CRT Converter DDC Clock

DDI C is not connected on the current die, but may be connected in the future.

GMBUS Controller Programming Interface

The GMBUS (Graphic Management Bus) is used to access/control devices connected to the GPIO pins.

Basic features:

1. I²C compatible.
2. Bus clock frequency of 50 KHz or 100 KHz.
3. Attaches to any of the GPIO pin pairs.
4. 7-bit or 10-bit Slave Address and 8-bit or 16-bit index.
5. Double buffered data register and a 9 bit counter support 0 byte to 256 byte transfers.
6. Supports stalls generated by the slave device pulling down the clock line (Slave Stall), or delaying the slave acknowledge response.
7. Status register indicates error conditions, data buffer busy, time out, and data complete acknowledgement.
8. Detects and reports time out conditions for a stall from a slave device, or a delayed or missing slave acknowledge.
9. Interrupts may optionally be generated.
10. Does not directly support segment pointer addressing as defined by the Enhanced Display Data Channel standard.

Segment pointer addressing as defined by the Enhanced Display Data Channel standard:

1. Use bit bashing (manual GPIO programming) to complete segment pointer write **without terminating in a stop or wait cycle**.
2. Terminate bit bashing phase with both I²C lines pulled high by tri-stating the data line before the clock line. Follow EDDC requirement for response received from slave device.
3. Initiate GMBUS cycle as required to transfer EDID following normal procedure.

Program 0x4653C[14] = 0x1 when doing back to back GMBUS transactions. The value can be safely left at 0x1 when GMBUS is not being used.

This will disable GMBUS unit level clock gating and only rely on partition level clock gating.

DC States

DC_STATE_EN

Plane Assignments and Capabilities

Broxton Plane Capabilities:

	Pipe A	Pipe B	Pipe C
Plane 4	Plane or Cursor	Plane or Cursor	Not supported
Plane 3	Plane	Plane	Plane or Cursor
Plane 2	Plane + Render Decompression, NV12	Plane + Render Decompression, NV12	Plane
Plane 1	Plane + Render Decompression, Frame Buffer compression, NV12	Plane + Render Decompression, NV12	Plane

Broxton Mapping to Command Streamer Plane Number

Display Plane Name	Command Streamer Plane Number
Plane 1 A	Plane 1
Plane 1 B	Plane 2
Plane 1 C	Plane 3
Plane 2 A	Plane 4
Plane 2 B	Plane 5
Plane 2 C	Plane 6
Plane 3 A	Plane 7
Plane 3 B	Plane 8
Plane 3 C	Plane 9
Plane 4 A	Plane 10
Plane 4 B	Plane 11
N/A	Plane 12

Display Buffer Programming

This topic describes display buffer allocation and shows a basic allocation method for single and multi-pipe modes. The display driver can choose to use more advanced allocation techniques as desired.

Display Buffer Allocation

Allocation of the display buffer is programmable for each display plane, using the buffer start and buffer end values in **PLANE_BUF_CFG**.



Proper display buffer allocation is important for Display hardware to function correctly. Optimal allocation provides better display residency in memory low power modes. Display Buffer allocation must be recalculated and programmed when pipes/planes get enabled or disabled.

Display Buffer Size

Display Buffer Size	Total Display Buffer Blocks	Fixed Bypass Path Allocation in Blocks	Blocks Available for Driver Programming
256 KB	512	4	0 - 507

Each display buffer block is 8 cache lines.

Allocation Requirements

Allocation must not overlap between any enabled planes.

A minimum allocation is required for any enabled plane. See Minimum Allocation Requirements below.

A gap between allocation for enabled planes is allowed.

The allocation for enabled planes should be as large as possible to allow for higher watermarks and better residency in memory power saving modes.

Planar YUV 420 Surfaces:

For YUV 420 Planar formats (NV12, P0xx), buffer allocation is done for Y and UV surfaces separately. Treat Y and UV surface as 2 separate planes. Also, the plane height and plane width for the UV plane should be halved.

UV Plane Height = Plane Height/2

UV Plane Width = Plane Width/2

Minimum Allocation Requirements

Allocation for each enabled plane must meet these minimum requirements.

Planes using Linear or X tiled memory formats must allocate a minimum of 8 blocks.

Planes using Y tiled memory formats must allocate blocks for a minimum number of scanlines worth of data. The formula and table of minimum scanlines is below.

Y tiled minimum allocation = Ceiling $[(4 * \text{Plane source width} * \text{Plane Bpp})/512] * \text{MinScanLines}/4 + 3$

Plane Bpp	Minimum Scanlines for Y Tile	
	0/180 Rotation	90/270 Rotation
1	8	32
2	8	16
4	8	8
8	8	4

Basic Allocation Method

These are basic methods that can be used for single and multi-pipe modes. For optimal power usage, the display driver can choose to use more advanced allocation techniques as desired.

Example Method 1:

Single Pipe

Allocate a fixed number of blocks to cursors and then allocate the remaining blocks among planes, based on each plane's data rate.

$$\text{BlocksAvailable} = \text{TotalBlocksAvailable}$$

1. Allocate 32 blocks for cursor

The driver frequently enables and disables the cursor or changes the cursor pixel format. Fixed allocation is preferred for cursor to minimize the buffer re-allocation. More allocation might be required to support deeper low power states (based on the results of watermark calculations).

$$\text{CursorBufAlloc} = 32$$

$$\text{BlocksAvailable} = \text{BlocksAvailable} - 32$$

2. Check for minimum buffer requirement

For each enabled plane

If Y tiled

MinScanLines = Look up minimum scanlines needed from the table

$$\text{PlaneMinAlloc} = \text{Ceiling} [(4 * \text{Plane width} * \text{Bpp})/512] * \text{MinScanLines}/4 + 3$$

Else

$$\text{PlaneMinAlloc} = 8$$

If sum of PlaneMinAlloc > BlocksAvailable

Error - Display Mode can't be supported.

The driver can change the number of enabled planes or the plane configuration and rerun the algorithm.

3. Calculate Relative Data Rate for planes



In this step the driver may want to use the expected maximum plane source sizes so it does not have to reallocate for a plane that is changing size.

For each enabled plane

If PlaneScalerEnabled

*PlaneScaleFactor = (Plane width/Scaler window X size) * (Plane height/Scaler window Y size)*

Else

PlaneScaleFactor = 1

*PlaneRelativeDataRate = Plane height * Plane width * plane source bytes per pixel * PlaneScaleFactor*

4. Allocate blocks for enabled planes as per the Data rate ratio.

For each plane that needs allocation (PlaneBlockAllocFinal == false)

*PlaneBufAlloc = floor (BlocksAvailable * PlaneRelativeDataRate/Sum of PlaneRelativeDataRate of all planes that need allocation).*

*floor - rounds down to an integer value dropping the fractional part.

5. Adjust for minimum allocation requirement

AdjustmentRequired = false

For each plane needs allocation (PlaneBlockAllocFinal == false)

If PlaneBufAlloc < PlaneMinAlloc

AdjustmentRequired = true

PlaneBufAlloc = PlaneMinAlloc

PlaneBlockAllocFinal = true

BlocksAvailable = BlocksAvailable - PlaneMinAlloc

If AdjustmentRequired = true

Go back to step 4

Multi-Pipe

Option 1:

Allocate a fixed number of blocks to cursors, allocate $1/NumPipes$ of the remaining blocks to each pipe, then calculate each pipe individually as in the Single Pipe case.

NumPipes = Total number of display pipes in the hardware

1. Allocate 8 blocks for cursor per pipe

The driver frequently enables and disables the cursor or changes the cursor pixel format. Fixed allocation is preferred for cursor to minimize the buffer re-allocation. More allocation might be required to support deeper low power states (based on the results of watermark calculations).

For each enabled cursor

CursorBufAlloc = 8

$$\text{BlocksAvailable} = \text{TotalBlocksAvailable} - (8 * \text{NumPipes})$$

2. Distribute the blocks equally among the pipes

$$\text{BlocksAvailable} = \text{BlocksAvailable} / \text{NumPipes}$$

3. Assign blocks to the planes

For each pipe

Perform Single Pipe sequence, starting from step 2.

Option 2:

Allocate a fixed number of blocks to cursors, use the Single Pipe case for all the other planes across all pipes.

Example Method 2:

This allocation is based on the Watermark calculations and helps to distribute the buffer more optimally to achieve consistent latency levels supported in all planes across all pipes.

- Allocate fixed number of blocks for cursor (for example 32 blocks).
- For each enabled plane in all pipes, calculate buffer allocation needed for all Latency levels 1 to 7.
- Calculate the total buffer allocation needed for each latency level by adding the individual allocation of all enabled planes.
- Choose the max latency level that can be supported with the available display buffer. For each enabled plane, program/enable all watermarks up to that latency level.
- Allocate the buffer to the planes as required by the latency level chosen.

Use method 1 to allocate any remaining buffer.

Buffer allocation re-distribution

When an additional pipe is getting enabled, or an existing pipe requires more buffer to support a new mode or is disabled, buffer reallocation may be necessary for proper display functionality. Whenever a portion of the allocated buffer is taken away from one pipe and allocated to a different pipe, the following sequence should be followed to make sure that there are no buffer allocation overlaps at any point of time.

1. *For each pipe whose allocation is reduced*
 - a. *Program the new buffer allocation.*
 - b. *Wait for VBlank of that pipe for new allocation to update.*
2. *For each pipe whose allocation is increased*
 - a. *Program the new buffer allocation.*
 - b. *Wait for VBlank of that pipe for new allocation to update.*



Display Buffer Allocation and Watermark programming prior to OS boot

Basic programming of the display buffer and watermarks to allow limited display usage prior to OS boot: This will prevent package power saving states from enabling.

Supported usages:

- Up to 3 pipes enabled at once
- Up to one universal plane enabled per pipe. No cursor.
- Linear or Xtile memory
- Any RGB frame buffer pixel format 32bpp or less, without render compression
- Any screen resolution
- Downscaling less than or equal to 12.5%

Allocate 160 blocks per pipe.

Pipe A: 0-159, Pipe B: 160-319, Pipe C: 320-479

PLANE_BUF_CFG_<plane number>_A = 0x009F0000

PLANE_BUF_CFG_<plane number>_B = 0x013F00A0

PLANE_BUF_CFG_<plane number>_C = 0x01DF0140

Set level 0 watermarks for any enabled plane to 160 blocks and 2 lines.

PLANE_WM_<plane number>_<pipe>_0 = 0x800080A0

The higher level watermarks for any enabled plane must have bit 31=0 to keep the low power watermarks disabled.

VGA

The VGA Control register is located here. The VGA I/O registers are located in the VGA Registers document.

VGA_CONTROL

VGA Enabling Sequence:

1. Program GTdriver mailbox data low = 0x000082BC (Override valid, latency reduced).
2. Program GT driver mailbox interface = 0x8000001D (WRITE_LTR_OVERRIDE).
3. Poll for GT driver mailbox interface = 0x00000000 (done and success). Timeout after 1ms and do not enable VGA.
4. Enable VGA in VGA_CONTROL
5. Clear VGA I/O register SR01 bit 5



VGA Disabling Sequence

1. Set VGA I/O register SR01 bit 5 for screen off
2. Wait for 100 us
3. Disable VGA in VGA_CONTROL
4. Program GT driver mailbox data low = 0x00000000 (Override invalid).
5. Program GT driver mailbox interface = 0x8000001D (WRITE_LTR_OVERRIDE).

Poll for GTdriver mailbox interface = 0x00000000 (done and success). Timeout after 1ms and continue.

Cursor Plane

Planes
PLANE_SURFLIVE
CUR_SURFLIVE

The CUR_CTL and CUR_FBC_CTL active registers will be updated on the vertical blank or when pipe is disabled, after the CUR_BASE register is written, or when cursor is not yet enabled, providing an atomic update of those registers together with the CUR_BASE register.

DDI Buffer

Registers

DDI_BUF_CTL
PHY_CTL_DDI
PHY_CTL_FAMILY
PORT_CL1CM_DW0
PORT_CL1CM_DW9
PORT_CL1CM_DW10
PORT_CL1CM_DW28
PORT_CL1CM_DW30
PORT_REF_DW3
PORT_REF_DW6
PORT_REF_DW8
PORT_TX_DW2
PORT_TX_DW3
PORT_TX_DW4
PORT_TX_DW14
PORT_PCS_DW10

**PORT_PCS_DW12****P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR**

PORT_CL and PORT_REF address entire PHYs.

PORT_PCS address lane pairs (0+1, 2+3) per DDI (A, B, C).

PORT_TX address individual lanes (0, 1, 2, 3) per DDI (A, B, C), or the entire group of lanes within a DDI (A, B, C).

The group access address can be used to simultaneously write the same value to a register that has instances in all 4 lanes. This is only for use when the same exact register value is applied to all 4 lanes. Reads using a port group address usually cannot return correct data. For read/modify/write to a group, the read should be to one of the lane addresses, then the write to the group address.

Broxton

DDIB and DDIC share a dual channel PHY, so PHY based programming will impact both DDIs at the same time.

DDIA/EDP uses a single channel PHY, so it is the only port in that PHY.

DDI PHY Initialization Sequence

The DDI PHY must be initialized before any DDI mode set or using the Aux channel.

Only the DDIA PHY is connected to a Rcomp resistor. DDIB and DDIC are dependent on the Rcomp value from DDIA, so DDIA must be enabled first. If DDIA won't be used, it can be disabled after Rcomp is copied.

1. If any DDI will be used, enable DDIA first since it supplies Rcomp
 - a. Write 1b to power request CH1_PWRREQ1P0_SUS (DDIA/eDP IO Power On) in P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR
 - b. Poll for PORT_CL1CM_DW0_A iphyprggood == 1b and bit 7 (reserved) == 0b. Reserved bit is checked to ensure register is in an accessible state (recommended poll time interval = 100 us).
 - c. If motherboard DDI RCOMP resistor is 100 Ohms, set PORT_REF_DW8_A fcompresel = 1b, else leave at default 0b for 400 Ohms.
 - d. Program PLL Rcomp code offset
 - i. Write 0xE4 to iref0rcoffset in PORT_CL1CM_DW9_A
 - ii. Write 0xE4 to iref1rcoffset in PORT_CL1CM_DW10_A
 - e. Program power gating
 - i. Write 11b to sus_clk_config and 1b to ocl1powerdownen and oldo_dynpwrdownen in PORT_CL1CM_DW28_A
 - f. Set PHY_CTL_FAMILY_EDP Common Reset = 1b (Enable)
2. If DDIB or DDIC will be used enable both B and C since they share the same PHY
 - a. Write 1b to power request CH0_PWRREQ1P0_SUS (DDIB/DDIC IO Power On) in P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR
 - b. Poll for PORT_CL1CM_DW0_BC iphyprggood == 1b and bit 7 (reserved) == 0b. Reserved bit is checked to ensure register is in an accessible state.

- c. If motherboard DDI RCOMP resistor is 100 Ohms, set PORT_REF_DW8_BC fcompresel = 1b, else leave at default 0b for 400 Ohms.
 - d. Program PLL Rcomp code offset
 - i. Write 0xE4 to iref0rcoffset in PORT_CL1CM_DW9_B and PORT_CL1CM_DW9_C
 - ii. Write 0xE4 to iref1rcoffset in PORT_CL1CM_DW10_B and PORT_CL1CM_DW10_C
 - e. Program power gating
 - i. Write 11b to sus_clk_config and 1b to ocl1powerdownen and oldo_dynpwrdownen in PORT_CL1CM_DW28_BC
 - ii. Write 1b to oldo_dynpwrdownen in PORT_CL2CM_DW6 [BXT]
 - f. Copy Rcomp from single channel PHY (EDP A) to dual channel PHY (DDI BC)
 - i. Poll for PORT_REF_DW3_A grc_done == 1b
 - ii. Read and save grccode from PORT_REF_DW6_A
 - iii. Write the saved grccode to ogrccode_fast, ogrccode_slow, and ogrccode_nom in PORT_REF_DW6_BC
 - iv. Write 1b to grcdis and grc_rdy_ovrd in PORT_REF_DW8_BC
 - g. Set PHY_CTL_FAMILY_DDI Common Reset = 1b (Enable)
3. If DDIA/EDP won't be used it can now be disabled
1. Clear PHY_CTL_FAMILY_EDP Common Reset to 0b (disable)
 2. Clear P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR CH1_PWRREQ1P0_SUS (DDIA/eDP IO Power On) to 0b (power off)

DDI PHY Un-Initialization Sequence

- Disable the PHY to save power if it will not be used for awhile
- DDIA/EDP
 1. Clear PHY_CTL_FAMILY_EDP Common Reset to 0b (disable)
 2. Clear P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR CH1_PWRREQ1P0_SUS (DDIA/eDP IO Power On) to 0b (power off)
 3. If the PHY is needed again, follow the initialization sequence. Rcomp does not need to be copied if DDIB+DDIC have not been disabled.
- DDIB+DDIC
 1. Clear PHY_CTL_FAMILY_DDI Common Reset to 0b (disable)
 2. Clear P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR CH0_PWRREQ1P0_SUS (DDIB/DDIC IO Power On) to 0b (power off)

If the PHY is needed again, follow the initialization sequence, including the DDIA enable and Rcomp copying.

Latency Optimization Settings

The latency optimization setting affects the alignment between output of different data lanes. It must be programmed during the DDI mode set, before enabling DDI_BUF_CTL. The value depends on the number of lanes enabled and lane reversal.



The table below gives the value to program in PORT_TX_DW14_LN<0,1,2,3>_<DDI> latency_optim for each lane for a given lane configuration on that DDI. Group access cannot be used here since each lane can have a unique value, and any later writes to PORT_TX_DW14 must not use group access so that they don't overwrite the individual lane values.

Lane configuration / latency_optim setting	X1 - Reversed and non-reversed	X2 - reversed and non-reversed	X4 - Reversed and non-reversed
PORT_TX_DW14_LN0_<DDI>	0	1	1
PORT_TX_DW14_LN1_<DDI>	0	0	0
PORT_TX_DW14_LN2_<DDI>	0	1	1
PORT_TX_DW14_LN3_<DDI>	0	0	1

Voltage Swing Programming Sequence

This sequence is used to setup the voltage swing before enabling the DDI, as well as for changing the voltage during DisplayPort link training. The voltage swing values are listed in the tables below.

1. Clear calc init
 - Write 0 to PORT_PCS_DW10_GRP_<DDI Letter> reg_tx1swingcalclinit and reg_tx2swingcalclinit
2. Program swing and deemphasis
 - Write swing value to PORT_TX_DW2_GRP_<DDI Letter> omargin000
 - Write scale value to PORT_TX_DW2_GRP_<DDI Letter> ouniqtranscale
 - Write scale enable to PORT_TX_DW3_GRP_<DDI Letter> oscaledcompmethod
 - Write deemphasis value to PORT_TX_DW4_GRP_<DDI Letter> ow2tapdeemph9p5
3. Set calc init to trigger update
 - Write 1 to PORT_PCS_DW10_GRP_<DDI Letter> reg_tx1swingcalclinit and reg_tx2swingcalclinit

Voltage swing programming for DisplayPort							
Voltage Swing Level ¹	Pre-emphasis Level ¹	Non-Transition mV diff p-p	Transition mV diff p-p	Pre-emphasis dB	Scale Enable and Value	Deemphasis decimal	Swing decimal
0	0	400	400	0	0, Don't Care	128	52
0	1	400	600	3.5	0, Don't Care	85	78
0	2	400	800	6	0, Don't Care	64	104
0	3	400	1200	9.5	0, Don't Care	43	154
1	0	600	600	0	0, Don't Care	128	77
1	1	600	900	3.5	0, Don't Care	85	116
1	2	600	1200	6	0, Don't Care	64	154
2	0	800	800	0	0, Don't Care	128	102

Voltage swing programming for DisplayPort							
2	1	800	1200	3.5	0, Don't Care	85	154
3	0	1200	1200	0	1, 0x9A	128	154

¹The voltage swing level and pre-emphasis level values follow the naming used in the DisplayPort standard.

Voltage swing programming for embedded DisplayPorts that support low voltage swings							
Voltage Swing Level ¹	Pre-emphasis Level ¹	Non-Transition mV diff p-p	Transition mV diff p-p	Pre-emphasis dB	Scale Enable and Value	Deemphasis decimal	Swing decimal
0	0	200	200	0	0, Don't Care	128	26
0	1	200	240	1.5	0, Don't Care	112	38
0	2	200	320	4	0, Don't Care	96	48
0	3	200	400	6	0, Don't Care	69	54
1	0	250	250	0	0, Don't Care	128	32
1	1	250	300	1.5	0, Don't Care	104	48
1	2	250	400	4	0, Don't Care	85	54
2	0	300	300	0	0, Don't Care	128	43
2	1	300	360	1.5	0, Don't Care	101	54
3	0	350	350	0	0, Don't Care	128	48

¹The voltage swing level and pre-emphasis level values follow the naming used in the DisplayPort standard.


Broxton
Voltage swing programming for HDMI and DVI

Non-Transition mV diff p-p	Transition mV diff p-p	Pre-emphasis dB	Scale Enable and Value	Deemphasis decimal	Swing decimal	Recommended Usage
400	400	0	0, Don't Care	128	52	Recommended for HDMI Active Level Shifter
400	600	3.5	0, Don't Care	85	52	
400	900	6	0, Don't Care	64	52	
400	1200	9.5	0, Don't Care	43	42	
600	600	0	0, Don't Care	128	77	
600	900	3.5	0, Don't Care	85	77	
600	1200	6	0, Don't Care	64	77	
800	800	0	0, Don't Care	128	102	
800	1200	3.5	0, Don't Care	85	102	Recommended for HDMI Cost Reduced Level Shifter and DisplayPort Dual Mode
1200	1200	0	1, 0x9A	128	154	
1000	1000	0	1, 0x9A	128	133	Frequencies less than or equal to 165 MHz
850	1200	3	1, 0x9A	96 for lanes 0/1/2 *128 for lane 3	160	Frequencies greater than 165 MHz *Use group register offset to program deemphasis 96 to all lanes, then use the LN3 register offset to program deemphasis 128 for lane 3



Intel® Open Source HD Graphics, Intel Iris™ Graphics, and Intel Iris™ Pro Graphics

Programmer's Reference Manual

For the 2015 - 2016 Intel Core™ Processors, Celeron™ Processors, and Pentium™ Processors based on the "Skylake" Platform

Volume 8: Workarounds

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Workarounds

This page lists all BSpec narrative workarounds for BXT. Note that the functional area for each item is listed below, so you can search on this value or other content on this page. Also note that a "BSpec ID" has been assigned to make it easier to reference these items.

BSpec ID	Functional Area/Component		Submitted By	Workaround Name	Workaround Description	Valid Steppings
0302	3D			WaCompressedResourceRequiresConstVA21	GFXDRV: Hot spotting issue with render target compression. WA: Align lossless compressed resource allocations to 2MB or have fixed virtual addresses. This WA is specifically for steppings where HW will not fix.	All
0303	3D	MEDIA_STATE_FLUSH			A MEDIA_STATE_FLUSH with no options must be added after a GPGPU_WALKER command if pooled mode is enabled.	
0522	KMD			WaldleLiteRestore	SW must always ensure ring buffer head pointer is not equal to tail pointer of a context, whenever it is submitted to HW for execution. WA: Driver should not submit a context with head = tail.	BXT:C0
0523	KMD			WaldleLiteRestore	SW must always ensure "Force Restore Bit" in the context descriptor is set for a preempted context that is getting resubmitted. WA: Driver should not submit a context with head = tail.	BXT:C0



BSpec ID	Functional Area/Component		Submitted By	Workaround Name	Workaround Description	Valid Steppings
0525	Command Stream Programming			N/A	On BXT "RS enabled Batch Buffer Per Context" can be programmed with MI_SEMAPHORE_WAIT command in register poll mode. Resource streamer stops executing the "RS enabled Batch Buffer Per Context" on encountering MI_SEMAPHORE_WAIT command. SW must ensure all the commands meant to be executed by Resource Streamer from "RS enabled Batch Buffer Per Context" must be programmed prior to programming the MI_SEMAPHORE_WAIT command.	All
0891	GPGPU	Midthread preemption	Jim Valerio		When a pooled workload is mid-thread preempted, followed by RC6 or Render power gate, then the mid-thread restore process does not restore pooling-enabled signal soon enough. This causes context corruption and possibly a hang. WA: Insert "Media_Pool_State" command in the WA batch buffer that is run before a context restore (MMIO 0x21C4).	ALL



BSpec ID	Functional Area/Component		Submitted By	Workaround Name	Workaround Description	Valid Steppings
0908	SFC	SFC Crop Limitation for VEBOX+SFC Mode	Karthik N	WaDisableSFCSrcCrop	Below are the cases to switch from SFC to Render for VEBOX+SFC mode Case 1. ((SurfaceHeight > 1120) && (Top > 1120)) Case 2. ((SurfaceHeight > 1120) && (Bottom < SurfaceHeight)) Case 3. ((SurfaceHeight > 1120) && (Left > 0)) Case 4. ((SurfaceHeight > 1120) && (Right < SurfaceWidth))	ALL
0909	GS PrimID bug with Tessellation	Peter Doyle			GS Clock gating must be disabled under the following conditions: Tessellation enabled, GS enabled, GS PrimitiveID enabled.	BXT: ALL
0911	CPD	Bus Hang	Jim Valerio		Hang occurs with a change of CPD Exit ordering of messages. Reverting that change avoids the hang. WA: Set 0xA194[9]=0 to revert the change. This register is set in BIOS and locked.	BXT:ALL



BSpec ID	Functional Area/Component		Submitted By	Workaround Name	Workaround Description	Valid Steppings
0913	GPGPU		Hema C Nalluri		Hang occurs when CPD flows happen concurrently when CS is reading MMIO outside GT. WA: Reads to MMIO registers outside GT (Register Address > 0x40000) are not supported through MI commands (MI_LOAD_REGISTER_REG, MI_STORE_REGISTER_MEM) programmed in command buffer.	BXT:ALL
0915	HDC	Atomic Counter	Jim Valerio		Hang occurs with Atomic Counter message with binary operations (i.e. have a separate data operand), in some dynamic load situations. WA: Replace use of hidden counter with an explicit counter location, and then use a typed or untyped Dword Atomic operation message instead.	ALL
0921	GTI	GAM	Niran Cooray		When running legacy contexts with GTTC enabled, faults on upper levels of page table entries can result in a GAM hang. Only applicable when faults are supported. WA: Disable GTT Cache	ALL



BSpec ID	Functional Area/Component		Submitted By	Workaround Name	Workaround Description	Valid Steppings
0924	Blitter		Andrew Vanderheyden	DisallowOddSizedSmallFCBlits	FC Blitter cannot handle a blit whose $y\text{-height} \% 4 == 3$ and $y\text{-height} \leq 8$. This causes a system hang. WA: These blits must be detected and sent to the legacy blitter engine, not the fast copy engine.	ALL
0925	GTI	GAM	Niran Cooray		Clock gating issue in gamtwarb fub in gamtunit as its not accounting for the evicting cycle present in the ingress fifo btw GAMD and GAMT. Due to this the write buffer ID is used for multiple write transactions - which is not expected in GAM and results in a logic hang. We could have this scenario if we have S/W register based WCP/RCP invalidation [write to register 4AAC], instead of fence based invalidation. WA: Disable clock gating for the Write arbiter logic(0x4A08[10]=1) through GFX driver	ALL



Display Workarounds

This page lists all workarounds for Display. Note that the functional area for each item is listed below, so you can search on this value or other content on this page. Also note that a "BSpec ID" has been assigned to make it easier to reference these items.

BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0839	Display	MIPI		While MIPI is enabled in dual link mode (DPI MIPI_PORT_CTRL EN=1 or DBI writing a frame), the pipe attached to MIPI must have at least one plane or cursor enabled or pipe scaling enabled. Otherwise the MIPI image will shift and won't correct itself until MIPI is disabled and PG1 is disabled and re-enabled. BXT-Bstep: In the disable sequence, Planes can be disabled after disabling Device ready and MIPI port control BXT-Astep: Scalar as well needs to be ON before we start BXT B-step disable sequence.	All
0854	Display	Backlight		Backlight PWM may stop in the asserted state, causing backlight to stay fully on. WA: Before disabling PWM, set 0x46530 bit 13 for PWM1 or bit 14 for PWM2. The bits can remain set without harm.	SIWA_FROM_B0



BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
0855	Display	MIPI DSI		MIPI DSI dual link front back mode has image shifts if all planes and cursor on the pipe are disabled and pipe scaling (panel fitting) is disabled. WA: The pipe attached to MIPI DSI dual link in front back mode must always have at least one plane or cursor enabled or pipe scaling (panel fitting) enabled. The added plane can be hidden by using plane alpha to make it transparent.	All
0904	Display	VGA		Corruption with some VGA modes and clock frequencies. WA: Set the bits 30:29 of MMIO register 0x41004 to 01b.	ALL
1110	Display	FBC + PSR/PSR2		Missing flips when FBC is enabled with PSR link off/PSR2 deep sleep scenarios. WA: When FBC is enabled with PSR/PSR2, set bit 30 of MMIO register 0x420CC to 1b.	ALL



BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
1124	Display	Panel Power Sequencing		Incorrect panel power up delays WA: Wait at least 100us between programming PP_ON_DELAYS and enabling Power State Target in PP_CONTROL, or disable dpls clock gating before programming PP_ON_DELAYS and leave disabled until after enabling Power State Target in PP_CONTROL. North display dpls clock gate disable is register 0x46530 bits 17 and 16. South display dpls clock gate disable is register 0xC2020 bit 29.	All
1128	Display	MIPI DSI		MIPI DSI Rcomp failures which can cause image corruption at hot temperatures. BXT WA: In the MIPI Enable Sequence, just after the step that sets P_CR_GT_DISP_PWRON_0_2_0_GTTMMADR MIPIO_RST_CTRL to 0x1, program DSI_PHY_DW6 HS_OVR_EN=0x1 and HS_OVR_VALUE=0xA.	All
1135	Display	IPC		Display underrun when IPC is enabled. WA: The Line Time programmed in the WM_LINETIME register should be half of the actual calculated Line Time. Programmed Line Time = $1/2 \times \text{Calculated Line Time}$	All



BSpec ID	Functional Area/Component		Workaround Name	Workaround Description	Valid Steppings
1136	Display	PSR		Display underrun with PSR single frame update or PSR2, and planes with less than watermark level 7. WA: When using PSR single frame update or PSR2, all enabled planes must have enabled up to watermark level 7. If any plane cannot support level 7, then single frame update or PSR2 cannot be enabled.	All