



Intel® UHD Graphics Open Source

Programmer's Reference Manual

For the 2018 - 2019 Intel Core™ Processors, Pentium® Gold Processors, and Celeron® Processors based on the "Whiskey Lake" Platform

Volume 1: Configurations

January 2020, Revision 1.0



Creative Commons License

You are free to Share - to copy, distribute, display, and perform the work under the following conditions:

- **Attribution.** You must attribute the work in the manner specified by the author or licensor (but not in any way that suggests that they endorse you or your use of the work).
- **No Derivative Works.** You may not alter, transform, or build upon this work.

Notices and Disclaimers

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

A "Mission Critical Application" is any application in which failure of the Intel Product could result, directly or indirectly, in personal injury or death. SHOULD YOU PURCHASE OR USE INTEL'S PRODUCTS FOR ANY SUCH MISSION CRITICAL APPLICATION, YOU SHALL INDEMNIFY AND HOLD INTEL AND ITS SUBSIDIARIES, SUBCONTRACTORS AND AFFILIATES, AND THE DIRECTORS, OFFICERS, AND EMPLOYEES OF EACH, HARMLESS AGAINST ALL CLAIMS COSTS, DAMAGES, AND EXPENSES AND REASONABLE ATTORNEYS' FEES ARISING OUT OF, DIRECTLY OR INDIRECTLY, ANY CLAIM OF PRODUCT LIABILITY, PERSONAL INJURY, OR DEATH ARISING IN ANY WAY OUT OF SUCH MISSION CRITICAL APPLICATION, WHETHER OR NOT INTEL OR ITS SUBCONTRACTOR WAS NEGLIGENT IN THE DESIGN, MANUFACTURE, OR WARNING OF THE INTEL PRODUCT OR ANY OF ITS PARTS.

Intel may make changes to specifications and product descriptions at any time, without notice. Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined". Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. The information here is subject to change without notice. Do not finalize a design with this information.

The products described in this document may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Implementations of the I2C bus/protocol may require licenses from various entities, including Philips Electronics N.V. and North American Philips Corporation.

Intel and the Intel logo are trademarks of Intel Corporation in the U.S. and other countries.

* Other names and brands may be claimed as the property of others.

Copyright © 2020, Intel Corporation. All rights reserved.



Table of Contents

Configurations Overview	1
Top Level Block Diagrams WHL.....	2
Device Attributes WHL	3
Stepping and Device IDs WHL	7



Configurations Overview

The Intel "Gen" Graphics Architecture was first introduced to the market in 2004. Since that time, the architecture and implementation have evolved to add many new features, increase performance, and improve power efficiency.

Each product generation has its own configurations chapter. Each chapter has a section for each project, and each project contains the following subsections:

- Top Level Block Diagrams - Shows basic feature blocks of the project's graphics architecture for GT configurations.
- Device Attributes - Lists details of the graphics configuration options for each project.
- Steppings and Device IDs - Lists all the current unique GT Die / Packages for a specific project.

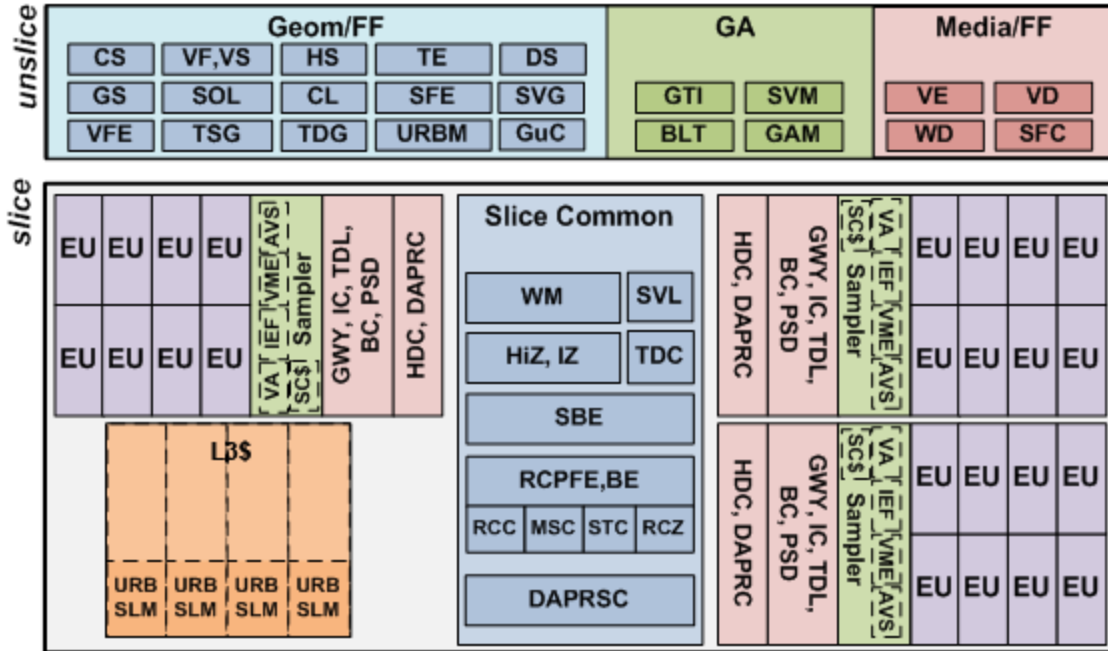


Top Level Block Diagrams WHL

The diagrams below show basic feature blocks of the Gen9 Whiskey Lake (WHL) graphics architecture.

GT2 Configuration

The GT2 configuration contains one Unslice and one Slice with separate power domains for each, although they share a single clock domain.





Device Attributes WHL

The following table lists detailed GT device attributes for Whiskey Lake (WHL) SKUs.

NOTE: This information is preliminary, and subject to change.

Product Configuration Attribute Table		
Product Family	WHL	
Architectural Name *	1x2x6	1x3x8
SKU Name	GT1F	GT2
Global Attributes		
Slice count	1	1
Subslice Count	2	3
EU/Subslice	6	8
EU count (total)	12	23 / 24 [b]
Thread Count	7	7
Thread Count (Total)	84	161 / 168
FLOPs/Ck - Half Precision, MAD (peak)	384	736 / 768
FLOPs/Ck - Single Precision, MAD (peak)	192	368 / 384
FLOPs/Ck - Double Precision, MAD (peak)	48	92 / 96
Unslice clocking (coupled/decoupled from Cr slice)	coupled	coupled
GTI / Ring Interfaces	1	1
GTI bandwidth (bytes/unslice-clk)	64: R	64: R
	64: W	64: W
eDRAM Support	N/A	N/A
Graphics Virtual Address Range	48 bit	48 bit
Graphics Physical Address Range	39 bit	39 bit
Caches & Dedicated Memories		
L3 Cache, total size (bytes)	384K	768K
L3 Cache, bank count	2	4
L3 Cache, bandwidth (bytes/clk)	2x 64: R	4x 64: R
	2x 64: W	4x 64: W
L3 Cache, D\$ Size (Kbytes)	192K - 256K	512K
URB Size (kbytes)	128K - 192K	384K
SLM Size (kbytes)	0, 128K	0, 192K



Product Configuration Attribute Table		
LLC/L4 size (bytes) [1]	~2MB/CPU core	~2MB/CPU core
Instruction Cache (IC, bytes)	2x 48K	3x 48K
Color Cache (RCC, bytes)	24K	24K
MSC Cache (MSC, bytes)	16K	16K
HiZ Cache (HZC, bytes)	12K	12K
Z Cache (RCZ, bytes)	32K	32K
Stencil Cache (STC, bytes)	8K	8K
Instruction Issue Rates		
FMAD, SP (ops/EU/clock)	8	8
FMUL, SP (ops/EU/clock)	8	8
FADD, SP (ops/EU/clock)	8	8
MIN,MAX, SP (ops/EU/clock)	8	8
CMP, SP (ops/EU/clock)	8	8
INV, SP (ops/EU/clock)	2	2
SQRT, SP (ops/EU/clock)	2	2
RSQRT, SP (ops/EU/clock)	2	2
LOG, SP (ops/EU/clock)	2	2
EXP, SP (ops/EU/clock)	2	2
POW, SP (ops/EU/clock)	1	1
IDIV, SP (ops/EU/clock)	1-6	1-6
TRIG, SP (ops/EU/clock)	2	2
FDIV, SP (ops/EU/clock)	1	1
Load/Store		
Data Ports (HDC)	2	3
L3 Load/Store (dwords/clock)	2x 64	3x 64
SLM Load/Store (dwords/clock)	2x 64	3x 64
Atomic Inc, 32b - sequential addresses (dwords/clock)	2x 64	3x 64
Atomic Inc, 32b - same address (dwords/clock)	2x 4	3x 4
Atomic CmpWr, 32b - sequential addresses (dwords/clock)	2x 32	3x 32
Atomic CmpWr, 32b - same address (dwords/clock)	2x 4	3x 4
3D Attributes		
Geometry pipes	1	1
Samplers (3D)	2	3



Product Configuration Attribute Table		
Texel Rate, point, 32b (tex/clock)	8	12
Texel Rate, point, 64b (tex/clock)	8	12
Texel Rate, point, 128b (tex/clock)	8	12
Texel Rate, bilinear, 32b (tex/clock)	8	12
Texel Rate, bilinear, 64b (tex/clock)	8	12
Texel Rate, bilinear, 128b (tex/clock)	2	3
Texel Rate, trilinear, 32b (tex/clock)	8	12
Texel Rate, trilinear, 64b (tex/clock)	4	6
Texel Rate, trilinear, 128b (tex/clock)	1	1.5
Texel Rate, aniso 2x, MIP Linear,, 32b (tex/clock)	2	3
Texel Rate, aniso 4x, MIP Linear,, 32b (tex/clock)	1	1.5
Texel Rate, aniso 8x, MIP Linear,, 32b (tex/clock)	0.5	0.75
Texel Rate, aniso 16x, MIP Linear,, 32b (tex/clock)	0.25	0.375
HiZ Rate, (ppc)	64	64
IZ Rate, (ppc)	16	16
Stencil Rate (ppc)	64	64
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)		
Pixel Rate, fill, 32bpp (pix/clock, RCC hit)	8	8
Pixel Rate, fill, 32bpp (pix/clock, LLC hit @ 1.0x unslice clock) [2]		
Pixel Rate, fill, 32bpp (pix/clock, LLC hit, @ 1.5x unslice clock) [2]	N/A	N/A
Pixel Rate, fill, 32bpp (pix/clock, memory, @ 1.0x unslice clock) [2]		
Pixel Rate, fill, 32bpp (pix/clock, memory, @ 1.5x unslice clock) [2]	N/A	N/A
(500 MHz, DDR-2400 or eDRAM; Range depends on dynamic compression ratio)		
Pixel Rate, blend, 32bpp (p/clock, RCC hit)	8	8



Product Configuration Attribute Table		
Pixel Rate, blend, 32bpp (p/clock, LLC hit, @ 1.0x unslice clock) [2]		
Pixel Rate, blend, 32bpp (p/clock, LLC hit, @ 1.5x unslice clock) [2]	N/A	N/A
Pixel Rate, blend, 32bpp (pix/clock, memory, @ 1.0x unslice clock) [2]		
Pixel Rate, blend, 32bpp (pix/clock, memory, @ 1.5x unslice clock) [2]	N/A	N/A
Media Attributes		
Samplers (media)	2	3
VDBox Instances	1	1
VEBox Instances	1	1
SFC Instances	1	1
WGBox Instances	N/A	N/A
Display Attributes		
Display Pipes	3	3
Display Planes per Pipe	3	3
DDI ports	2	2
eDP ports	1	1
Footnotes: * Architectural Name = Slice Count x Subslice Count x EUs per Subslice [a] SKU naming & details has not yet been decided. [b] One EU reserved for die recovery purposes. [c] In the GT4 SKU, a decoupled unslice feature is supported, where the slice and unslice may operate on independent voltage planes (if supported by the platform), and may have independent clocking.		



Stepping and Device IDs WHL

The following table lists variations of GT Die / Packages for Gen9 Whiskey Lake (WHL).

This information is preliminary, and subject to change at any time.

Segment	SKU	TDP	EUs	CPU Brand	Brand #	GFX Name	CPU Stepping	GT/Display Version	DID2 Grouping	DID2 8th Gen	Rev ID	POR	Notes
Mobile	U42	15	24	Core i7	620	Intel® UHD Graphics	WHL W0	KBL G0 / KBL C0	15	3EA0	0x0	Y	
Mobile	U42	15	24	Core i5	620	Intel® UHD Graphics	WHL W0	KBL G0 / KBL C0	15	3EA0	0x0	Y	
Mobile	U2f2	15	23	Core i3	620	Intel® UHD Graphics	WHL W0	KBL G0 / KBL C0	15	3EA0	0x0	Y	
Mobile	U2f2	15	24	Core i3	620	Intel® UHD Graphics	WHL W0	KBL G0 / KBL C0	15	3EA0	0x0	Y	Readiness SKU
Mobile	U41f	15	12	Pentium	610	Intel® UHD Graphics	WHL W0	KBL G0 / KBL C0	16	3EA1	0x0	Y	Readiness SKU
Mobile	U2f1f	15	12	Celeron	610	Intel® UHD Graphics	WHL W0	KBL G0 / KBL C0	16	3EA1	0x0	Y	Readiness SKU
Mobile	U42	15	24	Core i7	620	Intel® UHD Graphics	WHL V0	CFLC0 / KBL C0	15	3EA0	0x2	Y	
Mobile	U42	15	24	Core i5	620	Intel® UHD Graphics	WHL V0	CFLC0 / KBL C0	15	3EA0	0x2	Y	
Mobile	U2f2	15	23	Core i3	620	Intel® UHD Graphics	WHL V0	CFLC0 / KBL C0	15	3EA0	0x2	Y	
Mobile	U2f2	15	24	Core i3	620	Intel® UHD Graphics	WHL V0	CFLC0 / KBL C0	15	3EA0	0x2	Y	Readiness SKU
Mobile	U41f	15	12	Pentium	610	Intel® UHD Graphics	WHL V0	CFLC0 / KBL C0	16	3EA1	0x2	Y	Readiness SKU
Mobile	U2f1f	15	12	Celeron	610	Intel® UHD Graphics	WHL V0	CFLC0 / KBL C0	16	3EA1	0x2	Y	Readiness SKU

WHL U42 W0 GT baseline = KBL G0.