SiFive Vector Coprocessor Interface (VCIX) Software Specification

Version 1.1

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Proprietary Notice

Revision History

Version	Date	Changes
1.1	June 26, 2024	• Update intrinsics descriptions to have the __riscv_ prefix.
1.0	December 15, 2022	• Initial revision

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Introduction

The SiFive Vector Coprocessor Interface (VCIX) provides a flexible mechanism to extend application processors with custom coprocessors and variable-latency arithmetic units. The interface offers throughput comparable to that of standard RISC-V vector instructions. To accelerate performance, system designers may use VCIX as a low-latency, high-throughput interface to a coprocessor.

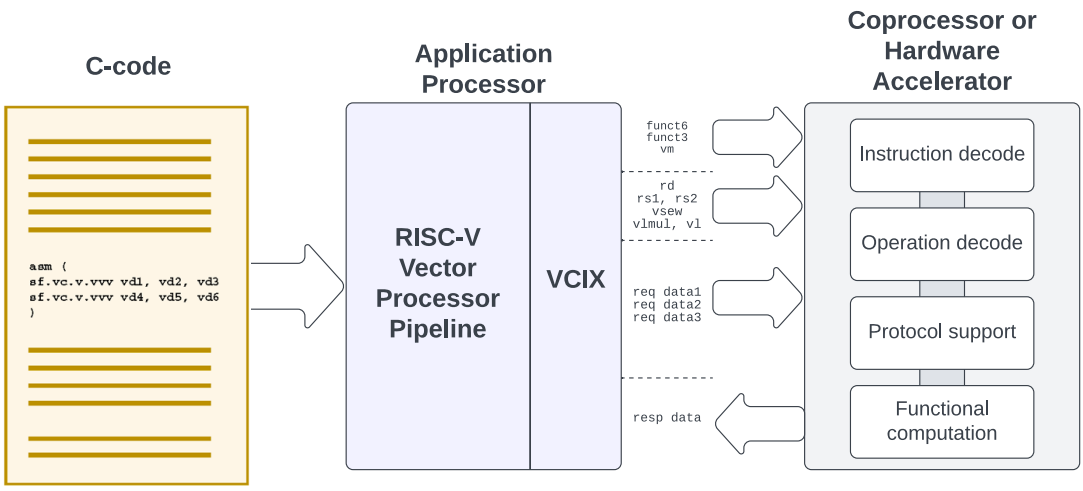

Figure 1: *VCIX Block Diagram*

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Instruction Formats

Coprocessor instructions are encoded within the CUSTOM-2 major opcode, i.e., instruction bits 6..0 are `1011011`. They use encoding and operand patterns similar to standard RISC-V vector instructions. Hyphens denote opcode bits usable by the coprocessor for any purpose.

Mnemonic	funct6	vm	rs2	rs1	funct3	rd	Destination	Sources
sf.vc.x	0000--	1	-----	xs1	100	-----	none	scalar xs1
sf.vc.v.x	0000--	0	-----	xs1	100	vd	vector vd	scalar xs1
sf.vc.i	0000--	1	-----	simm	011	-----	none	simm[4:0]
sf.vc.v.i	0000--	0	-----	simm	011	vd	vector vd	simm[4:0]
sf.vc.vv	0010--	1	vs2	vs1	000	-----	none	vector vs1, vector vs2
sf.vc.v.vv	0010--	0	vs2	vs1	000	vd	vector vd	vector vs1, vector vs2
sf.vc.xv	0010--	1	vs2	xs1	100	-----	none	scalar xs1, vector vs2
sf.vc.v.xv	0010--	0	vs2	xs1	100	vd	vector vd	scalar xs1, vector vs2
sf.vc.iv	0010--	1	vs2	simm	011	-----	none	simm[4:0], vector vs2
sf.vc.v.iv	0010--	0	vs2	simm	011	vd	vector vd	simm[4:0], vector vs2
sf.vc.fv	00101-	1	vs2	fs1	101	-----	none	scalar fs1, vector vs2
sf.vc.v.fv	00101-	0	vs2	fs1	101	vd	vector vd	scalar fs1, vector vs2
sf.vc.vvv	1010--	1	vs2	vs1	000	vd	none	vector vs1, vector vs2, vector vd
sf.vc.v.vvv	1010--	0	vs2	vs1	000	vd	vector vd	vector vs1, vector vs2, vector vd
sf.vc.xvv	1010--	1	vs2	xs1	100	vd	none	scalar xs1, vector vs2, vector vd
sf.vc.v.xvv	1010--	0	vs2	xs1	100	vd	vector vd	scalar xs1, vector vs2, vector vd
sf.vc.ivv	1010--	1	vs2	simm	011	vd	none	simm[4:0], vector vs2, vector vd
sf.vc.v.ivv	1010--	0	vs2	simm	011	vd	vector vd	simm[4:0], vector vs2, vector vd
sf.vc.fvv	10101-	1	vs2	fs1	101	vd	none	scalar fs1, vector vs2, vector vd
sf.vc.v.fvv	10101-	0	vs2	fs1	101	vd	vector vd	scalar fs1, vector vs2, vector vd
sf.vc.vvw	1111--	1	vs2	vs1	000	vd	none	vector vs1, vector vs2, wide vd
sf.vc.v.vvw	1111--	0	vs2	vs1	000	vd	wide vd	vector vs1, vector vs2, wide vd
sf.vc.xvw	1111--	1	vs2	xs1	100	vd	none	scalar xs1, vector vs2, wide vd
sf.vc.v.xvw	1111--	0	vs2	xs1	100	vd	wide vd	scalar xs1, vector vs2, wide vd
sf.vc.ivw	1111--	1	vs2	simm	011	vd	none	simm[4:0], vector vs2, wide vd
sf.vc.v.ivw	1111--	0	vs2	simm	011	vd	wide vd	simm[4:0], vector vs2, wide vd
sf.vc.fvw	11111-	1	vs2	fs1	101	vd	none	scalar fs1, vector vs2, wide vd
sf.vc.v.fvw	11111-	0	vs2	fs1	101	vd	wide vd	scalar fs1, vector vs2, wide vd

Bits 24..20 encode the vs2 argument; bits 19..15 encode the xs1/fs1/vs1/simm[4:0] argument; bits 11..7 encode vd. Bit position 26, and sometimes 27, are available for arbitrary coprocessor use. For the formats for which the vs2 argument is not present, the vs2 field is available for arbitrary coprocessor use.

Bit 25 (the vm field) indicates whether the instruction writes the destination register, vd. When vm is 1, vd is not written. When vm is 0, vd is written. For the instructions with three source operands, vd remains a source, regardless of the setting of vm. For the formats for which the vd

source operand is not present, the vd field becomes free for arbitrary coprocessor use when vm is 1.

Hazard-checking logic permits at most one outstanding instruction per destination register, but there is no such limit on the number of outstanding instructions for which the vm field is 1.

Coprocessor instructions respect SEW, LMUL, and vl.

Coprocessor instructions are not masked. Coprocessor instructions always follow a modified tail-agnostic policy: for instructions that write vd, the contents of elements [vl, VLMAX-1] become UNSPECIFIED.

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Exceptions

Variants with scalar floating-point arguments raise an illegal-instruction exception when `SEW` is not set to a supported floating-point width. Furthermore, when `FLEN` > `SEW`, floating-point scalars must be NaN-boxed (i.e., bits `FLEN`-1 .. `SEW` must be all 1s), else they're interpreted as the canonical NaN.

Coprocessor instructions respect and update the `mstatus.VS` field in the same manner as other vector instructions, including raising illegal-instruction exceptions when `mstatus.VS=0`.

Illegal-instruction exceptions are raised when register-overlap constraints for different-EEW operands are violated. These constraints are the same as for other RISC-V vector instructions, as described in this section of the RISC-V vector ISA specification:

https://github.com/riscv/riscv-v-spec/blob/master/v-spec.adoc#52-vector-operands

The coprocessor interface does not provide a mechanism for coprocessors to raise exceptions.

Traps on coprocessor instructions are always reported with a `vstart` of 0. Coprocessor instructions raise an illegal instruction exception if `vstart` is non-zero.

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Toolchain Interface

VCIX needs to enabled by adding `xsfvcp` to -march string. For example, consider the following:

```
-march=rv64gc_xsfvcp
```

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Assembly Mnemonics

Assembly mnemonics will closely follow the pattern of other custom vector instructions, except with additional immediates corresponding to the custom-use bits of the `funct6`, `rs2`, and `rd` fields, where applicable. Each of these immediates is input as an integer in [0,2b-1], where `b` is the number of custom-use bits in the associated field. This contrasts with the `simm5` field, which is input, where applicable, as an integer in [-16,15], analogously to standard vector instructions.

```
sf.vc.x     <bit-27-26>,<bit-24-20>,<bit-11-7>, rs1
sf.vc.v.x   <bit-27-26>,<bit-24-20>, vd, rs1
sf.vc.i     <bit-27-26>,<bit-24-20>,<bit-11-7>, simm5
sf.vc.v.i   <bit-27-26>,<bit-24-20>, vd, simm5
sf.vc.vv    <bit-27-26>,<bit-11-7>, vs2, vs1
sf.vc.v.vv  <bit-27-26>, vd, vs2, vs1
sf.vc.xv    <bit-27-26>,<bit-11-7>, vs2, rs1
sf.vc.v.xv  <bit-27-26>, vd, vs2, rs1
sf.vc.iv    <bit-27-26>,<bit-11-7>, vs2, simm5
sf.vc.v.iv  <bit-27-26>, vd, vs2, simm5
sf.vc.fv    <bit-26>,<bit-11-7>, vs2, fs1
sf.vc.v.fv  <bit-26>, vd,vs2,fs1
sf.vc.vvv   <bit-27-26>, vd, vs2, vs1
sf.vc.v.vvv <bit-27-26>, vd, vs2, vs1
sf.vc.xvv   <bit-27-26>, vd, vs2, rs1
sf.vc.v.xvv <bit-27-26>, vd, vs2, rs1
sf.vc.ivv   <bit-27-26>, vd, vs2, simm5
sf.vc.v.ivv <bit-27-26>, vd, vs2, simm5
sf.vc.fvv   <bit-26>, vd, vs2, fs1
sf.vc.v.fvv <bit-26>, vd, vs2, fs1
sf.vc.vvw   <bit-27-26>, vd, vs2, vs1
sf.vc.v.vvw <bit-27-26>, vd, vs2, vs1
sf.vc.xvw   <bit-27-26>, vd, vs2, rs1
sf.vc.v.xvw <bit-27-26>, vd, vs2, rs1
sf.vc.ivw   <bit-27-26>, vd, vs2, simm5
sf.vc.v.ivw <bit-27-26>, vd, vs2, simm5
sf.vc.fvw   <bit-26>, vd, vs2, fs1
sf.vc.v.fvw <bit-26>, vd, vs2, fs1
```

The user can leverage assembler macros to improve maintainability, like the following:

```
# Define new mnemonics sf.mac.v.vvv by macro.
.macro sf.mac.v.vvv vd, vs1, vs2
  sf.vc.v.vvv 0x1, \vd, \vs2, \vs1
.endm
  # Same as sf.vc.v.vvv 0x1, v2, v3, v4, but better for maintainability
  sf.mac.v.vvv v2, v4, v3
  # Same as sf.mac.v.vvv v2, v4, v3, but user need to provide 0x1 for bit 27 and bit
```

```
26, which
  # is error prone.
  sf.vc.v.vvv 0x1, v2, v3, v4
```

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C Intrinsics

The VCIX intrinsic interface is designed to be compatible with the existing RVV intrinsics API, and we strongly recommended using this API rather than inline assembly. `vl` and `vtype` are managed by the compiler in the programming model of RVV intrinsic program. Mixing C intrinsics with inline assembly might result in poor quality of the generated code.

The design of VCIX intrinsic interface:

- Only provides unsigned integer types as the arguments and return type for both scalar and vector type. The only exception is an instruction that has floating point scalar arguments. These will take a `SEW`-width floating point scalar as argument instead of `SEW`-width unsigned integer scalar. The user may apply type-casts, type-punning, and RVV vreinterpret intrinsics to use other than unsigned integer types.
- Provides two intrinsics for having side-effects and having no side-effects. The intrinsic function naming convention uses "_se" to describe an intrinsic as having side-effects. A side-effects version is only provided if the instruction does not write `vd`.
- Only non-masked intrinsics are provided, and all VCIX intrinsics have tail agnostic semantics, and no tail policy setting or tu version.

The naming rule of a VCIX instruction is as follows:

<mnemonics>[_se]_u[SEW]m[LMUL]

LMUL := 1 | 2 |4 | 8 | f2 | f4 | f8 SEW := 8 | 16 | 32 | 64

Mnemonics part will transform dot with underline, for example `sf.vc.x` will transform to `sf_vc_x`.

There is no mechanism for describing the cost model and pipeline mode for VCIX intrinsics.

Note

VCIX only provides the tail agnostic version, but the compiler might generate `vsetvli` with tu to optimize the program.

Note

Compiler might reorder the VCIX intrinsics between non-side-effect intrinsics, but will guarantee the order among side-effect intrinsics.

6.1 Example of VCIX Intrinsic Function

Below is an example of the typical VCIX intrinsic:

```
vuint8m2_t __riscv_sf_vc_v_vv_u8m2 (const int bit_field27_26, vuint8m2_t vs2,
vuint8m2_t vs1, size_t vl);
```

This intrinsic compiles to the assembly instruction `sf.vc.vvv <bit-27-26>, vd, vs2, vs1`. This instruction takes as inputs two vector operands and returns a vector result. The `uint8m2` designation means that SEW is set to 8-bit and LMUL is set to 2. The <bit-27-26> field can be used by the designer to implement four different operations for this instruction. If more operations are desired, unused vector operands or immediate fields can be used to encode a larger number of operations. For example the `sf.vc.v.ivv` instruction format has a 5-bit immediate field that can be used for this purpose.

The full list of VCIX intrinsics is provided in Appendix A.

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Glossary

Table 1: *Glossary*

SEW	Selected element width
LMUL	Grouping multiplier
VLEN	Vector register length
EEW	Effective element width

Appendix A

List of VCIX C Intrinsics Functions

The full list of VCIX intrinsics is provided below:

```
void __riscv_sf_vc_x_se_u8mf8 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u8mf4 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u8mf2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u8m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u8m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u8m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u8m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u16mf4 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u16mf2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u16m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u16m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u16m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u16m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u32mf2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u32m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u32m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u32m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u32m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u64m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint64_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u64m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint64_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u64m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint64_t xs1, size_t vl);
```

```
void __riscv_sf_vc_x_se_u64m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint64_t xs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_x_u8mf8 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8mf8_t __riscv_sf_vc_v_x_se_u8mf8 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8mf4_t __riscv_sf_vc_v_x_u8mf4 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8mf4_t __riscv_sf_vc_v_x_se_u8mf4 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8mf2_t __riscv_sf_vc_v_x_u8mf2 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8mf2_t __riscv_sf_vc_v_x_se_u8mf2 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8m1_t __riscv_sf_vc_v_x_u8m1 (int bit_field27_26, int bit_field24_20, uint8_t xs1, size_t
vl);
vuint8m1_t __riscv_sf_vc_v_x_se_u8m1 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8m2_t __riscv_sf_vc_v_x_u8m2 (int bit_field27_26, int bit_field24_20, uint8_t xs1, size_t
vl);
vuint8m2_t __riscv_sf_vc_v_x_se_u8m2 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8m4_t __riscv_sf_vc_v_x_u8m4 (int bit_field27_26, int bit_field24_20, uint8_t xs1, size_t
vl);
vuint8m4_t __riscv_sf_vc_v_x_se_u8m4 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8m8_t __riscv_sf_vc_v_x_u8m8 (int bit_field27_26, int bit_field24_20, uint8_t xs1, size_t
vl);
vuint8m8_t __riscv_sf_vc_v_x_se_u8m8 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_x_u16mf4 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_x_se_u16mf4 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_x_u16mf2 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_x_se_u16mf2 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_x_u16m1 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_x_se_u16m1 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_x_u16m2 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_x_se_u16m2 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_x_u16m4 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_x_se_u16m4 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_x_u16m8 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_x_se_u16m8 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_x_u32mf2 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
```

```
vuint32mf2_t __riscv_sf_vc_v_x_se_u32mf2 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_x_u32m1 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_x_se_u32m1 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_x_u32m2 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_x_se_u32m2 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_x_u32m4 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_x_se_u32m4 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_x_u32m8 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_x_se_u32m8 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_x_u64m1 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_x_se_u64m1 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_x_u64m2 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_x_se_u64m2 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_x_u64m4 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_x_se_u64m4 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_x_u64m8 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_x_se_u64m8 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
void __riscv_sf_vc_i_se_u8mf8 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u8mf4 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u8mf2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u8m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u8m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u8m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u8m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u16mf4 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u16mf2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u16m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u16m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
```

```
void __riscv_sf_vc_i_se_u16m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u16m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u32mf2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u32m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u32m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u32m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u32m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u64m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u64m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u64m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u64m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_i_u8mf8 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8mf8_t __riscv_sf_vc_v_i_se_u8mf8 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint8mf4_t __riscv_sf_vc_v_i_u8mf4 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8mf4_t __riscv_sf_vc_v_i_se_u8mf4 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint8mf2_t __riscv_sf_vc_v_i_u8mf2 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8mf2_t __riscv_sf_vc_v_i_se_u8mf2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint8m1_t __riscv_sf_vc_v_i_u8m1 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m1_t __riscv_sf_vc_v_i_se_u8m1 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m2_t __riscv_sf_vc_v_i_u8m2 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m2_t __riscv_sf_vc_v_i_se_u8m2 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m4_t __riscv_sf_vc_v_i_u8m4 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m4_t __riscv_sf_vc_v_i_se_u8m4 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m8_t __riscv_sf_vc_v_i_u8m8 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m8_t __riscv_sf_vc_v_i_se_u8m8 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint16mf4_t __riscv_sf_vc_v_i_u16mf4 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_i_se_u16mf4 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_i_u16mf2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
```

```
vuint16mf2_t __riscv_sf_vc_v_i_se_u16mf2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_i_u16m1 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint16m1_t __riscv_sf_vc_v_i_se_u16m1 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_i_u16m2 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint16m2_t __riscv_sf_vc_v_i_se_u16m2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_i_u16m4 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint16m4_t __riscv_sf_vc_v_i_se_u16m4 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_i_u16m8 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint16m8_t __riscv_sf_vc_v_i_se_u16m8 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_i_u32mf2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_i_se_u32mf2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_i_u32m1 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint32m1_t __riscv_sf_vc_v_i_se_u32m1 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_i_u32m2 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint32m2_t __riscv_sf_vc_v_i_se_u32m2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_i_u32m4 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint32m4_t __riscv_sf_vc_v_i_se_u32m4 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_i_u32m8 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint32m8_t __riscv_sf_vc_v_i_se_u32m8 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_i_u64m1 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint64m1_t __riscv_sf_vc_v_i_se_u64m1 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_i_u64m2 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint64m2_t __riscv_sf_vc_v_i_se_u64m2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_i_u64m4 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint64m4_t __riscv_sf_vc_v_i_se_u64m4 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_i_u64m8 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint64m8_t __riscv_sf_vc_v_i_se_u64m8 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
void __riscv_sf_vc_vv_se_u8mf8 (int bit_field27_26, int bit_field11_7, vuint8mf8_t vs2,
vuint8mf8_t rs1, size_t vl);
```

```
void __riscv_sf_vc_vv_se_u8mf4 (int bit_field27_26, int bit_field11_7, vuint8mf4_t vs2,
vuint8mf4_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u8mf2 (int bit_field27_26, int bit_field11_7, vuint8mf2_t vs2,
vuint8mf2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u8m1 (int bit_field27_26, int bit_field11_7, vuint8m1_t vs2,
vuint8m1_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u8m2 (int bit_field27_26, int bit_field11_7, vuint8m2_t vs2,
vuint8m2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u8m4 (int bit_field27_26, int bit_field11_7, vuint8m4_t vs2,
vuint8m4_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u8m8 (int bit_field27_26, int bit_field11_7, vuint8m8_t vs2,
vuint8m8_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u16mf4 (int bit_field27_26, int bit_field11_7, vuint16mf4_t vs2,
vuint16mf4_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u16mf2 (int bit_field27_26, int bit_field11_7, vuint16mf2_t vs2,
vuint16mf2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u16m1 (int bit_field27_26, int bit_field11_7, vuint16m1_t vs2,
vuint16m1_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u16m2 (int bit_field27_26, int bit_field11_7, vuint16m2_t vs2,
vuint16m2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u16m4 (int bit_field27_26, int bit_field11_7, vuint16m4_t vs2,
vuint16m4_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u16m8 (int bit_field27_26, int bit_field11_7, vuint16m8_t vs2,
vuint16m8_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u32mf2 (int bit_field27_26, int bit_field11_7, vuint32mf2_t vs2,
vuint32mf2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u32m1 (int bit_field27_26, int bit_field11_7, vuint32m1_t vs2,
vuint32m1_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u32m2 (int bit_field27_26, int bit_field11_7, vuint32m2_t vs2,
vuint32m2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u32m4 (int bit_field27_26, int bit_field11_7, vuint32m4_t vs2,
vuint32m4_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u32m8 (int bit_field27_26, int bit_field11_7, vuint32m8_t vs2,
vuint32m8_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u64m1 (int bit_field27_26, int bit_field11_7, vuint64m1_t vs2,
vuint64m1_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u64m2 (int bit_field27_26, int bit_field11_7, vuint64m2_t vs2,
vuint64m2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u64m4 (int bit_field27_26, int bit_field11_7, vuint64m4_t vs2,
vuint64m4_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u64m8 (int bit_field27_26, int bit_field11_7, vuint64m8_t vs2,
vuint64m8_t rs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_vv_u8mf8 (int bit_field27_26, vuint8mf8_t vs2, vuint8mf8_t rs1,
size_t vl);
vuint8mf8_t __riscv_sf_vc_v_vv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vs2, vuint8mf8_t rs1,
size_t vl);
vuint8mf4_t __riscv_sf_vc_v_vv_u8mf4 (int bit_field27_26, vuint8mf4_t vs2, vuint8mf4_t rs1,
size_t vl);
vuint8mf4_t __riscv_sf_vc_v_vv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vs2, vuint8mf4_t rs1,
size_t vl);
vuint8mf2_t __riscv_sf_vc_v_vv_u8mf2 (int bit_field27_26, vuint8mf2_t vs2, vuint8mf2_t rs1,
size_t vl);
vuint8mf2_t __riscv_sf_vc_v_vv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vs2, vuint8mf2_t rs1,
size_t vl);
vuint8m1_t __riscv_sf_vc_v_vv_u8m1 (int bit_field27_26, vuint8m1_t vs2, vuint8m1_t rs1, size_t
vl);
```

```
vuint8m1_t __riscv_sf_vc_v_vv_se_u8m1 (int bit_field27_26, vuint8m1_t vs2, vuint8m1_t rs1,
size_t vl);
vuint8m2_t __riscv_sf_vc_v_vv_u8m2 (int bit_field27_26, vuint8m2_t vs2, vuint8m2_t rs1, size_t
vl);
vuint8m2_t __riscv_sf_vc_v_vv_se_u8m2 (int bit_field27_26, vuint8m2_t vs2, vuint8m2_t rs1,
size_t vl);
vuint8m4_t __riscv_sf_vc_v_vv_u8m4 (int bit_field27_26, vuint8m4_t vs2, vuint8m4_t rs1, size_t
vl);
vuint8m4_t __riscv_sf_vc_v_vv_se_u8m4 (int bit_field27_26, vuint8m4_t vs2, vuint8m4_t rs1,
size_t vl);
vuint8m8_t __riscv_sf_vc_v_vv_u8m8 (int bit_field27_26, vuint8m8_t vs2, vuint8m8_t rs1, size_t
vl);
vuint8m8_t __riscv_sf_vc_v_vv_se_u8m8 (int bit_field27_26, vuint8m8_t vs2, vuint8m8_t rs1,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_vv_u16mf4 (int bit_field27_26, vuint16mf4_t vs2, vuint16mf4_t rs1,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_vv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vs2, vuint16mf4_t
rs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_vv_u16mf2 (int bit_field27_26, vuint16mf2_t vs2, vuint16mf2_t rs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_vv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vs2, vuint16mf2_t
rs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_vv_u16m1 (int bit_field27_26, vuint16m1_t vs2, vuint16m1_t rs1,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_vv_se_u16m1 (int bit_field27_26, vuint16m1_t vs2, vuint16m1_t rs1,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_vv_u16m2 (int bit_field27_26, vuint16m2_t vs2, vuint16m2_t rs1,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_vv_se_u16m2 (int bit_field27_26, vuint16m2_t vs2, vuint16m2_t rs1,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_vv_u16m4 (int bit_field27_26, vuint16m4_t vs2, vuint16m4_t rs1,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_vv_se_u16m4 (int bit_field27_26, vuint16m4_t vs2, vuint16m4_t rs1,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_vv_u16m8 (int bit_field27_26, vuint16m8_t vs2, vuint16m8_t rs1,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_vv_se_u16m8 (int bit_field27_26, vuint16m8_t vs2, vuint16m8_t rs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_vv_u32mf2 (int bit_field27_26, vuint32mf2_t vs2, vuint32mf2_t rs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_vv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vs2, vuint32mf2_t
rs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_vv_u32m1 (int bit_field27_26, vuint32m1_t vs2, vuint32m1_t rs1,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_vv_se_u32m1 (int bit_field27_26, vuint32m1_t vs2, vuint32m1_t rs1,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_vv_u32m2 (int bit_field27_26, vuint32m2_t vs2, vuint32m2_t rs1,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_vv_se_u32m2 (int bit_field27_26, vuint32m2_t vs2, vuint32m2_t rs1,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_vv_u32m4 (int bit_field27_26, vuint32m4_t vs2, vuint32m4_t rs1,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_vv_se_u32m4 (int bit_field27_26, vuint32m4_t vs2, vuint32m4_t rs1,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_vv_u32m8 (int bit_field27_26, vuint32m8_t vs2, vuint32m8_t rs1,
size_t vl);
```

```
vuint32m8_t __riscv_sf_vc_v_vv_se_u32m8 (int bit_field27_26, vuint32m8_t vs2, vuint32m8_t rs1,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_vv_u64m1 (int bit_field27_26, vuint64m1_t vs2, vuint64m1_t rs1,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_vv_se_u64m1 (int bit_field27_26, vuint64m1_t vs2, vuint64m1_t rs1,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_vv_u64m2 (int bit_field27_26, vuint64m2_t vs2, vuint64m2_t rs1,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_vv_se_u64m2 (int bit_field27_26, vuint64m2_t vs2, vuint64m2_t rs1,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_vv_u64m4 (int bit_field27_26, vuint64m4_t vs2, vuint64m4_t rs1,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_vv_se_u64m4 (int bit_field27_26, vuint64m4_t vs2, vuint64m4_t rs1,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_vv_u64m8 (int bit_field27_26, vuint64m8_t vs2, vuint64m8_t rs1,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_vv_se_u64m8 (int bit_field27_26, vuint64m8_t vs2, vuint64m8_t rs1,
size_t vl);
void __riscv_sf_vc_xv_se_u8mf8 (int bit_field27_26, int bit_field11_7, vuint8mf8_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u8mf4 (int bit_field27_26, int bit_field11_7, vuint8mf4_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u8mf2 (int bit_field27_26, int bit_field11_7, vuint8mf2_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u8m1 (int bit_field27_26, int bit_field11_7, vuint8m1_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u8m2 (int bit_field27_26, int bit_field11_7, vuint8m2_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u8m4 (int bit_field27_26, int bit_field11_7, vuint8m4_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u8m8 (int bit_field27_26, int bit_field11_7, vuint8m8_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u16mf4 (int bit_field27_26, int bit_field11_7, vuint16mf4_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u16mf2 (int bit_field27_26, int bit_field11_7, vuint16mf2_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u16m1 (int bit_field27_26, int bit_field11_7, vuint16m1_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u16m2 (int bit_field27_26, int bit_field11_7, vuint16m2_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u16m4 (int bit_field27_26, int bit_field11_7, vuint16m4_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u16m8 (int bit_field27_26, int bit_field11_7, vuint16m8_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u32mf2 (int bit_field27_26, int bit_field11_7, vuint32mf2_t vs2,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u32m1 (int bit_field27_26, int bit_field11_7, vuint32m1_t vs2,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u32m2 (int bit_field27_26, int bit_field11_7, vuint32m2_t vs2,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u32m4 (int bit_field27_26, int bit_field11_7, vuint32m4_t vs2,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u32m8 (int bit_field27_26, int bit_field11_7, vuint32m8_t vs2,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u64m1 (int bit_field27_26, int bit_field11_7, vuint64m1_t vs2,
uint64_t xs1, size_t vl);
```

```
void __riscv_sf_vc_xv_se_u64m2 (int bit_field27_26, int bit_field11_7, vuint64m2_t vs2,
uint64_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u64m4 (int bit_field27_26, int bit_field11_7, vuint64m4_t vs2,
uint64_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u64m8 (int bit_field27_26, int bit_field11_7, vuint64m8_t vs2,
uint64_t xs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_xv_u8mf8 (int bit_field27_26, vuint8mf8_t vs2, uint8_t xs1, size_t
vl);
vuint8mf8_t __riscv_sf_vc_v_xv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vs2, uint8_t xs1,
size_t vl);
vuint8mf4_t __riscv_sf_vc_v_xv_u8mf4 (int bit_field27_26, vuint8mf4_t vs2, uint8_t xs1, size_t
vl);
vuint8mf4_t __riscv_sf_vc_v_xv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vs2, uint8_t xs1,
size_t vl);
vuint8mf2_t __riscv_sf_vc_v_xv_u8mf2 (int bit_field27_26, vuint8mf2_t vs2, uint8_t xs1, size_t
vl);
vuint8mf2_t __riscv_sf_vc_v_xv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vs2, uint8_t xs1,
size_t vl);
vuint8m1_t __riscv_sf_vc_v_xv_u8m1 (int bit_field27_26, vuint8m1_t vs2, uint8_t xs1, size_t vl);
vuint8m1_t __riscv_sf_vc_v_xv_se_u8m1 (int bit_field27_26, vuint8m1_t vs2, uint8_t xs1, size_t
vl);
vuint8m2_t __riscv_sf_vc_v_xv_u8m2 (int bit_field27_26, vuint8m2_t vs2, uint8_t xs1, size_t vl);
vuint8m2_t __riscv_sf_vc_v_xv_se_u8m2 (int bit_field27_26, vuint8m2_t vs2, uint8_t xs1, size_t
vl);
vuint8m4_t __riscv_sf_vc_v_xv_u8m4 (int bit_field27_26, vuint8m4_t vs2, uint8_t xs1, size_t vl);
vuint8m4_t __riscv_sf_vc_v_xv_se_u8m4 (int bit_field27_26, vuint8m4_t vs2, uint8_t xs1, size_t
vl);
vuint8m8_t __riscv_sf_vc_v_xv_u8m8 (int bit_field27_26, vuint8m8_t vs2, uint8_t xs1, size_t vl);
vuint8m8_t __riscv_sf_vc_v_xv_se_u8m8 (int bit_field27_26, vuint8m8_t vs2, uint8_t xs1, size_t
vl);
vuint16mf4_t __riscv_sf_vc_v_xv_u16mf4 (int bit_field27_26, vuint16mf4_t vs2, uint16_t xs1,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_xv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vs2, uint16_t xs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_xv_u16mf2 (int bit_field27_26, vuint16mf2_t vs2, uint16_t xs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_xv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vs2, uint16_t xs1,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_xv_u16m1 (int bit_field27_26, vuint16m1_t vs2, uint16_t xs1, size_t
vl);
vuint16m1_t __riscv_sf_vc_v_xv_se_u16m1 (int bit_field27_26, vuint16m1_t vs2, uint16_t xs1,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_xv_u16m2 (int bit_field27_26, vuint16m2_t vs2, uint16_t xs1, size_t
vl);
vuint16m2_t __riscv_sf_vc_v_xv_se_u16m2 (int bit_field27_26, vuint16m2_t vs2, uint16_t xs1,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_xv_u16m4 (int bit_field27_26, vuint16m4_t vs2, uint16_t xs1, size_t
vl);
vuint16m4_t __riscv_sf_vc_v_xv_se_u16m4 (int bit_field27_26, vuint16m4_t vs2, uint16_t xs1,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_xv_u16m8 (int bit_field27_26, vuint16m8_t vs2, uint16_t xs1, size_t
vl);
vuint16m8_t __riscv_sf_vc_v_xv_se_u16m8 (int bit_field27_26, vuint16m8_t vs2, uint16_t xs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_xv_u32mf2 (int bit_field27_26, vuint32mf2_t vs2, uint32_t xs1,
size_t vl);
```

```
vuint32mf2_t __riscv_sf_vc_v_xv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vs2, uint32_t xs1,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_xv_u32m1 (int bit_field27_26, vuint32m1_t vs2, uint32_t xs1, size_t
vl);
vuint32m1_t __riscv_sf_vc_v_xv_se_u32m1 (int bit_field27_26, vuint32m1_t vs2, uint32_t xs1,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_xv_u32m2 (int bit_field27_26, vuint32m2_t vs2, uint32_t xs1, size_t
vl);
vuint32m2_t __riscv_sf_vc_v_xv_se_u32m2 (int bit_field27_26, vuint32m2_t vs2, uint32_t xs1,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_xv_u32m4 (int bit_field27_26, vuint32m4_t vs2, uint32_t xs1, size_t
vl);
vuint32m4_t __riscv_sf_vc_v_xv_se_u32m4 (int bit_field27_26, vuint32m4_t vs2, uint32_t xs1,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_xv_u32m8 (int bit_field27_26, vuint32m8_t vs2, uint32_t xs1, size_t
vl);
vuint32m8_t __riscv_sf_vc_v_xv_se_u32m8 (int bit_field27_26, vuint32m8_t vs2, uint32_t xs1,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_xv_u64m1 (int bit_field27_26, vuint64m1_t vs2, uint64_t xs1, size_t
vl);
vuint64m1_t __riscv_sf_vc_v_xv_se_u64m1 (int bit_field27_26, vuint64m1_t vs2, uint64_t xs1,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_xv_u64m2 (int bit_field27_26, vuint64m2_t vs2, uint64_t xs1, size_t
vl);
vuint64m2_t __riscv_sf_vc_v_xv_se_u64m2 (int bit_field27_26, vuint64m2_t vs2, uint64_t xs1,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_xv_u64m4 (int bit_field27_26, vuint64m4_t vs2, uint64_t xs1, size_t
vl);
vuint64m4_t __riscv_sf_vc_v_xv_se_u64m4 (int bit_field27_26, vuint64m4_t vs2, uint64_t xs1,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_xv_u64m8 (int bit_field27_26, vuint64m8_t vs2, uint64_t xs1, size_t
vl);
vuint64m8_t __riscv_sf_vc_v_xv_se_u64m8 (int bit_field27_26, vuint64m8_t vs2, uint64_t xs1,
size_t vl);
void __riscv_sf_vc_iv_se_u8mf8 (int bit_field27_26, int bit_field11_7, vuint8mf8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u8mf4 (int bit_field27_26, int bit_field11_7, vuint8mf4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u8mf2 (int bit_field27_26, int bit_field11_7, vuint8mf2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u8m1 (int bit_field27_26, int bit_field11_7, vuint8m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u8m2 (int bit_field27_26, int bit_field11_7, vuint8m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u8m4 (int bit_field27_26, int bit_field11_7, vuint8m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u8m8 (int bit_field27_26, int bit_field11_7, vuint8m8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u16mf4 (int bit_field27_26, int bit_field11_7, vuint16mf4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u16mf2 (int bit_field27_26, int bit_field11_7, vuint16mf2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u16m1 (int bit_field27_26, int bit_field11_7, vuint16m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u16m2 (int bit_field27_26, int bit_field11_7, vuint16m2_t vs2, int
simm5, size_t vl);
```

```
void __riscv_sf_vc_iv_se_u16m4 (int bit_field27_26, int bit_field11_7, vuint16m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u16m8 (int bit_field27_26, int bit_field11_7, vuint16m8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u32mf2 (int bit_field27_26, int bit_field11_7, vuint32mf2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u32m1 (int bit_field27_26, int bit_field11_7, vuint32m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u32m2 (int bit_field27_26, int bit_field11_7, vuint32m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u32m4 (int bit_field27_26, int bit_field11_7, vuint32m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u32m8 (int bit_field27_26, int bit_field11_7, vuint32m8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u64m1 (int bit_field27_26, int bit_field11_7, vuint64m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u64m2 (int bit_field27_26, int bit_field11_7, vuint64m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u64m4 (int bit_field27_26, int bit_field11_7, vuint64m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u64m8 (int bit_field27_26, int bit_field11_7, vuint64m8_t vs2, int
simm5, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_iv_u8mf8 (int bit_field27_26, vuint8mf8_t vs2, int simm5, size_t
vl);
vuint8mf8_t __riscv_sf_vc_v_iv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vs2, int simm5, size_t
vl);
vuint8mf4_t __riscv_sf_vc_v_iv_u8mf4 (int bit_field27_26, vuint8mf4_t vs2, int simm5, size_t
vl);
vuint8mf4_t __riscv_sf_vc_v_iv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vs2, int simm5, size_t
vl);
vuint8mf2_t __riscv_sf_vc_v_iv_u8mf2 (int bit_field27_26, vuint8mf2_t vs2, int simm5, size_t
vl);
vuint8mf2_t __riscv_sf_vc_v_iv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vs2, int simm5, size_t
vl);
vuint8m1_t __riscv_sf_vc_v_iv_u8m1 (int bit_field27_26, vuint8m1_t vs2, int simm5, size_t vl);
vuint8m1_t __riscv_sf_vc_v_iv_se_u8m1 (int bit_field27_26, vuint8m1_t vs2, int simm5, size_t
vl);
vuint8m2_t __riscv_sf_vc_v_iv_u8m2 (int bit_field27_26, vuint8m2_t vs2, int simm5, size_t vl);
vuint8m2_t __riscv_sf_vc_v_iv_se_u8m2 (int bit_field27_26, vuint8m2_t vs2, int simm5, size_t
vl);
vuint8m4_t __riscv_sf_vc_v_iv_u8m4 (int bit_field27_26, vuint8m4_t vs2, int simm5, size_t vl);
vuint8m4_t __riscv_sf_vc_v_iv_se_u8m4 (int bit_field27_26, vuint8m4_t vs2, int simm5, size_t
vl);
vuint8m8_t __riscv_sf_vc_v_iv_u8m8 (int bit_field27_26, vuint8m8_t vs2, int simm5, size_t vl);
vuint8m8_t __riscv_sf_vc_v_iv_se_u8m8 (int bit_field27_26, vuint8m8_t vs2, int simm5, size_t
vl);
vuint16mf4_t __riscv_sf_vc_v_iv_u16mf4 (int bit_field27_26, vuint16mf4_t vs2, int simm5, size_t
vl);
vuint16mf4_t __riscv_sf_vc_v_iv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vs2, int simm5,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_iv_u16mf2 (int bit_field27_26, vuint16mf2_t vs2, int simm5, size_t
vl);
vuint16mf2_t __riscv_sf_vc_v_iv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vs2, int simm5,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_iv_u16m1 (int bit_field27_26, vuint16m1_t vs2, int simm5, size_t
vl);
```

```
vuint16m1_t __riscv_sf_vc_v_iv_se_u16m1 (int bit_field27_26, vuint16m1_t vs2, int simm5, size_t
vl);
vuint16m2_t __riscv_sf_vc_v_iv_u16m2 (int bit_field27_26, vuint16m2_t vs2, int simm5, size_t
vl);
vuint16m2_t __riscv_sf_vc_v_iv_se_u16m2 (int bit_field27_26, vuint16m2_t vs2, int simm5, size_t
vl);
vuint16m4_t __riscv_sf_vc_v_iv_u16m4 (int bit_field27_26, vuint16m4_t vs2, int simm5, size_t
vl);
vuint16m4_t __riscv_sf_vc_v_iv_se_u16m4 (int bit_field27_26, vuint16m4_t vs2, int simm5, size_t
vl);
vuint16m8_t __riscv_sf_vc_v_iv_u16m8 (int bit_field27_26, vuint16m8_t vs2, int simm5, size_t
vl);
vuint16m8_t __riscv_sf_vc_v_iv_se_u16m8 (int bit_field27_26, vuint16m8_t vs2, int simm5, size_t
vl);
vuint32mf2_t __riscv_sf_vc_v_iv_u32mf2 (int bit_field27_26, vuint32mf2_t vs2, int simm5, size_t
vl);
vuint32mf2_t __riscv_sf_vc_v_iv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vs2, int simm5,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_iv_u32m1 (int bit_field27_26, vuint32m1_t vs2, int simm5, size_t
vl);
vuint32m1_t __riscv_sf_vc_v_iv_se_u32m1 (int bit_field27_26, vuint32m1_t vs2, int simm5, size_t
vl);
vuint32m2_t __riscv_sf_vc_v_iv_u32m2 (int bit_field27_26, vuint32m2_t vs2, int simm5, size_t
vl);
vuint32m2_t __riscv_sf_vc_v_iv_se_u32m2 (int bit_field27_26, vuint32m2_t vs2, int simm5, size_t
vl);
vuint32m4_t __riscv_sf_vc_v_iv_u32m4 (int bit_field27_26, vuint32m4_t vs2, int simm5, size_t
vl);
vuint32m4_t __riscv_sf_vc_v_iv_se_u32m4 (int bit_field27_26, vuint32m4_t vs2, int simm5, size_t
vl);
vuint32m8_t __riscv_sf_vc_v_iv_u32m8 (int bit_field27_26, vuint32m8_t vs2, int simm5, size_t
vl);
vuint32m8_t __riscv_sf_vc_v_iv_se_u32m8 (int bit_field27_26, vuint32m8_t vs2, int simm5, size_t
vl);
vuint64m1_t __riscv_sf_vc_v_iv_u64m1 (int bit_field27_26, vuint64m1_t vs2, int simm5, size_t
vl);
vuint64m1_t __riscv_sf_vc_v_iv_se_u64m1 (int bit_field27_26, vuint64m1_t vs2, int simm5, size_t
vl);
vuint64m2_t __riscv_sf_vc_v_iv_u64m2 (int bit_field27_26, vuint64m2_t vs2, int simm5, size_t
vl);
vuint64m2_t __riscv_sf_vc_v_iv_se_u64m2 (int bit_field27_26, vuint64m2_t vs2, int simm5, size_t
vl);
vuint64m4_t __riscv_sf_vc_v_iv_u64m4 (int bit_field27_26, vuint64m4_t vs2, int simm5, size_t
vl);
vuint64m4_t __riscv_sf_vc_v_iv_se_u64m4 (int bit_field27_26, vuint64m4_t vs2, int simm5, size_t
vl);
vuint64m8_t __riscv_sf_vc_v_iv_u64m8 (int bit_field27_26, vuint64m8_t vs2, int simm5, size_t
vl);
vuint64m8_t __riscv_sf_vc_v_iv_se_u64m8 (int bit_field27_26, vuint64m8_t vs2, int simm5, size_t
vl);
void __riscv_sf_vc_fv_se_u16mf4 (int bit_field26, int bit_field11_7, vuint16mf4_t vs2,
float16_t fs1, size_t vl);
void __riscv_sf_vc_fv_se_u16mf2 (int bit_field26, int bit_field11_7, vuint16mf2_t vs2,
float16_t fs1, size_t vl);
void __riscv_sf_vc_fv_se_u16m1 (int bit_field26, int bit_field11_7, vuint16m1_t vs2, float16_t
fs1, size_t vl);
```

```
void __riscv_sf_vc_fv_se_u16m2 (int bit_field26, int bit_field11_7, vuint16m2_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u16m4 (int bit_field26, int bit_field11_7, vuint16m4_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u16m8 (int bit_field26, int bit_field11_7, vuint16m8_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u32mf2 (int bit_field26, int bit_field11_7, vuint32mf2_t vs2,
float32_t fs1, size_t vl);
void __riscv_sf_vc_fv_se_u32m1 (int bit_field26, int bit_field11_7, vuint32m1_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u32m2 (int bit_field26, int bit_field11_7, vuint32m2_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u32m4 (int bit_field26, int bit_field11_7, vuint32m4_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u32m8 (int bit_field26, int bit_field11_7, vuint32m8_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u64m1 (int bit_field26, int bit_field11_7, vuint64m1_t vs2, float64_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u64m2 (int bit_field26, int bit_field11_7, vuint64m2_t vs2, float64_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u64m4 (int bit_field26, int bit_field11_7, vuint64m4_t vs2, float64_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u64m8 (int bit_field26, int bit_field11_7, vuint64m8_t vs2, float64_t
fs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_fv_u16mf4 (int bit_field26, vuint16mf4_t vs2, float16_t fs1,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_fv_se_u16mf4 (int bit_field26, vuint16mf4_t vs2, float16_t fs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_fv_u16mf2 (int bit_field26, vuint16mf2_t vs2, float16_t fs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_fv_se_u16mf2 (int bit_field26, vuint16mf2_t vs2, float16_t fs1,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_fv_u16m1 (int bit_field26, vuint16m1_t vs2, float16_t fs1, size_t
vl);
vuint16m1_t __riscv_sf_vc_v_fv_se_u16m1 (int bit_field26, vuint16m1_t vs2, float16_t fs1,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_fv_u16m2 (int bit_field26, vuint16m2_t vs2, float16_t fs1, size_t
vl);
vuint16m2_t __riscv_sf_vc_v_fv_se_u16m2 (int bit_field26, vuint16m2_t vs2, float16_t fs1,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_fv_u16m4 (int bit_field26, vuint16m4_t vs2, float16_t fs1, size_t
vl);
vuint16m4_t __riscv_sf_vc_v_fv_se_u16m4 (int bit_field26, vuint16m4_t vs2, float16_t fs1,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_fv_u16m8 (int bit_field26, vuint16m8_t vs2, float16_t fs1, size_t
vl);
vuint16m8_t __riscv_sf_vc_v_fv_se_u16m8 (int bit_field26, vuint16m8_t vs2, float16_t fs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_fv_u32mf2 (int bit_field26, vuint32mf2_t vs2, float32_t fs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_fv_se_u32mf2 (int bit_field26, vuint32mf2_t vs2, float32_t fs1,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_fv_u32m1 (int bit_field26, vuint32m1_t vs2, float32_t fs1, size_t
vl);
vuint32m1_t __riscv_sf_vc_v_fv_se_u32m1 (int bit_field26, vuint32m1_t vs2, float32_t fs1,
size_t vl);
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vuint32m2_t __riscv_sf_vc_v_fv_u32m2 (int bit_field26, vuint32m2_t vs2, float32_t fs1, size_t
vl);
vuint32m2_t __riscv_sf_vc_v_fv_se_u32m2 (int bit_field26, vuint32m2_t vs2, float32_t fs1,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_fv_u32m4 (int bit_field26, vuint32m4_t vs2, float32_t fs1, size_t
vl);
vuint32m4_t __riscv_sf_vc_v_fv_se_u32m4 (int bit_field26, vuint32m4_t vs2, float32_t fs1,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_fv_u32m8 (int bit_field26, vuint32m8_t vs2, float32_t fs1, size_t
vl);
vuint32m8_t __riscv_sf_vc_v_fv_se_u32m8 (int bit_field26, vuint32m8_t vs2, float32_t fs1,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_fv_u64m1 (int bit_field26, vuint64m1_t vs2, float64_t fs1, size_t
vl);
vuint64m1_t __riscv_sf_vc_v_fv_se_u64m1 (int bit_field26, vuint64m1_t vs2, float64_t fs1,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_fv_u64m2 (int bit_field26, vuint64m2_t vs2, float64_t fs1, size_t
vl);
vuint64m2_t __riscv_sf_vc_v_fv_se_u64m2 (int bit_field26, vuint64m2_t vs2, float64_t fs1,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_fv_u64m4 (int bit_field26, vuint64m4_t vs2, float64_t fs1, size_t
vl);
vuint64m4_t __riscv_sf_vc_v_fv_se_u64m4 (int bit_field26, vuint64m4_t vs2, float64_t fs1,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_fv_u64m8 (int bit_field26, vuint64m8_t vs2, float64_t fs1, size_t
vl);
vuint64m8_t __riscv_sf_vc_v_fv_se_u64m8 (int bit_field26, vuint64m8_t vs2, float64_t fs1,
size_t vl);
void __riscv_sf_vc_vvv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2,
vuint8mf8_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2,
vuint8mf4_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2,
vuint8mf2_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2, vuint8m1_t
rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2, vuint8m2_t
rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2, vuint8m4_t
rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2, vuint8m8_t
rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t vs2,
vuint16mf4_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t vs2,
vuint16mf2_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2,
vuint16m1_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2,
vuint16m2_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2,
vuint16m4_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2,
vuint16m8_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t vs2,
vuint32mf2_t rs1, size_t vl);
```

```
void __riscv_sf_vc_vvv_se_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2,
vuint32m1_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2,
vuint32m2_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2,
vuint32m4_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2,
vuint32m8_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2,
vuint64m1_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2,
vuint64m2_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2,
vuint64m4_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2,
vuint64m8_t rs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_vvv_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2,
vuint8mf8_t rs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_vvv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2,
vuint8mf8_t rs1, size_t vl);
vuint8mf4_t __riscv_sf_vc_v_vvv_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2,
vuint8mf4_t rs1, size_t vl);
vuint8mf4_t __riscv_sf_vc_v_vvv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2,
vuint8mf4_t rs1, size_t vl);
vuint8mf2_t __riscv_sf_vc_v_vvv_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2,
vuint8mf2_t rs1, size_t vl);
vuint8mf2_t __riscv_sf_vc_v_vvv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2,
vuint8mf2_t rs1, size_t vl);
vuint8m1_t __riscv_sf_vc_v_vvv_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2,
vuint8m1_t rs1, size_t vl);
vuint8m1_t __riscv_sf_vc_v_vvv_se_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2,
vuint8m1_t rs1, size_t vl);
vuint8m2_t __riscv_sf_vc_v_vvv_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2,
vuint8m2_t rs1, size_t vl);
vuint8m2_t __riscv_sf_vc_v_vvv_se_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2,
vuint8m2_t rs1, size_t vl);
vuint8m4_t __riscv_sf_vc_v_vvv_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2,
vuint8m4_t rs1, size_t vl);
vuint8m4_t __riscv_sf_vc_v_vvv_se_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2,
vuint8m4_t rs1, size_t vl);
vuint8m8_t __riscv_sf_vc_v_vvv_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2,
vuint8m8_t rs1, size_t vl);
vuint8m8_t __riscv_sf_vc_v_vvv_se_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2,
vuint8m8_t rs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_vvv_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t vs2,
vuint16mf4_t rs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_vvv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t
vs2, vuint16mf4_t rs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_vvv_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t vs2,
vuint16mf2_t rs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_vvv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t
vs2, vuint16mf2_t rs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_vvv_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2,
vuint16m1_t rs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_vvv_se_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2,
vuint16m1_t rs1, size_t vl);
```

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vuint16m2_t __riscv_sf_vc_v_vvv_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2,
vuint16m2_t rs1, size_t vl);
vuint16m2_t __riscv_sf_vc_v_vvv_se_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2,
vuint16m2_t rs1, size_t vl);
vuint16m4_t __riscv_sf_vc_v_vvv_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2,
vuint16m4_t rs1, size_t vl);
vuint16m4_t __riscv_sf_vc_v_vvv_se_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2,
vuint16m4_t rs1, size_t vl);
vuint16m8_t __riscv_sf_vc_v_vvv_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2,
vuint16m8_t rs1, size_t vl);
vuint16m8_t __riscv_sf_vc_v_vvv_se_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2,
vuint16m8_t rs1, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_vvv_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t vs2,
vuint32mf2_t rs1, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_vvv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t
vs2, vuint32mf2_t rs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_vvv_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2,
vuint32m1_t rs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_vvv_se_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2,
vuint32m1_t rs1, size_t vl);
vuint32m2_t __riscv_sf_vc_v_vvv_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2,
vuint32m2_t rs1, size_t vl);
vuint32m2_t __riscv_sf_vc_v_vvv_se_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2,
vuint32m2_t rs1, size_t vl);
vuint32m4_t __riscv_sf_vc_v_vvv_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2,
vuint32m4_t rs1, size_t vl);
vuint32m4_t __riscv_sf_vc_v_vvv_se_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2,
vuint32m4_t rs1, size_t vl);
vuint32m8_t __riscv_sf_vc_v_vvv_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2,
vuint32m8_t rs1, size_t vl);
vuint32m8_t __riscv_sf_vc_v_vvv_se_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2,
vuint32m8_t rs1, size_t vl);
vuint64m1_t __riscv_sf_vc_v_vvv_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2,
vuint64m1_t rs1, size_t vl);
vuint64m1_t __riscv_sf_vc_v_vvv_se_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2,
vuint64m1_t rs1, size_t vl);
vuint64m2_t __riscv_sf_vc_v_vvv_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2,
vuint64m2_t rs1, size_t vl);
vuint64m2_t __riscv_sf_vc_v_vvv_se_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2,
vuint64m2_t rs1, size_t vl);
vuint64m4_t __riscv_sf_vc_v_vvv_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2,
vuint64m4_t rs1, size_t vl);
vuint64m4_t __riscv_sf_vc_v_vvv_se_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2,
vuint64m4_t rs1, size_t vl);
vuint64m8_t __riscv_sf_vc_v_vvv_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2,
vuint64m8_t rs1, size_t vl);
vuint64m8_t __riscv_sf_vc_v_vvv_se_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2,
vuint64m8_t rs1, size_t vl);
void __riscv_sf_vc_xvv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2, uint8_t xs1,
size_t vl);
```

```
void __riscv_sf_vc_xvv_se_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2, uint8_t xs1,
size_t vl);
void __riscv_sf_vc_xvv_se_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2, uint8_t xs1,
size_t vl);
void __riscv_sf_vc_xvv_se_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2, uint8_t xs1,
size_t vl);
void __riscv_sf_vc_xvv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2, uint16_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2, uint16_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2, uint16_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2, uint16_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t vs2,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2, uint32_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2, uint32_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2, uint32_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2, uint32_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2, uint64_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2, uint64_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2, uint64_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2, uint64_t
xs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_xvv_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2,
uint8_t xs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_xvv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2,
uint8_t xs1, size_t vl);
vuint8mf4_t __riscv_sf_vc_v_xvv_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2,
uint8_t xs1, size_t vl);
vuint8mf4_t __riscv_sf_vc_v_xvv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2,
uint8_t xs1, size_t vl);
vuint8mf2_t __riscv_sf_vc_v_xvv_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2,
uint8_t xs1, size_t vl);
vuint8mf2_t __riscv_sf_vc_v_xvv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2,
uint8_t xs1, size_t vl);
vuint8m1_t __riscv_sf_vc_v_xvv_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2, uint8_t
xs1, size_t vl);
vuint8m1_t __riscv_sf_vc_v_xvv_se_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2,
uint8_t xs1, size_t vl);
vuint8m2_t __riscv_sf_vc_v_xvv_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2, uint8_t
xs1, size_t vl);
vuint8m2_t __riscv_sf_vc_v_xvv_se_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2,
uint8_t xs1, size_t vl);
```

```
vuint8m4_t __riscv_sf_vc_v_xvv_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2, uint8_t
xs1, size_t vl);
vuint8m4_t __riscv_sf_vc_v_xvv_se_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2,
uint8_t xs1, size_t vl);
vuint8m8_t __riscv_sf_vc_v_xvv_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2, uint8_t
xs1, size_t vl);
vuint8m8_t __riscv_sf_vc_v_xvv_se_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2,
uint8_t xs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_xvv_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t vs2,
uint16_t xs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_xvv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t
vs2, uint16_t xs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_xvv_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t vs2,
uint16_t xs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_xvv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t
vs2, uint16_t xs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_xvv_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2,
uint16_t xs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_xvv_se_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2,
uint16_t xs1, size_t vl);
vuint16m2_t __riscv_sf_vc_v_xvv_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2,
uint16_t xs1, size_t vl);
vuint16m2_t __riscv_sf_vc_v_xvv_se_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2,
uint16_t xs1, size_t vl);
vuint16m4_t __riscv_sf_vc_v_xvv_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2,
uint16_t xs1, size_t vl);
vuint16m4_t __riscv_sf_vc_v_xvv_se_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2,
uint16_t xs1, size_t vl);
vuint16m8_t __riscv_sf_vc_v_xvv_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2,
uint16_t xs1, size_t vl);
vuint16m8_t __riscv_sf_vc_v_xvv_se_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2,
uint16_t xs1, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_xvv_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t vs2,
uint32_t xs1, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_xvv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t
vs2, uint32_t xs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_xvv_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2,
uint32_t xs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_xvv_se_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2,
uint32_t xs1, size_t vl);
vuint32m2_t __riscv_sf_vc_v_xvv_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2,
uint32_t xs1, size_t vl);
vuint32m2_t __riscv_sf_vc_v_xvv_se_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2,
uint32_t xs1, size_t vl);
vuint32m4_t __riscv_sf_vc_v_xvv_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2,
uint32_t xs1, size_t vl);
vuint32m4_t __riscv_sf_vc_v_xvv_se_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2,
uint32_t xs1, size_t vl);
vuint32m8_t __riscv_sf_vc_v_xvv_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2,
uint32_t xs1, size_t vl);
vuint32m8_t __riscv_sf_vc_v_xvv_se_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2,
uint32_t xs1, size_t vl);
vuint64m1_t __riscv_sf_vc_v_xvv_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2,
uint64_t xs1, size_t vl);
vuint64m1_t __riscv_sf_vc_v_xvv_se_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2,
uint64_t xs1, size_t vl);
```

```
vuint64m2_t __riscv_sf_vc_v_xvv_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2,
uint64_t xs1, size_t vl);
vuint64m2_t __riscv_sf_vc_v_xvv_se_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2,
uint64_t xs1, size_t vl);
vuint64m4_t __riscv_sf_vc_v_xvv_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2,
uint64_t xs1, size_t vl);
vuint64m4_t __riscv_sf_vc_v_xvv_se_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2,
uint64_t xs1, size_t vl);
vuint64m8_t __riscv_sf_vc_v_xvv_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2,
uint64_t xs1, size_t vl);
vuint64m8_t __riscv_sf_vc_v_xvv_se_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2,
uint64_t xs1, size_t vl);
void __riscv_sf_vc_ivv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2, int simm5,
size_t vl);
void __riscv_sf_vc_ivv_se_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2, int simm5,
size_t vl);
void __riscv_sf_vc_ivv_se_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2, int simm5,
size_t vl);
void __riscv_sf_vc_ivv_se_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2, int simm5,
size_t vl);
void __riscv_sf_vc_ivv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2, int
simm5, size_t vl);
```

```
vuint8mf8_t __riscv_sf_vc_v_ivv_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2, int
simm5, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_ivv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2,
int simm5, size_t vl);
vuint8mf4_t __riscv_sf_vc_v_ivv_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2, int
simm5, size_t vl);
vuint8mf4_t __riscv_sf_vc_v_ivv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2,
int simm5, size_t vl);
vuint8mf2_t __riscv_sf_vc_v_ivv_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2, int
simm5, size_t vl);
vuint8mf2_t __riscv_sf_vc_v_ivv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2,
int simm5, size_t vl);
vuint8m1_t __riscv_sf_vc_v_ivv_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2, int
simm5, size_t vl);
vuint8m1_t __riscv_sf_vc_v_ivv_se_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2, int
simm5, size_t vl);
vuint8m2_t __riscv_sf_vc_v_ivv_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2, int
simm5, size_t vl);
vuint8m2_t __riscv_sf_vc_v_ivv_se_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2, int
simm5, size_t vl);
vuint8m4_t __riscv_sf_vc_v_ivv_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2, int
simm5, size_t vl);
vuint8m4_t __riscv_sf_vc_v_ivv_se_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2, int
simm5, size_t vl);
vuint8m8_t __riscv_sf_vc_v_ivv_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2, int
simm5, size_t vl);
vuint8m8_t __riscv_sf_vc_v_ivv_se_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2, int
simm5, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_ivv_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t vs2,
int simm5, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_ivv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t
vs2, int simm5, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_ivv_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t vs2,
int simm5, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_ivv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t
vs2, int simm5, size_t vl);
vuint16m1_t __riscv_sf_vc_v_ivv_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2, int
simm5, size_t vl);
vuint16m1_t __riscv_sf_vc_v_ivv_se_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2,
int simm5, size_t vl);
vuint16m2_t __riscv_sf_vc_v_ivv_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2, int
simm5, size_t vl);
vuint16m2_t __riscv_sf_vc_v_ivv_se_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2,
int simm5, size_t vl);
vuint16m4_t __riscv_sf_vc_v_ivv_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2, int
simm5, size_t vl);
vuint16m4_t __riscv_sf_vc_v_ivv_se_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2,
int simm5, size_t vl);
vuint16m8_t __riscv_sf_vc_v_ivv_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2, int
simm5, size_t vl);
vuint16m8_t __riscv_sf_vc_v_ivv_se_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2,
int simm5, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_ivv_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t vs2,
int simm5, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_ivv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t
vs2, int simm5, size_t vl);
```

```
vuint32m1_t __riscv_sf_vc_v_ivv_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2, int
simm5, size_t vl);
vuint32m1_t __riscv_sf_vc_v_ivv_se_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2,
int simm5, size_t vl);
vuint32m2_t __riscv_sf_vc_v_ivv_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2, int
simm5, size_t vl);
vuint32m2_t __riscv_sf_vc_v_ivv_se_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2,
int simm5, size_t vl);
vuint32m4_t __riscv_sf_vc_v_ivv_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2, int
simm5, size_t vl);
vuint32m4_t __riscv_sf_vc_v_ivv_se_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2,
int simm5, size_t vl);
vuint32m8_t __riscv_sf_vc_v_ivv_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2, int
simm5, size_t vl);
vuint32m8_t __riscv_sf_vc_v_ivv_se_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2,
int simm5, size_t vl);
vuint64m1_t __riscv_sf_vc_v_ivv_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2, int
simm5, size_t vl);
vuint64m1_t __riscv_sf_vc_v_ivv_se_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2,
int simm5, size_t vl);
vuint64m2_t __riscv_sf_vc_v_ivv_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2, int
simm5, size_t vl);
vuint64m2_t __riscv_sf_vc_v_ivv_se_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2,
int simm5, size_t vl);
vuint64m4_t __riscv_sf_vc_v_ivv_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2, int
simm5, size_t vl);
vuint64m4_t __riscv_sf_vc_v_ivv_se_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2,
int simm5, size_t vl);
vuint64m8_t __riscv_sf_vc_v_ivv_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2, int
simm5, size_t vl);
vuint64m8_t __riscv_sf_vc_v_ivv_se_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2,
int simm5, size_t vl);
void __riscv_sf_vc_fvv_se_u16mf4 (int bit_field26, vuint16mf4_t vd, vuint16mf4_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u16mf2 (int bit_field26, vuint16mf2_t vd, vuint16mf2_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u16m1 (int bit_field26, vuint16m1_t vd, vuint16m1_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u16m2 (int bit_field26, vuint16m2_t vd, vuint16m2_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u16m4 (int bit_field26, vuint16m4_t vd, vuint16m4_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u16m8 (int bit_field26, vuint16m8_t vd, vuint16m8_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u32mf2 (int bit_field26, vuint32mf2_t vd, vuint32mf2_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u32m1 (int bit_field26, vuint32m1_t vd, vuint32m1_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u32m2 (int bit_field26, vuint32m2_t vd, vuint32m2_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u32m4 (int bit_field26, vuint32m4_t vd, vuint32m4_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u32m8 (int bit_field26, vuint32m8_t vd, vuint32m8_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u64m1 (int bit_field26, vuint64m1_t vd, vuint64m1_t vs2, float64_t
fs1, size_t vl);
```

```
void __riscv_sf_vc_fvv_se_u64m2 (int bit_field26, vuint64m2_t vd, vuint64m2_t vs2, float64_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u64m4 (int bit_field26, vuint64m4_t vd, vuint64m4_t vs2, float64_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u64m8 (int bit_field26, vuint64m8_t vd, vuint64m8_t vs2, float64_t
fs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_fvv_u16mf4 (int bit_field26, vuint16mf4_t vd, vuint16mf4_t vs2,
float16_t fs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_fvv_se_u16mf4 (int bit_field26, vuint16mf4_t vd, vuint16mf4_t vs2,
float16_t fs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_fvv_u16mf2 (int bit_field26, vuint16mf2_t vd, vuint16mf2_t vs2,
float16_t fs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_fvv_se_u16mf2 (int bit_field26, vuint16mf2_t vd, vuint16mf2_t vs2,
float16_t fs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_fvv_u16m1 (int bit_field26, vuint16m1_t vd, vuint16m1_t vs2,
float16_t fs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_fvv_se_u16m1 (int bit_field26, vuint16m1_t vd, vuint16m1_t vs2,
float16_t fs1, size_t vl);
vuint16m2_t __riscv_sf_vc_v_fvv_u16m2 (int bit_field26, vuint16m2_t vd, vuint16m2_t vs2,
float16_t fs1, size_t vl);
vuint16m2_t __riscv_sf_vc_v_fvv_se_u16m2 (int bit_field26, vuint16m2_t vd, vuint16m2_t vs2,
float16_t fs1, size_t vl);
vuint16m4_t __riscv_sf_vc_v_fvv_u16m4 (int bit_field26, vuint16m4_t vd, vuint16m4_t vs2,
float16_t fs1, size_t vl);
vuint16m4_t __riscv_sf_vc_v_fvv_se_u16m4 (int bit_field26, vuint16m4_t vd, vuint16m4_t vs2,
float16_t fs1, size_t vl);
vuint16m8_t __riscv_sf_vc_v_fvv_u16m8 (int bit_field26, vuint16m8_t vd, vuint16m8_t vs2,
float16_t fs1, size_t vl);
vuint16m8_t __riscv_sf_vc_v_fvv_se_u16m8 (int bit_field26, vuint16m8_t vd, vuint16m8_t vs2,
float16_t fs1, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_fvv_u32mf2 (int bit_field26, vuint32mf2_t vd, vuint32mf2_t vs2,
float32_t fs1, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_fvv_se_u32mf2 (int bit_field26, vuint32mf2_t vd, vuint32mf2_t vs2,
float32_t fs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_fvv_u32m1 (int bit_field26, vuint32m1_t vd, vuint32m1_t vs2,
float32_t fs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_fvv_se_u32m1 (int bit_field26, vuint32m1_t vd, vuint32m1_t vs2,
float32_t fs1, size_t vl);
vuint32m2_t __riscv_sf_vc_v_fvv_u32m2 (int bit_field26, vuint32m2_t vd, vuint32m2_t vs2,
float32_t fs1, size_t vl);
vuint32m2_t __riscv_sf_vc_v_fvv_se_u32m2 (int bit_field26, vuint32m2_t vd, vuint32m2_t vs2,
float32_t fs1, size_t vl);
vuint32m4_t __riscv_sf_vc_v_fvv_u32m4 (int bit_field26, vuint32m4_t vd, vuint32m4_t vs2,
float32_t fs1, size_t vl);
vuint32m4_t __riscv_sf_vc_v_fvv_se_u32m4 (int bit_field26, vuint32m4_t vd, vuint32m4_t vs2,
float32_t fs1, size_t vl);
vuint32m8_t __riscv_sf_vc_v_fvv_u32m8 (int bit_field26, vuint32m8_t vd, vuint32m8_t vs2,
float32_t fs1, size_t vl);
vuint32m8_t __riscv_sf_vc_v_fvv_se_u32m8 (int bit_field26, vuint32m8_t vd, vuint32m8_t vs2,
float32_t fs1, size_t vl);
vuint64m1_t __riscv_sf_vc_v_fvv_u64m1 (int bit_field26, vuint64m1_t vd, vuint64m1_t vs2,
float64_t fs1, size_t vl);
vuint64m1_t __riscv_sf_vc_v_fvv_se_u64m1 (int bit_field26, vuint64m1_t vd, vuint64m1_t vs2,
float64_t fs1, size_t vl);
vuint64m2_t __riscv_sf_vc_v_fvv_u64m2 (int bit_field26, vuint64m2_t vd, vuint64m2_t vs2,
float64_t fs1, size_t vl);
```

```
vuint64m2_t __riscv_sf_vc_v_fvv_se_u64m2 (int bit_field26, vuint64m2_t vd, vuint64m2_t vs2,
float64_t fs1, size_t vl);
vuint64m4_t __riscv_sf_vc_v_fvv_u64m4 (int bit_field26, vuint64m4_t vd, vuint64m4_t vs2,
float64_t fs1, size_t vl);
vuint64m4_t __riscv_sf_vc_v_fvv_se_u64m4 (int bit_field26, vuint64m4_t vd, vuint64m4_t vs2,
float64_t fs1, size_t vl);
vuint64m8_t __riscv_sf_vc_v_fvv_u64m8 (int bit_field26, vuint64m8_t vd, vuint64m8_t vs2,
float64_t fs1, size_t vl);
vuint64m8_t __riscv_sf_vc_v_fvv_se_u64m8 (int bit_field26, vuint64m8_t vd, vuint64m8_t vs2,
float64_t fs1, size_t vl);
void __riscv_sf_vc_x_se_u8mf8 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u8mf4 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u8mf2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u8m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u8m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u8m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u8m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint8_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u16mf4 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u16mf2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u16m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u16m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u16m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u16m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u32mf2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u32m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u32m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u32m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u32m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u64m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint64_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u64m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint64_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u64m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint64_t xs1, size_t vl);
void __riscv_sf_vc_x_se_u64m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7,
uint64_t xs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_x_u8mf8 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
```

```
vuint8mf8_t __riscv_sf_vc_v_x_se_u8mf8 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8mf4_t __riscv_sf_vc_v_x_u8mf4 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8mf4_t __riscv_sf_vc_v_x_se_u8mf4 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8mf2_t __riscv_sf_vc_v_x_u8mf2 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8mf2_t __riscv_sf_vc_v_x_se_u8mf2 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8m1_t __riscv_sf_vc_v_x_u8m1 (int bit_field27_26, int bit_field24_20, uint8_t xs1, size_t
vl);
vuint8m1_t __riscv_sf_vc_v_x_se_u8m1 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8m2_t __riscv_sf_vc_v_x_u8m2 (int bit_field27_26, int bit_field24_20, uint8_t xs1, size_t
vl);
vuint8m2_t __riscv_sf_vc_v_x_se_u8m2 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8m4_t __riscv_sf_vc_v_x_u8m4 (int bit_field27_26, int bit_field24_20, uint8_t xs1, size_t
vl);
vuint8m4_t __riscv_sf_vc_v_x_se_u8m4 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint8m8_t __riscv_sf_vc_v_x_u8m8 (int bit_field27_26, int bit_field24_20, uint8_t xs1, size_t
vl);
vuint8m8_t __riscv_sf_vc_v_x_se_u8m8 (int bit_field27_26, int bit_field24_20, uint8_t xs1,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_x_u16mf4 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_x_se_u16mf4 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_x_u16mf2 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_x_se_u16mf2 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_x_u16m1 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_x_se_u16m1 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_x_u16m2 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_x_se_u16m2 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_x_u16m4 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_x_se_u16m4 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_x_u16m8 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_x_se_u16m8 (int bit_field27_26, int bit_field24_20, uint16_t xs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_x_u32mf2 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_x_se_u32mf2 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_x_u32m1 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
```

```
vuint32m1_t __riscv_sf_vc_v_x_se_u32m1 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_x_u32m2 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_x_se_u32m2 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_x_u32m4 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_x_se_u32m4 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_x_u32m8 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_x_se_u32m8 (int bit_field27_26, int bit_field24_20, uint32_t xs1,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_x_u64m1 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_x_se_u64m1 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_x_u64m2 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_x_se_u64m2 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_x_u64m4 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_x_se_u64m4 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_x_u64m8 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_x_se_u64m8 (int bit_field27_26, int bit_field24_20, uint64_t xs1,
size_t vl);
void __riscv_sf_vc_i_se_u8mf8 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u8mf4 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u8mf2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u8m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u8m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u8m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u8m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u16mf4 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u16mf2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u16m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u16m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u16m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u16m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
```

```
void __riscv_sf_vc_i_se_u32mf2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u32m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u32m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u32m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u32m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u64m1 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u64m2 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u64m4 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
void __riscv_sf_vc_i_se_u64m8 (int bit_field27_26, int bit_field24_20, int bit_field11_7, int
simm5, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_i_u8mf8 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8mf8_t __riscv_sf_vc_v_i_se_u8mf8 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint8mf4_t __riscv_sf_vc_v_i_u8mf4 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8mf4_t __riscv_sf_vc_v_i_se_u8mf4 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint8mf2_t __riscv_sf_vc_v_i_u8mf2 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8mf2_t __riscv_sf_vc_v_i_se_u8mf2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint8m1_t __riscv_sf_vc_v_i_u8m1 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m1_t __riscv_sf_vc_v_i_se_u8m1 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m2_t __riscv_sf_vc_v_i_u8m2 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m2_t __riscv_sf_vc_v_i_se_u8m2 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m4_t __riscv_sf_vc_v_i_u8m4 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m4_t __riscv_sf_vc_v_i_se_u8m4 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m8_t __riscv_sf_vc_v_i_u8m8 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint8m8_t __riscv_sf_vc_v_i_se_u8m8 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint16mf4_t __riscv_sf_vc_v_i_u16mf4 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_i_se_u16mf4 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_i_u16mf2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_i_se_u16mf2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_i_u16m1 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
```

```
vuint16m1_t __riscv_sf_vc_v_i_se_u16m1 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_i_u16m2 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint16m2_t __riscv_sf_vc_v_i_se_u16m2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_i_u16m4 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint16m4_t __riscv_sf_vc_v_i_se_u16m4 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_i_u16m8 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint16m8_t __riscv_sf_vc_v_i_se_u16m8 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_i_u32mf2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_i_se_u32mf2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_i_u32m1 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint32m1_t __riscv_sf_vc_v_i_se_u32m1 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_i_u32m2 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint32m2_t __riscv_sf_vc_v_i_se_u32m2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_i_u32m4 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint32m4_t __riscv_sf_vc_v_i_se_u32m4 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_i_u32m8 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint32m8_t __riscv_sf_vc_v_i_se_u32m8 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_i_u64m1 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint64m1_t __riscv_sf_vc_v_i_se_u64m1 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_i_u64m2 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint64m2_t __riscv_sf_vc_v_i_se_u64m2 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_i_u64m4 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint64m4_t __riscv_sf_vc_v_i_se_u64m4 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_i_u64m8 (int bit_field27_26, int bit_field24_20, int simm5, size_t
vl);
vuint64m8_t __riscv_sf_vc_v_i_se_u64m8 (int bit_field27_26, int bit_field24_20, int simm5,
size_t vl);
void __riscv_sf_vc_vv_se_u8mf8 (int bit_field27_26, int bit_field11_7, vuint8mf8_t vs2,
vuint8mf8_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u8mf4 (int bit_field27_26, int bit_field11_7, vuint8mf4_t vs2,
vuint8mf4_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u8mf2 (int bit_field27_26, int bit_field11_7, vuint8mf2_t vs2,
vuint8mf2_t rs1, size_t vl);
```

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void __riscv_sf_vc_vv_se_u8m1 (int bit_field27_26, int bit_field11_7, vuint8m1_t vs2,
vuint8m1_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u8m2 (int bit_field27_26, int bit_field11_7, vuint8m2_t vs2,
vuint8m2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u8m4 (int bit_field27_26, int bit_field11_7, vuint8m4_t vs2,
vuint8m4_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u8m8 (int bit_field27_26, int bit_field11_7, vuint8m8_t vs2,
vuint8m8_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u16mf4 (int bit_field27_26, int bit_field11_7, vuint16mf4_t vs2,
vuint16mf4_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u16mf2 (int bit_field27_26, int bit_field11_7, vuint16mf2_t vs2,
vuint16mf2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u16m1 (int bit_field27_26, int bit_field11_7, vuint16m1_t vs2,
vuint16m1_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u16m2 (int bit_field27_26, int bit_field11_7, vuint16m2_t vs2,
vuint16m2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u16m4 (int bit_field27_26, int bit_field11_7, vuint16m4_t vs2,
vuint16m4_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u16m8 (int bit_field27_26, int bit_field11_7, vuint16m8_t vs2,
vuint16m8_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u32mf2 (int bit_field27_26, int bit_field11_7, vuint32mf2_t vs2,
vuint32mf2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u32m1 (int bit_field27_26, int bit_field11_7, vuint32m1_t vs2,
vuint32m1_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u32m2 (int bit_field27_26, int bit_field11_7, vuint32m2_t vs2,
vuint32m2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u32m4 (int bit_field27_26, int bit_field11_7, vuint32m4_t vs2,
vuint32m4_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u32m8 (int bit_field27_26, int bit_field11_7, vuint32m8_t vs2,
vuint32m8_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u64m1 (int bit_field27_26, int bit_field11_7, vuint64m1_t vs2,
vuint64m1_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u64m2 (int bit_field27_26, int bit_field11_7, vuint64m2_t vs2,
vuint64m2_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u64m4 (int bit_field27_26, int bit_field11_7, vuint64m4_t vs2,
vuint64m4_t rs1, size_t vl);
void __riscv_sf_vc_vv_se_u64m8 (int bit_field27_26, int bit_field11_7, vuint64m8_t vs2,
vuint64m8_t rs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_vv_u8mf8 (int bit_field27_26, vuint8mf8_t vs2, vuint8mf8_t rs1,
size_t vl);
vuint8mf8_t __riscv_sf_vc_v_vv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vs2, vuint8mf8_t rs1,
size_t vl);
vuint8mf4_t __riscv_sf_vc_v_vv_u8mf4 (int bit_field27_26, vuint8mf4_t vs2, vuint8mf4_t rs1,
size_t vl);
vuint8mf4_t __riscv_sf_vc_v_vv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vs2, vuint8mf4_t rs1,
size_t vl);
vuint8mf2_t __riscv_sf_vc_v_vv_u8mf2 (int bit_field27_26, vuint8mf2_t vs2, vuint8mf2_t rs1,
size_t vl);
vuint8mf2_t __riscv_sf_vc_v_vv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vs2, vuint8mf2_t rs1,
size_t vl);
vuint8m1_t __riscv_sf_vc_v_vv_u8m1 (int bit_field27_26, vuint8m1_t vs2, vuint8m1_t rs1, size_t
vl);
vuint8m1_t __riscv_sf_vc_v_vv_se_u8m1 (int bit_field27_26, vuint8m1_t vs2, vuint8m1_t rs1,
size_t vl);
vuint8m2_t __riscv_sf_vc_v_vv_u8m2 (int bit_field27_26, vuint8m2_t vs2, vuint8m2_t rs1, size_t
vl);
```

```
vuint8m2_t __riscv_sf_vc_v_vv_se_u8m2 (int bit_field27_26, vuint8m2_t vs2, vuint8m2_t rs1,
size_t vl);
vuint8m4_t __riscv_sf_vc_v_vv_u8m4 (int bit_field27_26, vuint8m4_t vs2, vuint8m4_t rs1, size_t
vl);
vuint8m4_t __riscv_sf_vc_v_vv_se_u8m4 (int bit_field27_26, vuint8m4_t vs2, vuint8m4_t rs1,
size_t vl);
vuint8m8_t __riscv_sf_vc_v_vv_u8m8 (int bit_field27_26, vuint8m8_t vs2, vuint8m8_t rs1, size_t
vl);
vuint8m8_t __riscv_sf_vc_v_vv_se_u8m8 (int bit_field27_26, vuint8m8_t vs2, vuint8m8_t rs1,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_vv_u16mf4 (int bit_field27_26, vuint16mf4_t vs2, vuint16mf4_t rs1,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_vv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vs2, vuint16mf4_t
rs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_vv_u16mf2 (int bit_field27_26, vuint16mf2_t vs2, vuint16mf2_t rs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_vv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vs2, vuint16mf2_t
rs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_vv_u16m1 (int bit_field27_26, vuint16m1_t vs2, vuint16m1_t rs1,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_vv_se_u16m1 (int bit_field27_26, vuint16m1_t vs2, vuint16m1_t rs1,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_vv_u16m2 (int bit_field27_26, vuint16m2_t vs2, vuint16m2_t rs1,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_vv_se_u16m2 (int bit_field27_26, vuint16m2_t vs2, vuint16m2_t rs1,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_vv_u16m4 (int bit_field27_26, vuint16m4_t vs2, vuint16m4_t rs1,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_vv_se_u16m4 (int bit_field27_26, vuint16m4_t vs2, vuint16m4_t rs1,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_vv_u16m8 (int bit_field27_26, vuint16m8_t vs2, vuint16m8_t rs1,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_vv_se_u16m8 (int bit_field27_26, vuint16m8_t vs2, vuint16m8_t rs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_vv_u32mf2 (int bit_field27_26, vuint32mf2_t vs2, vuint32mf2_t rs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_vv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vs2, vuint32mf2_t
rs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_vv_u32m1 (int bit_field27_26, vuint32m1_t vs2, vuint32m1_t rs1,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_vv_se_u32m1 (int bit_field27_26, vuint32m1_t vs2, vuint32m1_t rs1,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_vv_u32m2 (int bit_field27_26, vuint32m2_t vs2, vuint32m2_t rs1,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_vv_se_u32m2 (int bit_field27_26, vuint32m2_t vs2, vuint32m2_t rs1,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_vv_u32m4 (int bit_field27_26, vuint32m4_t vs2, vuint32m4_t rs1,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_vv_se_u32m4 (int bit_field27_26, vuint32m4_t vs2, vuint32m4_t rs1,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_vv_u32m8 (int bit_field27_26, vuint32m8_t vs2, vuint32m8_t rs1,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_vv_se_u32m8 (int bit_field27_26, vuint32m8_t vs2, vuint32m8_t rs1,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_vv_u64m1 (int bit_field27_26, vuint64m1_t vs2, vuint64m1_t rs1,
size_t vl);
```

```
vuint64m1_t __riscv_sf_vc_v_vv_se_u64m1 (int bit_field27_26, vuint64m1_t vs2, vuint64m1_t rs1,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_vv_u64m2 (int bit_field27_26, vuint64m2_t vs2, vuint64m2_t rs1,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_vv_se_u64m2 (int bit_field27_26, vuint64m2_t vs2, vuint64m2_t rs1,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_vv_u64m4 (int bit_field27_26, vuint64m4_t vs2, vuint64m4_t rs1,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_vv_se_u64m4 (int bit_field27_26, vuint64m4_t vs2, vuint64m4_t rs1,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_vv_u64m8 (int bit_field27_26, vuint64m8_t vs2, vuint64m8_t rs1,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_vv_se_u64m8 (int bit_field27_26, vuint64m8_t vs2, vuint64m8_t rs1,
size_t vl);
void __riscv_sf_vc_xv_se_u8mf8 (int bit_field27_26, int bit_field11_7, vuint8mf8_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u8mf4 (int bit_field27_26, int bit_field11_7, vuint8mf4_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u8mf2 (int bit_field27_26, int bit_field11_7, vuint8mf2_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u8m1 (int bit_field27_26, int bit_field11_7, vuint8m1_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u8m2 (int bit_field27_26, int bit_field11_7, vuint8m2_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u8m4 (int bit_field27_26, int bit_field11_7, vuint8m4_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u8m8 (int bit_field27_26, int bit_field11_7, vuint8m8_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xv_se_u16mf4 (int bit_field27_26, int bit_field11_7, vuint16mf4_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u16mf2 (int bit_field27_26, int bit_field11_7, vuint16mf2_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u16m1 (int bit_field27_26, int bit_field11_7, vuint16m1_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u16m2 (int bit_field27_26, int bit_field11_7, vuint16m2_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u16m4 (int bit_field27_26, int bit_field11_7, vuint16m4_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u16m8 (int bit_field27_26, int bit_field11_7, vuint16m8_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u32mf2 (int bit_field27_26, int bit_field11_7, vuint32mf2_t vs2,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u32m1 (int bit_field27_26, int bit_field11_7, vuint32m1_t vs2,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u32m2 (int bit_field27_26, int bit_field11_7, vuint32m2_t vs2,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u32m4 (int bit_field27_26, int bit_field11_7, vuint32m4_t vs2,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u32m8 (int bit_field27_26, int bit_field11_7, vuint32m8_t vs2,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u64m1 (int bit_field27_26, int bit_field11_7, vuint64m1_t vs2,
uint64_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u64m2 (int bit_field27_26, int bit_field11_7, vuint64m2_t vs2,
uint64_t xs1, size_t vl);
void __riscv_sf_vc_xv_se_u64m4 (int bit_field27_26, int bit_field11_7, vuint64m4_t vs2,
uint64_t xs1, size_t vl);
```

```
void __riscv_sf_vc_xv_se_u64m8 (int bit_field27_26, int bit_field11_7, vuint64m8_t vs2,
uint64_t xs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_xv_u8mf8 (int bit_field27_26, vuint8mf8_t vs2, uint8_t xs1, size_t
vl);
vuint8mf8_t __riscv_sf_vc_v_xv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vs2, uint8_t xs1,
size_t vl);
vuint8mf4_t __riscv_sf_vc_v_xv_u8mf4 (int bit_field27_26, vuint8mf4_t vs2, uint8_t xs1, size_t
vl);
vuint8mf4_t __riscv_sf_vc_v_xv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vs2, uint8_t xs1,
size_t vl);
vuint8mf2_t __riscv_sf_vc_v_xv_u8mf2 (int bit_field27_26, vuint8mf2_t vs2, uint8_t xs1, size_t
vl);
vuint8mf2_t __riscv_sf_vc_v_xv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vs2, uint8_t xs1,
size_t vl);
vuint8m1_t __riscv_sf_vc_v_xv_u8m1 (int bit_field27_26, vuint8m1_t vs2, uint8_t xs1, size_t vl);
vuint8m1_t __riscv_sf_vc_v_xv_se_u8m1 (int bit_field27_26, vuint8m1_t vs2, uint8_t xs1, size_t
vl);
vuint8m2_t __riscv_sf_vc_v_xv_u8m2 (int bit_field27_26, vuint8m2_t vs2, uint8_t xs1, size_t vl);
vuint8m2_t __riscv_sf_vc_v_xv_se_u8m2 (int bit_field27_26, vuint8m2_t vs2, uint8_t xs1, size_t
vl);
vuint8m4_t __riscv_sf_vc_v_xv_u8m4 (int bit_field27_26, vuint8m4_t vs2, uint8_t xs1, size_t vl);
vuint8m4_t __riscv_sf_vc_v_xv_se_u8m4 (int bit_field27_26, vuint8m4_t vs2, uint8_t xs1, size_t
vl);
vuint8m8_t __riscv_sf_vc_v_xv_u8m8 (int bit_field27_26, vuint8m8_t vs2, uint8_t xs1, size_t vl);
vuint8m8_t __riscv_sf_vc_v_xv_se_u8m8 (int bit_field27_26, vuint8m8_t vs2, uint8_t xs1, size_t
vl);
vuint16mf4_t __riscv_sf_vc_v_xv_u16mf4 (int bit_field27_26, vuint16mf4_t vs2, uint16_t xs1,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_xv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vs2, uint16_t xs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_xv_u16mf2 (int bit_field27_26, vuint16mf2_t vs2, uint16_t xs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_xv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vs2, uint16_t xs1,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_xv_u16m1 (int bit_field27_26, vuint16m1_t vs2, uint16_t xs1, size_t
vl);
vuint16m1_t __riscv_sf_vc_v_xv_se_u16m1 (int bit_field27_26, vuint16m1_t vs2, uint16_t xs1,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_xv_u16m2 (int bit_field27_26, vuint16m2_t vs2, uint16_t xs1, size_t
vl);
vuint16m2_t __riscv_sf_vc_v_xv_se_u16m2 (int bit_field27_26, vuint16m2_t vs2, uint16_t xs1,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_xv_u16m4 (int bit_field27_26, vuint16m4_t vs2, uint16_t xs1, size_t
vl);
vuint16m4_t __riscv_sf_vc_v_xv_se_u16m4 (int bit_field27_26, vuint16m4_t vs2, uint16_t xs1,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_xv_u16m8 (int bit_field27_26, vuint16m8_t vs2, uint16_t xs1, size_t
vl);
vuint16m8_t __riscv_sf_vc_v_xv_se_u16m8 (int bit_field27_26, vuint16m8_t vs2, uint16_t xs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_xv_u32mf2 (int bit_field27_26, vuint32mf2_t vs2, uint32_t xs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_xv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vs2, uint32_t xs1,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_xv_u32m1 (int bit_field27_26, vuint32m1_t vs2, uint32_t xs1, size_t
vl);
```

```
vuint32m1_t __riscv_sf_vc_v_xv_se_u32m1 (int bit_field27_26, vuint32m1_t vs2, uint32_t xs1,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_xv_u32m2 (int bit_field27_26, vuint32m2_t vs2, uint32_t xs1, size_t
vl);
vuint32m2_t __riscv_sf_vc_v_xv_se_u32m2 (int bit_field27_26, vuint32m2_t vs2, uint32_t xs1,
size_t vl);
vuint32m4_t __riscv_sf_vc_v_xv_u32m4 (int bit_field27_26, vuint32m4_t vs2, uint32_t xs1, size_t
vl);
vuint32m4_t __riscv_sf_vc_v_xv_se_u32m4 (int bit_field27_26, vuint32m4_t vs2, uint32_t xs1,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_xv_u32m8 (int bit_field27_26, vuint32m8_t vs2, uint32_t xs1, size_t
vl);
vuint32m8_t __riscv_sf_vc_v_xv_se_u32m8 (int bit_field27_26, vuint32m8_t vs2, uint32_t xs1,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_xv_u64m1 (int bit_field27_26, vuint64m1_t vs2, uint64_t xs1, size_t
vl);
vuint64m1_t __riscv_sf_vc_v_xv_se_u64m1 (int bit_field27_26, vuint64m1_t vs2, uint64_t xs1,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_xv_u64m2 (int bit_field27_26, vuint64m2_t vs2, uint64_t xs1, size_t
vl);
vuint64m2_t __riscv_sf_vc_v_xv_se_u64m2 (int bit_field27_26, vuint64m2_t vs2, uint64_t xs1,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_xv_u64m4 (int bit_field27_26, vuint64m4_t vs2, uint64_t xs1, size_t
vl);
vuint64m4_t __riscv_sf_vc_v_xv_se_u64m4 (int bit_field27_26, vuint64m4_t vs2, uint64_t xs1,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_xv_u64m8 (int bit_field27_26, vuint64m8_t vs2, uint64_t xs1, size_t
vl);
vuint64m8_t __riscv_sf_vc_v_xv_se_u64m8 (int bit_field27_26, vuint64m8_t vs2, uint64_t xs1,
size_t vl);
void __riscv_sf_vc_iv_se_u8mf8 (int bit_field27_26, int bit_field11_7, vuint8mf8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u8mf4 (int bit_field27_26, int bit_field11_7, vuint8mf4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u8mf2 (int bit_field27_26, int bit_field11_7, vuint8mf2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u8m1 (int bit_field27_26, int bit_field11_7, vuint8m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u8m2 (int bit_field27_26, int bit_field11_7, vuint8m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u8m4 (int bit_field27_26, int bit_field11_7, vuint8m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u8m8 (int bit_field27_26, int bit_field11_7, vuint8m8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u16mf4 (int bit_field27_26, int bit_field11_7, vuint16mf4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u16mf2 (int bit_field27_26, int bit_field11_7, vuint16mf2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u16m1 (int bit_field27_26, int bit_field11_7, vuint16m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u16m2 (int bit_field27_26, int bit_field11_7, vuint16m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u16m4 (int bit_field27_26, int bit_field11_7, vuint16m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u16m8 (int bit_field27_26, int bit_field11_7, vuint16m8_t vs2, int
simm5, size_t vl);
```

```
void __riscv_sf_vc_iv_se_u32mf2 (int bit_field27_26, int bit_field11_7, vuint32mf2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u32m1 (int bit_field27_26, int bit_field11_7, vuint32m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u32m2 (int bit_field27_26, int bit_field11_7, vuint32m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u32m4 (int bit_field27_26, int bit_field11_7, vuint32m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u32m8 (int bit_field27_26, int bit_field11_7, vuint32m8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u64m1 (int bit_field27_26, int bit_field11_7, vuint64m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u64m2 (int bit_field27_26, int bit_field11_7, vuint64m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u64m4 (int bit_field27_26, int bit_field11_7, vuint64m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_iv_se_u64m8 (int bit_field27_26, int bit_field11_7, vuint64m8_t vs2, int
simm5, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_iv_u8mf8 (int bit_field27_26, vuint8mf8_t vs2, int simm5, size_t
vl);
vuint8mf8_t __riscv_sf_vc_v_iv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vs2, int simm5, size_t
vl);
vuint8mf4_t __riscv_sf_vc_v_iv_u8mf4 (int bit_field27_26, vuint8mf4_t vs2, int simm5, size_t
vl);
vuint8mf4_t __riscv_sf_vc_v_iv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vs2, int simm5, size_t
vl);
vuint8mf2_t __riscv_sf_vc_v_iv_u8mf2 (int bit_field27_26, vuint8mf2_t vs2, int simm5, size_t
vl);
vuint8mf2_t __riscv_sf_vc_v_iv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vs2, int simm5, size_t
vl);
vuint8m1_t __riscv_sf_vc_v_iv_u8m1 (int bit_field27_26, vuint8m1_t vs2, int simm5, size_t vl);
vuint8m1_t __riscv_sf_vc_v_iv_se_u8m1 (int bit_field27_26, vuint8m1_t vs2, int simm5, size_t
vl);
vuint8m2_t __riscv_sf_vc_v_iv_u8m2 (int bit_field27_26, vuint8m2_t vs2, int simm5, size_t vl);
vuint8m2_t __riscv_sf_vc_v_iv_se_u8m2 (int bit_field27_26, vuint8m2_t vs2, int simm5, size_t
vl);
vuint8m4_t __riscv_sf_vc_v_iv_u8m4 (int bit_field27_26, vuint8m4_t vs2, int simm5, size_t vl);
vuint8m4_t __riscv_sf_vc_v_iv_se_u8m4 (int bit_field27_26, vuint8m4_t vs2, int simm5, size_t
vl);
vuint8m8_t __riscv_sf_vc_v_iv_u8m8 (int bit_field27_26, vuint8m8_t vs2, int simm5, size_t vl);
vuint8m8_t __riscv_sf_vc_v_iv_se_u8m8 (int bit_field27_26, vuint8m8_t vs2, int simm5, size_t
vl);
vuint16mf4_t __riscv_sf_vc_v_iv_u16mf4 (int bit_field27_26, vuint16mf4_t vs2, int simm5, size_t
vl);
vuint16mf4_t __riscv_sf_vc_v_iv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vs2, int simm5,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_iv_u16mf2 (int bit_field27_26, vuint16mf2_t vs2, int simm5, size_t
vl);
vuint16mf2_t __riscv_sf_vc_v_iv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vs2, int simm5,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_iv_u16m1 (int bit_field27_26, vuint16m1_t vs2, int simm5, size_t
vl);
vuint16m1_t __riscv_sf_vc_v_iv_se_u16m1 (int bit_field27_26, vuint16m1_t vs2, int simm5, size_t
vl);
vuint16m2_t __riscv_sf_vc_v_iv_u16m2 (int bit_field27_26, vuint16m2_t vs2, int simm5, size_t
vl);
```

```
vuint16m2_t __riscv_sf_vc_v_iv_se_u16m2 (int bit_field27_26, vuint16m2_t vs2, int simm5, size_t
vl);
vuint16m4_t __riscv_sf_vc_v_iv_u16m4 (int bit_field27_26, vuint16m4_t vs2, int simm5, size_t
vl);
vuint16m4_t __riscv_sf_vc_v_iv_se_u16m4 (int bit_field27_26, vuint16m4_t vs2, int simm5, size_t
vl);
vuint16m8_t __riscv_sf_vc_v_iv_u16m8 (int bit_field27_26, vuint16m8_t vs2, int simm5, size_t
vl);
vuint16m8_t __riscv_sf_vc_v_iv_se_u16m8 (int bit_field27_26, vuint16m8_t vs2, int simm5, size_t
vl);
vuint32mf2_t __riscv_sf_vc_v_iv_u32mf2 (int bit_field27_26, vuint32mf2_t vs2, int simm5, size_t
vl);
vuint32mf2_t __riscv_sf_vc_v_iv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vs2, int simm5,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_iv_u32m1 (int bit_field27_26, vuint32m1_t vs2, int simm5, size_t
vl);
vuint32m1_t __riscv_sf_vc_v_iv_se_u32m1 (int bit_field27_26, vuint32m1_t vs2, int simm5, size_t
vl);
vuint32m2_t __riscv_sf_vc_v_iv_u32m2 (int bit_field27_26, vuint32m2_t vs2, int simm5, size_t
vl);
vuint32m2_t __riscv_sf_vc_v_iv_se_u32m2 (int bit_field27_26, vuint32m2_t vs2, int simm5, size_t
vl);
vuint32m4_t __riscv_sf_vc_v_iv_u32m4 (int bit_field27_26, vuint32m4_t vs2, int simm5, size_t
vl);
vuint32m4_t __riscv_sf_vc_v_iv_se_u32m4 (int bit_field27_26, vuint32m4_t vs2, int simm5, size_t
vl);
vuint32m8_t __riscv_sf_vc_v_iv_u32m8 (int bit_field27_26, vuint32m8_t vs2, int simm5, size_t
vl);
vuint32m8_t __riscv_sf_vc_v_iv_se_u32m8 (int bit_field27_26, vuint32m8_t vs2, int simm5, size_t
vl);
vuint64m1_t __riscv_sf_vc_v_iv_u64m1 (int bit_field27_26, vuint64m1_t vs2, int simm5, size_t
vl);
vuint64m1_t __riscv_sf_vc_v_iv_se_u64m1 (int bit_field27_26, vuint64m1_t vs2, int simm5, size_t
vl);
vuint64m2_t __riscv_sf_vc_v_iv_u64m2 (int bit_field27_26, vuint64m2_t vs2, int simm5, size_t
vl);
vuint64m2_t __riscv_sf_vc_v_iv_se_u64m2 (int bit_field27_26, vuint64m2_t vs2, int simm5, size_t
vl);
vuint64m4_t __riscv_sf_vc_v_iv_u64m4 (int bit_field27_26, vuint64m4_t vs2, int simm5, size_t
vl);
vuint64m4_t __riscv_sf_vc_v_iv_se_u64m4 (int bit_field27_26, vuint64m4_t vs2, int simm5, size_t
vl);
vuint64m8_t __riscv_sf_vc_v_iv_u64m8 (int bit_field27_26, vuint64m8_t vs2, int simm5, size_t
vl);
vuint64m8_t __riscv_sf_vc_v_iv_se_u64m8 (int bit_field27_26, vuint64m8_t vs2, int simm5, size_t
vl);
void __riscv_sf_vc_fv_se_u16mf4 (int bit_field26, int bit_field11_7, vuint16mf4_t vs2,
float16_t fs1, size_t vl);
void __riscv_sf_vc_fv_se_u16mf2 (int bit_field26, int bit_field11_7, vuint16mf2_t vs2,
float16_t fs1, size_t vl);
void __riscv_sf_vc_fv_se_u16m1 (int bit_field26, int bit_field11_7, vuint16m1_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u16m2 (int bit_field26, int bit_field11_7, vuint16m2_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u16m4 (int bit_field26, int bit_field11_7, vuint16m4_t vs2, float16_t
fs1, size_t vl);
```

```
void __riscv_sf_vc_fv_se_u16m8 (int bit_field26, int bit_field11_7, vuint16m8_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u32mf2 (int bit_field26, int bit_field11_7, vuint32mf2_t vs2,
float32_t fs1, size_t vl);
void __riscv_sf_vc_fv_se_u32m1 (int bit_field26, int bit_field11_7, vuint32m1_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u32m2 (int bit_field26, int bit_field11_7, vuint32m2_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u32m4 (int bit_field26, int bit_field11_7, vuint32m4_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u32m8 (int bit_field26, int bit_field11_7, vuint32m8_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u64m1 (int bit_field26, int bit_field11_7, vuint64m1_t vs2, float64_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u64m2 (int bit_field26, int bit_field11_7, vuint64m2_t vs2, float64_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u64m4 (int bit_field26, int bit_field11_7, vuint64m4_t vs2, float64_t
fs1, size_t vl);
void __riscv_sf_vc_fv_se_u64m8 (int bit_field26, int bit_field11_7, vuint64m8_t vs2, float64_t
fs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_fv_u16mf4 (int bit_field26, vuint16mf4_t vs2, float16_t fs1,
size_t vl);
vuint16mf4_t __riscv_sf_vc_v_fv_se_u16mf4 (int bit_field26, vuint16mf4_t vs2, float16_t fs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_fv_u16mf2 (int bit_field26, vuint16mf2_t vs2, float16_t fs1,
size_t vl);
vuint16mf2_t __riscv_sf_vc_v_fv_se_u16mf2 (int bit_field26, vuint16mf2_t vs2, float16_t fs1,
size_t vl);
vuint16m1_t __riscv_sf_vc_v_fv_u16m1 (int bit_field26, vuint16m1_t vs2, float16_t fs1, size_t
vl);
vuint16m1_t __riscv_sf_vc_v_fv_se_u16m1 (int bit_field26, vuint16m1_t vs2, float16_t fs1,
size_t vl);
vuint16m2_t __riscv_sf_vc_v_fv_u16m2 (int bit_field26, vuint16m2_t vs2, float16_t fs1, size_t
vl);
vuint16m2_t __riscv_sf_vc_v_fv_se_u16m2 (int bit_field26, vuint16m2_t vs2, float16_t fs1,
size_t vl);
vuint16m4_t __riscv_sf_vc_v_fv_u16m4 (int bit_field26, vuint16m4_t vs2, float16_t fs1, size_t
vl);
vuint16m4_t __riscv_sf_vc_v_fv_se_u16m4 (int bit_field26, vuint16m4_t vs2, float16_t fs1,
size_t vl);
vuint16m8_t __riscv_sf_vc_v_fv_u16m8 (int bit_field26, vuint16m8_t vs2, float16_t fs1, size_t
vl);
vuint16m8_t __riscv_sf_vc_v_fv_se_u16m8 (int bit_field26, vuint16m8_t vs2, float16_t fs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_fv_u32mf2 (int bit_field26, vuint32mf2_t vs2, float32_t fs1,
size_t vl);
vuint32mf2_t __riscv_sf_vc_v_fv_se_u32mf2 (int bit_field26, vuint32mf2_t vs2, float32_t fs1,
size_t vl);
vuint32m1_t __riscv_sf_vc_v_fv_u32m1 (int bit_field26, vuint32m1_t vs2, float32_t fs1, size_t
vl);
vuint32m1_t __riscv_sf_vc_v_fv_se_u32m1 (int bit_field26, vuint32m1_t vs2, float32_t fs1,
size_t vl);
vuint32m2_t __riscv_sf_vc_v_fv_u32m2 (int bit_field26, vuint32m2_t vs2, float32_t fs1, size_t
vl);
vuint32m2_t __riscv_sf_vc_v_fv_se_u32m2 (int bit_field26, vuint32m2_t vs2, float32_t fs1,
size_t vl);
```

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vuint32m4_t __riscv_sf_vc_v_fv_u32m4 (int bit_field26, vuint32m4_t vs2, float32_t fs1, size_t
vl);
vuint32m4_t __riscv_sf_vc_v_fv_se_u32m4 (int bit_field26, vuint32m4_t vs2, float32_t fs1,
size_t vl);
vuint32m8_t __riscv_sf_vc_v_fv_u32m8 (int bit_field26, vuint32m8_t vs2, float32_t fs1, size_t
vl);
vuint32m8_t __riscv_sf_vc_v_fv_se_u32m8 (int bit_field26, vuint32m8_t vs2, float32_t fs1,
size_t vl);
vuint64m1_t __riscv_sf_vc_v_fv_u64m1 (int bit_field26, vuint64m1_t vs2, float64_t fs1, size_t
vl);
vuint64m1_t __riscv_sf_vc_v_fv_se_u64m1 (int bit_field26, vuint64m1_t vs2, float64_t fs1,
size_t vl);
vuint64m2_t __riscv_sf_vc_v_fv_u64m2 (int bit_field26, vuint64m2_t vs2, float64_t fs1, size_t
vl);
vuint64m2_t __riscv_sf_vc_v_fv_se_u64m2 (int bit_field26, vuint64m2_t vs2, float64_t fs1,
size_t vl);
vuint64m4_t __riscv_sf_vc_v_fv_u64m4 (int bit_field26, vuint64m4_t vs2, float64_t fs1, size_t
vl);
vuint64m4_t __riscv_sf_vc_v_fv_se_u64m4 (int bit_field26, vuint64m4_t vs2, float64_t fs1,
size_t vl);
vuint64m8_t __riscv_sf_vc_v_fv_u64m8 (int bit_field26, vuint64m8_t vs2, float64_t fs1, size_t
vl);
vuint64m8_t __riscv_sf_vc_v_fv_se_u64m8 (int bit_field26, vuint64m8_t vs2, float64_t fs1,
size_t vl);
void __riscv_sf_vc_vvv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2,
vuint8mf8_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2,
vuint8mf4_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2,
vuint8mf2_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2, vuint8m1_t
rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2, vuint8m2_t
rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2, vuint8m4_t
rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2, vuint8m8_t
rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t vs2,
vuint16mf4_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t vs2,
vuint16mf2_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2,
vuint16m1_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2,
vuint16m2_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2,
vuint16m4_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2,
vuint16m8_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t vs2,
vuint32mf2_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2,
vuint32m1_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2,
vuint32m2_t rs1, size_t vl);
```

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void __riscv_sf_vc_vvv_se_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2,
vuint32m4_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2,
vuint32m8_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2,
vuint64m1_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2,
vuint64m2_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2,
vuint64m4_t rs1, size_t vl);
void __riscv_sf_vc_vvv_se_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2,
vuint64m8_t rs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_vvv_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2,
vuint8mf8_t rs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_vvv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2,
vuint8mf8_t rs1, size_t vl);
vuint8mf4_t __riscv_sf_vc_v_vvv_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2,
vuint8mf4_t rs1, size_t vl);
vuint8mf4_t __riscv_sf_vc_v_vvv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2,
vuint8mf4_t rs1, size_t vl);
vuint8mf2_t __riscv_sf_vc_v_vvv_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2,
vuint8mf2_t rs1, size_t vl);
vuint8mf2_t __riscv_sf_vc_v_vvv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2,
vuint8mf2_t rs1, size_t vl);
vuint8m1_t __riscv_sf_vc_v_vvv_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2,
vuint8m1_t rs1, size_t vl);
vuint8m1_t __riscv_sf_vc_v_vvv_se_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2,
vuint8m1_t rs1, size_t vl);
vuint8m2_t __riscv_sf_vc_v_vvv_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2,
vuint8m2_t rs1, size_t vl);
vuint8m2_t __riscv_sf_vc_v_vvv_se_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2,
vuint8m2_t rs1, size_t vl);
vuint8m4_t __riscv_sf_vc_v_vvv_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2,
vuint8m4_t rs1, size_t vl);
vuint8m4_t __riscv_sf_vc_v_vvv_se_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2,
vuint8m4_t rs1, size_t vl);
vuint8m8_t __riscv_sf_vc_v_vvv_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2,
vuint8m8_t rs1, size_t vl);
vuint8m8_t __riscv_sf_vc_v_vvv_se_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2,
vuint8m8_t rs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_vvv_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t vs2,
vuint16mf4_t rs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_vvv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t
vs2, vuint16mf4_t rs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_vvv_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t vs2,
vuint16mf2_t rs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_vvv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t
vs2, vuint16mf2_t rs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_vvv_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2,
vuint16m1_t rs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_vvv_se_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2,
vuint16m1_t rs1, size_t vl);
vuint16m2_t __riscv_sf_vc_v_vvv_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2,
vuint16m2_t rs1, size_t vl);
vuint16m2_t __riscv_sf_vc_v_vvv_se_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2,
vuint16m2_t rs1, size_t vl);
```

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vuint16m4_t __riscv_sf_vc_v_vvv_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2,
vuint16m4_t rs1, size_t vl);
vuint16m4_t __riscv_sf_vc_v_vvv_se_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2,
vuint16m4_t rs1, size_t vl);
vuint16m8_t __riscv_sf_vc_v_vvv_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2,
vuint16m8_t rs1, size_t vl);
vuint16m8_t __riscv_sf_vc_v_vvv_se_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2,
vuint16m8_t rs1, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_vvv_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t vs2,
vuint32mf2_t rs1, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_vvv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t
vs2, vuint32mf2_t rs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_vvv_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2,
vuint32m1_t rs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_vvv_se_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2,
vuint32m1_t rs1, size_t vl);
vuint32m2_t __riscv_sf_vc_v_vvv_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2,
vuint32m2_t rs1, size_t vl);
vuint32m2_t __riscv_sf_vc_v_vvv_se_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2,
vuint32m2_t rs1, size_t vl);
vuint32m4_t __riscv_sf_vc_v_vvv_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2,
vuint32m4_t rs1, size_t vl);
vuint32m4_t __riscv_sf_vc_v_vvv_se_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2,
vuint32m4_t rs1, size_t vl);
vuint32m8_t __riscv_sf_vc_v_vvv_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2,
vuint32m8_t rs1, size_t vl);
vuint32m8_t __riscv_sf_vc_v_vvv_se_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2,
vuint32m8_t rs1, size_t vl);
vuint64m1_t __riscv_sf_vc_v_vvv_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2,
vuint64m1_t rs1, size_t vl);
vuint64m1_t __riscv_sf_vc_v_vvv_se_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2,
vuint64m1_t rs1, size_t vl);
vuint64m2_t __riscv_sf_vc_v_vvv_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2,
vuint64m2_t rs1, size_t vl);
vuint64m2_t __riscv_sf_vc_v_vvv_se_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2,
vuint64m2_t rs1, size_t vl);
vuint64m4_t __riscv_sf_vc_v_vvv_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2,
vuint64m4_t rs1, size_t vl);
vuint64m4_t __riscv_sf_vc_v_vvv_se_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2,
vuint64m4_t rs1, size_t vl);
vuint64m8_t __riscv_sf_vc_v_vvv_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2,
vuint64m8_t rs1, size_t vl);
vuint64m8_t __riscv_sf_vc_v_vvv_se_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2,
vuint64m8_t rs1, size_t vl);
void __riscv_sf_vc_xvv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2, uint8_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2, uint8_t xs1,
size_t vl);
void __riscv_sf_vc_xvv_se_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2, uint8_t xs1,
size_t vl);
void __riscv_sf_vc_xvv_se_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2, uint8_t xs1,
size_t vl);
```

```
void __riscv_sf_vc_xvv_se_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2, uint8_t xs1,
size_t vl);
void __riscv_sf_vc_xvv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t vs2,
uint16_t xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2, uint16_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2, uint16_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2, uint16_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2, uint16_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t vs2,
uint32_t xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2, uint32_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2, uint32_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2, uint32_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2, uint32_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2, uint64_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2, uint64_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2, uint64_t
xs1, size_t vl);
void __riscv_sf_vc_xvv_se_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2, uint64_t
xs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_xvv_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2,
uint8_t xs1, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_xvv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2,
uint8_t xs1, size_t vl);
vuint8mf4_t __riscv_sf_vc_v_xvv_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2,
uint8_t xs1, size_t vl);
vuint8mf4_t __riscv_sf_vc_v_xvv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2,
uint8_t xs1, size_t vl);
vuint8mf2_t __riscv_sf_vc_v_xvv_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2,
uint8_t xs1, size_t vl);
vuint8mf2_t __riscv_sf_vc_v_xvv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2,
uint8_t xs1, size_t vl);
vuint8m1_t __riscv_sf_vc_v_xvv_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2, uint8_t
xs1, size_t vl);
vuint8m1_t __riscv_sf_vc_v_xvv_se_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2,
uint8_t xs1, size_t vl);
vuint8m2_t __riscv_sf_vc_v_xvv_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2, uint8_t
xs1, size_t vl);
vuint8m2_t __riscv_sf_vc_v_xvv_se_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2,
uint8_t xs1, size_t vl);
vuint8m4_t __riscv_sf_vc_v_xvv_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2, uint8_t
xs1, size_t vl);
vuint8m4_t __riscv_sf_vc_v_xvv_se_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2,
uint8_t xs1, size_t vl);
```

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vuint8m8_t __riscv_sf_vc_v_xvv_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2, uint8_t
xs1, size_t vl);
vuint8m8_t __riscv_sf_vc_v_xvv_se_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2,
uint8_t xs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_xvv_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t vs2,
uint16_t xs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_xvv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t
vs2, uint16_t xs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_xvv_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t vs2,
uint16_t xs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_xvv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t
vs2, uint16_t xs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_xvv_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2,
uint16_t xs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_xvv_se_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2,
uint16_t xs1, size_t vl);
vuint16m2_t __riscv_sf_vc_v_xvv_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2,
uint16_t xs1, size_t vl);
vuint16m2_t __riscv_sf_vc_v_xvv_se_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2,
uint16_t xs1, size_t vl);
vuint16m4_t __riscv_sf_vc_v_xvv_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2,
uint16_t xs1, size_t vl);
vuint16m4_t __riscv_sf_vc_v_xvv_se_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2,
uint16_t xs1, size_t vl);
vuint16m8_t __riscv_sf_vc_v_xvv_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2,
uint16_t xs1, size_t vl);
vuint16m8_t __riscv_sf_vc_v_xvv_se_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2,
uint16_t xs1, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_xvv_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t vs2,
uint32_t xs1, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_xvv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t
vs2, uint32_t xs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_xvv_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2,
uint32_t xs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_xvv_se_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2,
uint32_t xs1, size_t vl);
vuint32m2_t __riscv_sf_vc_v_xvv_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2,
uint32_t xs1, size_t vl);
vuint32m2_t __riscv_sf_vc_v_xvv_se_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2,
uint32_t xs1, size_t vl);
vuint32m4_t __riscv_sf_vc_v_xvv_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2,
uint32_t xs1, size_t vl);
vuint32m4_t __riscv_sf_vc_v_xvv_se_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2,
uint32_t xs1, size_t vl);
vuint32m8_t __riscv_sf_vc_v_xvv_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2,
uint32_t xs1, size_t vl);
vuint32m8_t __riscv_sf_vc_v_xvv_se_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2,
uint32_t xs1, size_t vl);
vuint64m1_t __riscv_sf_vc_v_xvv_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2,
uint64_t xs1, size_t vl);
vuint64m1_t __riscv_sf_vc_v_xvv_se_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2,
uint64_t xs1, size_t vl);
vuint64m2_t __riscv_sf_vc_v_xvv_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2,
uint64_t xs1, size_t vl);
vuint64m2_t __riscv_sf_vc_v_xvv_se_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2,
uint64_t xs1, size_t vl);
```

```
vuint64m4_t __riscv_sf_vc_v_xvv_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2,
uint64_t xs1, size_t vl);
vuint64m4_t __riscv_sf_vc_v_xvv_se_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2,
uint64_t xs1, size_t vl);
vuint64m8_t __riscv_sf_vc_v_xvv_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2,
uint64_t xs1, size_t vl);
vuint64m8_t __riscv_sf_vc_v_xvv_se_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2,
uint64_t xs1, size_t vl);
void __riscv_sf_vc_ivv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2, int simm5,
size_t vl);
void __riscv_sf_vc_ivv_se_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2, int simm5,
size_t vl);
void __riscv_sf_vc_ivv_se_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2, int simm5,
size_t vl);
void __riscv_sf_vc_ivv_se_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2, int simm5,
size_t vl);
void __riscv_sf_vc_ivv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2, int
simm5, size_t vl);
void __riscv_sf_vc_ivv_se_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2, int
simm5, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_ivv_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2, int
simm5, size_t vl);
vuint8mf8_t __riscv_sf_vc_v_ivv_se_u8mf8 (int bit_field27_26, vuint8mf8_t vd, vuint8mf8_t vs2,
int simm5, size_t vl);
```

```
vuint8mf4_t __riscv_sf_vc_v_ivv_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2, int
simm5, size_t vl);
vuint8mf4_t __riscv_sf_vc_v_ivv_se_u8mf4 (int bit_field27_26, vuint8mf4_t vd, vuint8mf4_t vs2,
int simm5, size_t vl);
vuint8mf2_t __riscv_sf_vc_v_ivv_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2, int
simm5, size_t vl);
vuint8mf2_t __riscv_sf_vc_v_ivv_se_u8mf2 (int bit_field27_26, vuint8mf2_t vd, vuint8mf2_t vs2,
int simm5, size_t vl);
vuint8m1_t __riscv_sf_vc_v_ivv_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2, int
simm5, size_t vl);
vuint8m1_t __riscv_sf_vc_v_ivv_se_u8m1 (int bit_field27_26, vuint8m1_t vd, vuint8m1_t vs2, int
simm5, size_t vl);
vuint8m2_t __riscv_sf_vc_v_ivv_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2, int
simm5, size_t vl);
vuint8m2_t __riscv_sf_vc_v_ivv_se_u8m2 (int bit_field27_26, vuint8m2_t vd, vuint8m2_t vs2, int
simm5, size_t vl);
vuint8m4_t __riscv_sf_vc_v_ivv_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2, int
simm5, size_t vl);
vuint8m4_t __riscv_sf_vc_v_ivv_se_u8m4 (int bit_field27_26, vuint8m4_t vd, vuint8m4_t vs2, int
simm5, size_t vl);
vuint8m8_t __riscv_sf_vc_v_ivv_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2, int
simm5, size_t vl);
vuint8m8_t __riscv_sf_vc_v_ivv_se_u8m8 (int bit_field27_26, vuint8m8_t vd, vuint8m8_t vs2, int
simm5, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_ivv_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t vs2,
int simm5, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_ivv_se_u16mf4 (int bit_field27_26, vuint16mf4_t vd, vuint16mf4_t
vs2, int simm5, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_ivv_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t vs2,
int simm5, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_ivv_se_u16mf2 (int bit_field27_26, vuint16mf2_t vd, vuint16mf2_t
vs2, int simm5, size_t vl);
vuint16m1_t __riscv_sf_vc_v_ivv_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2, int
simm5, size_t vl);
vuint16m1_t __riscv_sf_vc_v_ivv_se_u16m1 (int bit_field27_26, vuint16m1_t vd, vuint16m1_t vs2,
int simm5, size_t vl);
vuint16m2_t __riscv_sf_vc_v_ivv_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2, int
simm5, size_t vl);
vuint16m2_t __riscv_sf_vc_v_ivv_se_u16m2 (int bit_field27_26, vuint16m2_t vd, vuint16m2_t vs2,
int simm5, size_t vl);
vuint16m4_t __riscv_sf_vc_v_ivv_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2, int
simm5, size_t vl);
vuint16m4_t __riscv_sf_vc_v_ivv_se_u16m4 (int bit_field27_26, vuint16m4_t vd, vuint16m4_t vs2,
int simm5, size_t vl);
vuint16m8_t __riscv_sf_vc_v_ivv_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2, int
simm5, size_t vl);
vuint16m8_t __riscv_sf_vc_v_ivv_se_u16m8 (int bit_field27_26, vuint16m8_t vd, vuint16m8_t vs2,
int simm5, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_ivv_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t vs2,
int simm5, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_ivv_se_u32mf2 (int bit_field27_26, vuint32mf2_t vd, vuint32mf2_t
vs2, int simm5, size_t vl);
vuint32m1_t __riscv_sf_vc_v_ivv_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2, int
simm5, size_t vl);
vuint32m1_t __riscv_sf_vc_v_ivv_se_u32m1 (int bit_field27_26, vuint32m1_t vd, vuint32m1_t vs2,
int simm5, size_t vl);
```

```
vuint32m2_t __riscv_sf_vc_v_ivv_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2, int
simm5, size_t vl);
vuint32m2_t __riscv_sf_vc_v_ivv_se_u32m2 (int bit_field27_26, vuint32m2_t vd, vuint32m2_t vs2,
int simm5, size_t vl);
vuint32m4_t __riscv_sf_vc_v_ivv_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2, int
simm5, size_t vl);
vuint32m4_t __riscv_sf_vc_v_ivv_se_u32m4 (int bit_field27_26, vuint32m4_t vd, vuint32m4_t vs2,
int simm5, size_t vl);
vuint32m8_t __riscv_sf_vc_v_ivv_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2, int
simm5, size_t vl);
vuint32m8_t __riscv_sf_vc_v_ivv_se_u32m8 (int bit_field27_26, vuint32m8_t vd, vuint32m8_t vs2,
int simm5, size_t vl);
vuint64m1_t __riscv_sf_vc_v_ivv_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2, int
simm5, size_t vl);
vuint64m1_t __riscv_sf_vc_v_ivv_se_u64m1 (int bit_field27_26, vuint64m1_t vd, vuint64m1_t vs2,
int simm5, size_t vl);
vuint64m2_t __riscv_sf_vc_v_ivv_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2, int
simm5, size_t vl);
vuint64m2_t __riscv_sf_vc_v_ivv_se_u64m2 (int bit_field27_26, vuint64m2_t vd, vuint64m2_t vs2,
int simm5, size_t vl);
vuint64m4_t __riscv_sf_vc_v_ivv_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2, int
simm5, size_t vl);
vuint64m4_t __riscv_sf_vc_v_ivv_se_u64m4 (int bit_field27_26, vuint64m4_t vd, vuint64m4_t vs2,
int simm5, size_t vl);
vuint64m8_t __riscv_sf_vc_v_ivv_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2, int
simm5, size_t vl);
vuint64m8_t __riscv_sf_vc_v_ivv_se_u64m8 (int bit_field27_26, vuint64m8_t vd, vuint64m8_t vs2,
int simm5, size_t vl);
void __riscv_sf_vc_fvv_se_u16mf4 (int bit_field26, vuint16mf4_t vd, vuint16mf4_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u16mf2 (int bit_field26, vuint16mf2_t vd, vuint16mf2_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u16m1 (int bit_field26, vuint16m1_t vd, vuint16m1_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u16m2 (int bit_field26, vuint16m2_t vd, vuint16m2_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u16m4 (int bit_field26, vuint16m4_t vd, vuint16m4_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u16m8 (int bit_field26, vuint16m8_t vd, vuint16m8_t vs2, float16_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u32mf2 (int bit_field26, vuint32mf2_t vd, vuint32mf2_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u32m1 (int bit_field26, vuint32m1_t vd, vuint32m1_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u32m2 (int bit_field26, vuint32m2_t vd, vuint32m2_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u32m4 (int bit_field26, vuint32m4_t vd, vuint32m4_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u32m8 (int bit_field26, vuint32m8_t vd, vuint32m8_t vs2, float32_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u64m1 (int bit_field26, vuint64m1_t vd, vuint64m1_t vs2, float64_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u64m2 (int bit_field26, vuint64m2_t vd, vuint64m2_t vs2, float64_t
fs1, size_t vl);
void __riscv_sf_vc_fvv_se_u64m4 (int bit_field26, vuint64m4_t vd, vuint64m4_t vs2, float64_t
fs1, size_t vl);
```

```
void __riscv_sf_vc_fvv_se_u64m8 (int bit_field26, vuint64m8_t vd, vuint64m8_t vs2, float64_t
fs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_fvv_u16mf4 (int bit_field26, vuint16mf4_t vd, vuint16mf4_t vs2,
float16_t fs1, size_t vl);
vuint16mf4_t __riscv_sf_vc_v_fvv_se_u16mf4 (int bit_field26, vuint16mf4_t vd, vuint16mf4_t vs2,
float16_t fs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_fvv_u16mf2 (int bit_field26, vuint16mf2_t vd, vuint16mf2_t vs2,
float16_t fs1, size_t vl);
vuint16mf2_t __riscv_sf_vc_v_fvv_se_u16mf2 (int bit_field26, vuint16mf2_t vd, vuint16mf2_t vs2,
float16_t fs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_fvv_u16m1 (int bit_field26, vuint16m1_t vd, vuint16m1_t vs2,
float16_t fs1, size_t vl);
vuint16m1_t __riscv_sf_vc_v_fvv_se_u16m1 (int bit_field26, vuint16m1_t vd, vuint16m1_t vs2,
float16_t fs1, size_t vl);
vuint16m2_t __riscv_sf_vc_v_fvv_u16m2 (int bit_field26, vuint16m2_t vd, vuint16m2_t vs2,
float16_t fs1, size_t vl);
vuint16m2_t __riscv_sf_vc_v_fvv_se_u16m2 (int bit_field26, vuint16m2_t vd, vuint16m2_t vs2,
float16_t fs1, size_t vl);
vuint16m4_t __riscv_sf_vc_v_fvv_u16m4 (int bit_field26, vuint16m4_t vd, vuint16m4_t vs2,
float16_t fs1, size_t vl);
vuint16m4_t __riscv_sf_vc_v_fvv_se_u16m4 (int bit_field26, vuint16m4_t vd, vuint16m4_t vs2,
float16_t fs1, size_t vl);
vuint16m8_t __riscv_sf_vc_v_fvv_u16m8 (int bit_field26, vuint16m8_t vd, vuint16m8_t vs2,
float16_t fs1, size_t vl);
vuint16m8_t __riscv_sf_vc_v_fvv_se_u16m8 (int bit_field26, vuint16m8_t vd, vuint16m8_t vs2,
float16_t fs1, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_fvv_u32mf2 (int bit_field26, vuint32mf2_t vd, vuint32mf2_t vs2,
float32_t fs1, size_t vl);
vuint32mf2_t __riscv_sf_vc_v_fvv_se_u32mf2 (int bit_field26, vuint32mf2_t vd, vuint32mf2_t vs2,
float32_t fs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_fvv_u32m1 (int bit_field26, vuint32m1_t vd, vuint32m1_t vs2,
float32_t fs1, size_t vl);
vuint32m1_t __riscv_sf_vc_v_fvv_se_u32m1 (int bit_field26, vuint32m1_t vd, vuint32m1_t vs2,
float32_t fs1, size_t vl);
vuint32m2_t __riscv_sf_vc_v_fvv_u32m2 (int bit_field26, vuint32m2_t vd, vuint32m2_t vs2,
float32_t fs1, size_t vl);
vuint32m2_t __riscv_sf_vc_v_fvv_se_u32m2 (int bit_field26, vuint32m2_t vd, vuint32m2_t vs2,
float32_t fs1, size_t vl);
vuint32m4_t __riscv_sf_vc_v_fvv_u32m4 (int bit_field26, vuint32m4_t vd, vuint32m4_t vs2,
float32_t fs1, size_t vl);
vuint32m4_t __riscv_sf_vc_v_fvv_se_u32m4 (int bit_field26, vuint32m4_t vd, vuint32m4_t vs2,
float32_t fs1, size_t vl);
vuint32m8_t __riscv_sf_vc_v_fvv_u32m8 (int bit_field26, vuint32m8_t vd, vuint32m8_t vs2,
float32_t fs1, size_t vl);
vuint32m8_t __riscv_sf_vc_v_fvv_se_u32m8 (int bit_field26, vuint32m8_t vd, vuint32m8_t vs2,
float32_t fs1, size_t vl);
vuint64m1_t __riscv_sf_vc_v_fvv_u64m1 (int bit_field26, vuint64m1_t vd, vuint64m1_t vs2,
float64_t fs1, size_t vl);
vuint64m1_t __riscv_sf_vc_v_fvv_se_u64m1 (int bit_field26, vuint64m1_t vd, vuint64m1_t vs2,
float64_t fs1, size_t vl);
vuint64m2_t __riscv_sf_vc_v_fvv_u64m2 (int bit_field26, vuint64m2_t vd, vuint64m2_t vs2,
float64_t fs1, size_t vl);
vuint64m2_t __riscv_sf_vc_v_fvv_se_u64m2 (int bit_field26, vuint64m2_t vd, vuint64m2_t vs2,
float64_t fs1, size_t vl);
vuint64m4_t __riscv_sf_vc_v_fvv_u64m4 (int bit_field26, vuint64m4_t vd, vuint64m4_t vs2,
float64_t fs1, size_t vl);
```

```
vuint64m4_t __riscv_sf_vc_v_fvv_se_u64m4 (int bit_field26, vuint64m4_t vd, vuint64m4_t vs2,
float64_t fs1, size_t vl);
vuint64m8_t __riscv_sf_vc_v_fvv_u64m8 (int bit_field26, vuint64m8_t vd, vuint64m8_t vs2,
float64_t fs1, size_t vl);
vuint64m8_t __riscv_sf_vc_v_fvv_se_u64m8 (int bit_field26, vuint64m8_t vd, vuint64m8_t vs2,
float64_t fs1, size_t vl);
```